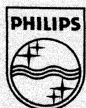
POWER SEMICONDUCTOR APPLICATIONS

Philips Semiconductors



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Preface

This book was prepared by the Power Semiconductor Applications Laboratory of the Philips Semiconductors product division, Hazel Grove. The book is intended as a guide to using power semiconductors both efficiently and reliably in power conversion applications. It is made up of seven main chapters each of which contains a number of application notes aimed at making it easier to select and use power semiconductors.

CHAPTER 1 forms an introduction to power semiconductors concentrating particularly on the two major power transistor technologies, Power MOSFETs and High Voltage Bipolar Transistors.

CHAPTER 2 is devoted to Switch Mode Power Supplies. It begins with a basic description of the most commonly used topologies and discusses the major issues surrounding the use of power semiconductors including rectifiers. Specific design examples are given as well as a look at designing the magnetic components. The end of this chapter describes resonant power supply technology.

CHAPTER 3 describes motion control in terms of ac, dc and stepper motor operation and control. This chapter looks only at transistor controls, phase control using thyristors and triacs is discussed separately in chapter 6.

CHAPTER 4 looks at television and monitor applications. A description of the operation of horizontal deflection circuits is given followed by transistor selection guides for both deflection and power supply applications. Deflection and power supply circuit examples are also given based on circuits designed by the Philips Components Application Laboratories (Eindhoven and Mitcham).

CHAPTER 5 concentrates on automotive electronics looking in detail at the requirements for the electronic switches taking into consideration the harsh environment in which they must operate.

CHAPTER 6 reviews thyristor and triac applications from the basics of device technology and operation to the simple design rules which should be followed to achieve maximum reliability. Specific examples are given in this chapter for a number of the common applications.

CHAPTER 7 looks at the thermal considerations for power semiconductors in terms of power dissipation and junction temperature limits. Part of this chapter is devoted to worked examples showing how junction temperatures can be calculated to ensure the limits are not exceeded. Heatsink requirements and designs are also discussed in the second half of this chapter.

Julian Humphreys

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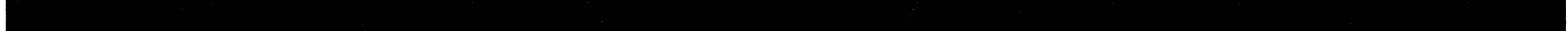

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CHAPTER 1

Introduction to Power Semiconductors

1.1 General

1.2 Power MOSFETS

1.3 High Voltage Bipolar Transistors

General

1.1.1 An Introduction To Power Devices

Today's mains-fed switching applications make use of a wide variety of active power semiconductor switches. This chapter considers the range of power devices on the market today, making comparisons both in terms of their operation and their general areas of application. The P-N diode will be considered first since this is the basis of all active switches. This will be followed by a look at both 3 layer and 4 layer switches.

Before looking at the switches let's briefly consider the various applications in which they are used. Virtually all mains fed power applications switch a current through an inductive load. This is the case even for resonant systems where the operating point is usually on the "inductive" side of the resonance curve. The voltage that the switch is normally required to block is, in the majority of cases, one or two times the maximum rectified input voltage depending on the configuration used. Resonant applications are the exception to this rule with higher voltages being generated by the circuit. For 110-240 V mains, the required voltage ratings for the switch can vary from 200 V to 1600 V.

Under normal operating conditions the off-state losses in the switch are practically zero. For square wave systems, the on-state losses (occurring during the on-time), are primarily determined by the on-state resistance which gives rise to an on-state voltage drop, V_{ON}. The (static) on-state losses may be calculated from:

$$P_{STATIC} = \delta . V_{ON} . I_{ON} \quad (1)$$

At the end of the "ON" time the switch is turned off. The turn-off current is normally high which gives rise to a loss dependent on the turn-off properties of the switch. The process of turn-on will also involve a degree of power loss so it is important not to neglect the turn-on properties either. Most applications either involve a high turn-on current or the current reaching its final value very quickly (high dI/dt). The total dynamic power loss is proportional to both the frequency and to the turn-on and turn-off energies.

$$P_{DYNAMIC} = f . (E_{ON} + E_{OFF}) \quad (2)$$

The total losses are the sum of the on-state and dynamic losses.

$$P_{TOT} = \delta . V_{ON} . I_{ON} + f . (E_{ON} + E_{OFF}) \quad (3)$$

The balance of these losses is primarily determined by the switch used. If the on-state loss dominates, operating frequency will have little influence and the maximum frequency of the device is limited only by its total delay time (the sum of all its switching times). At the other extreme a device whose on-state loss is negligible compared with the switching loss, will be limited in frequency due to the increasing dynamic losses.

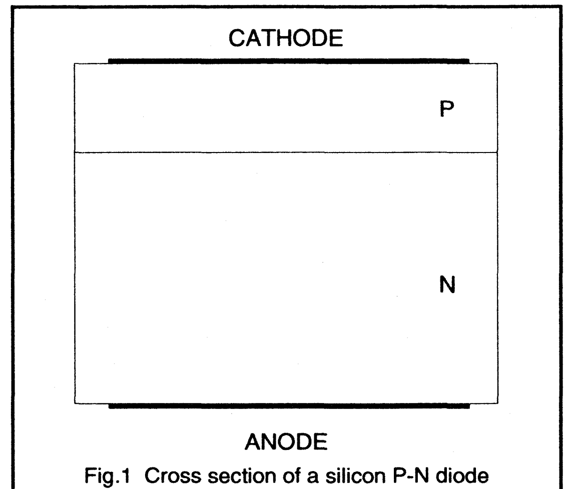


Fig.1 Cross section of a silicon P-N diode

High frequency switching When considering frequency limitation it is important to realise that the real issue is not just the frequency, but also the minimum on-time required. For example, an SMPS working at 100 kHz with an almost constant output power, will have a pulse on-time t_p of about 2-5 µs. This can be compared with a high performance UPS working at 10 kHz with low distortion which also requires a minimum on-time of 2 µs. Since the 10 kHz and 100 kHz applications considered here, require similar short on-times, both may be considered high frequency applications.

Resonant systems have the advantage of relaxing turn-on or turn-off or both. This however tends to be at the expense of V-A product of the switch. The relaxed switching conditions imply that in resonant systems switches can be used at higher frequencies than in non resonant systems. When evaluating switches this should be taken into account.

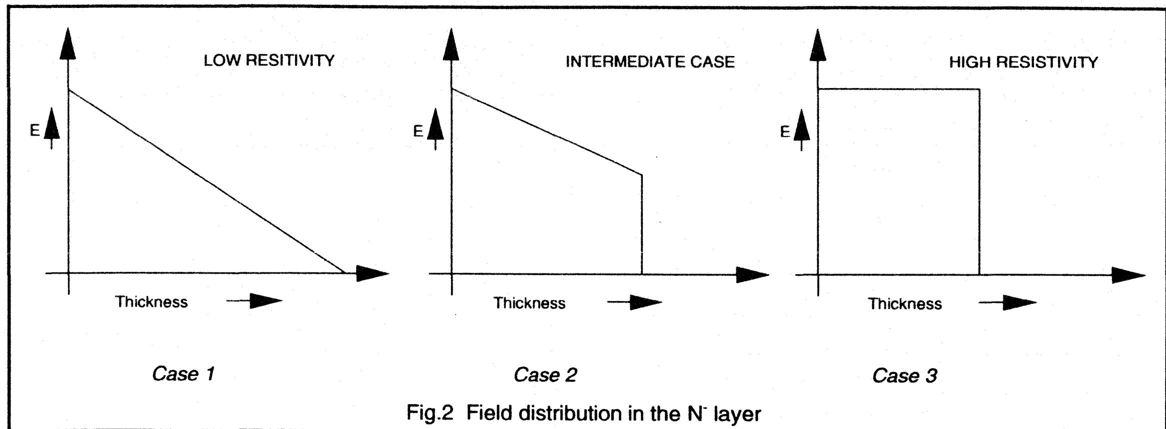


Fig.2 Field distribution in the N⁻ layer

At higher values of *throughput power*, the physical size of circuits increases and as a consequence, the stray inductances will also tend to increase. Since the required currents are higher, the energy stored in the stray inductances rises significantly, which in turn means the induced peak voltages also rise. As a result such applications force the use of longer pulse times, to keep losses down, and protection networks to limit overshoot or networks to slow down switching speeds. In addition the use of larger switches will also have consequences in terms of increasing the energy required to turn them on and off and drive energy is very important.

So, apart from the voltage and current capabilities of devices, it is necessary to consider static and dynamic losses, drive energy, dV/dt, dI/dt and Safe Operating Areas.

The silicon diode

Silicon is the semiconductor material used for all power switching devices. Lightly doped N^- silicon is usually taken as the starting material. The resistance of this material depends upon its resistivity, thickness and total area.

$$R = \rho . \frac{l}{A} \tag{4}$$

A resistor as such does not constitute an active switch, this requires an extra step which is the addition of a P-layer. The result is a diode of which a cross section is drawn in Fig.1

The blocking diode

Since all active devices contain a diode it is worth considering its structure in a little more detail. To achieve the high blocking voltages required for active power switches necessitates the presence of a thick N^- layer. To withstand a given voltage the N^- layer must have the right combination of thickness and resistivity. Some flexibility exists as to what that combination is allowed to be, the effects of varying the combination are described below.

Case 1: Wide N^- layer and low resistivity

Figure 2 gives the field profile in the N^- layer, assuming the junction formed with the P layer is at the left. The maximum field at the P-N junction is limited to 22 kV/cm by the breakdown properties of the silicon. The field at the other end is zero. The slope of the line is determined by the resistivity. The total voltage in the N^- layer is equal to the area underneath the curve. Please note that increasing the thickness of the device would not contribute to its voltage capability in this instance. This is the normal field profile when there is another P-layer at the back as in 4 layer devices (described later).

Case 2: Intermediate balance

The maximum field at the junction is the same, but the slope is less because of the higher resistivity of the material. The back now assumes the presence an N^+ layer, which is usually required for a good electrical contact. For the same voltage capability as in the previous case, this device will be thinner.

Case 3: High resistivity material

With sufficiently high resistivity material a near horizontal slope to the electric field is obtained. It is this scenario which will give rise to the thinnest possible devices for the same required breakdown voltage. Again an N^+ layer is required at the back.

An optimum thickness and resistivity exists which will give the lowest possible resistance for a given voltage capability. Both case 1 (very thick device) and case 3 (high resistivity) give high resistances, the table below shows the thickness and resistivity combinations possible for a 1000 V diode. The column named RA gives the resistance area product.

(A device thickness of less than 50 µm will never yield 1000 V and the same goes for a resistivity of less than 26 Ωcm.) The first specification is for the thinnest device possible and the last one is for the thickest device, (required when a P layer is present at the back). It can be seen that the lowest resistance is obtained with an intermediate value of resistivity and material thickness.

Thickness	Resistivity	RA	Comments
(µm)	(Ωcm)	Ωcm^2	
50	80	0.400	case 3
60	34	0.204	
65	30	0.195	
70	27	0.189	min. R
75	26	0.195	
80	26	0.208	
90	26	0.234	
100	26	0.260	case 1

To summarise, a designer of high voltage devices has only a limited choice of material resistivity and thickness with which to work. The lowest series resistance is obtained for a material thickness and resistivity intermediate between the possible extremes. This solution is the optimum for all majority carrier devices such as the PowerMOSFET and the J-FET where the on-resistance is uniquely defined by the series resistance. Other devices make use of charge storage effects to lower their on-state voltage. Consequently to optimise switching performance in these devices the best choice will be the thinnest layer such that the volume of stored charge is kept to a minimum. Finally as mentioned earlier, the design of a 4 layer device requires the thickest, low resistivity solution.

The forward biased diode

When a diode is forward biased, a forward current will flow. Internally this current will have two components: an electron current which flows from the N layer to the P layer and a hole current in the other direction. Both currents will generate a charge in the opposite layer (indicated with Q_P and Q_N in Fig.3). The highest doped region will deliver most of the current and generate most of the charge. Thus in a $P^+ N^-$ diode the current will primarily be made up of holes flowing from P to N and there will be a significant volume of hole charge in the N^- layer. This point is important when discussing active devices: whenever a diode is forward biased (such as a base-emitter diode) there will be a charge stored in the lowest doped region.

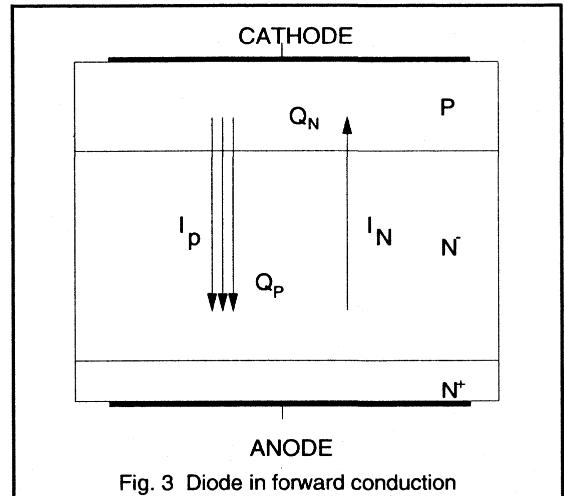


Fig. 3 Diode in forward conduction

The exact volume of charge that will result is dependent amongst other things on the minority carrier lifetime, τ. Using platinum or gold doping or by irradiation techniques the value of τ can be decreased. This has the effect of reducing the volume of stored charge and causing it to disappear more quickly at turn-off. A side effect is that the resistivity will increase slightly.

Three Layer devices

The three basic designs, which form the basis for all derived 3 layer devices, are given in Fig.4. It should be emphasised here that the discussion is restricted to high voltage devices only as indicated in the first section. This means that all relevant devices will have a *vertical structure*, characterised by a wide N^--layer.

The figure shows how a three layer device can be formed by adding an N type layer to the P-N diode structure. Two back to back P-N diodes thus form the basis of the device, where the P layer provides a means to control the current when the device is in the on-state.

There are three ways to use this P-layer as a control terminal. The first is to feed current into the terminal itself. The current through the main terminals is now proportional to the drive current. This device is called a *High Voltage Transistor* or *HVT*.

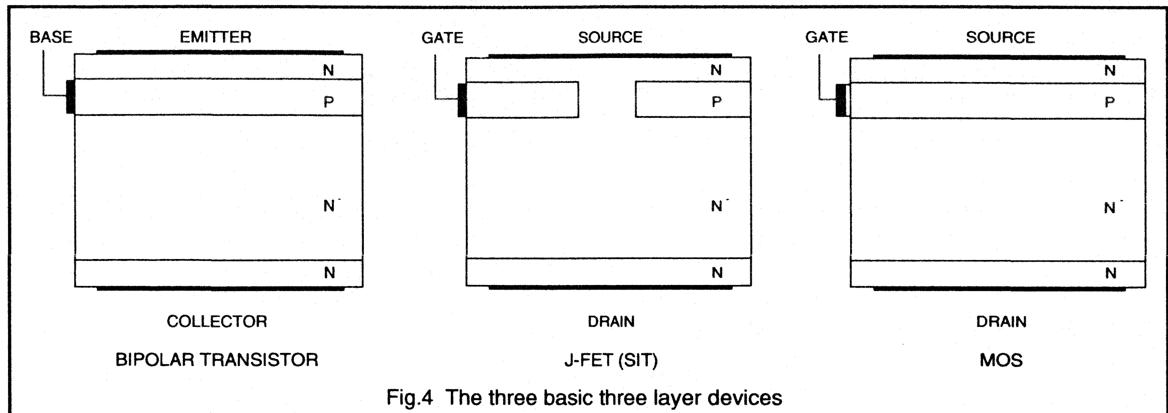


Fig.4 The three basic three layer devices

The second one is to have openings in the P-layer and permit the main current to flow between them. When reverse biasing the gate-source, a field is generated which blocks the opening and pinches off the main current. This device is known as the *J-FET* (junction FET) or *SIT* (Static Induction Transistor).

The third version has an electrode (gate) placed very close to the P-layer. The voltage on this gate pushes away the holes in the P-area and attracts electrons to the surface beneath the gate. A channel is thus formed between the main terminals so current can flow. The well known name for this device is *MOS transistor.*

In practice however, devices bear little resemblance to the constructions of Fig.4. In virtually all cases a planar construction is chosen i.e. the construction is such that one main terminal (emitter or source) and the drive contact are on the surface of the device. Each of the devices will now be considered in some more detail.

The High Voltage Transistor (HVT)

The *High Voltage Transistor* uses a positive base current to control the main collector current. The relation is: $I_C = H_{FE} * I_B$. The base current forward biases the base emitter P-N junction and, as explained previously, the ratio of both current components (electron / hole) depends on the doping. The base is made so thin that the emitter electrons immediately flow into the collector and by making the P-N$^+$ diode so the N$^+$ current will be much larger than the P-current, so $I_C >> I_B$.

When enough base drive is provided it is possible to forward bias the base-collector P-N junction also. This has a significant impact on the resistance of the N$^-$ layer; holes now injected from the P type base constitute stored charge causing a substantial reduction in on-state resistance, much lower than predicted by equation 4. Under these conditions the collector is an effective extension of the base.

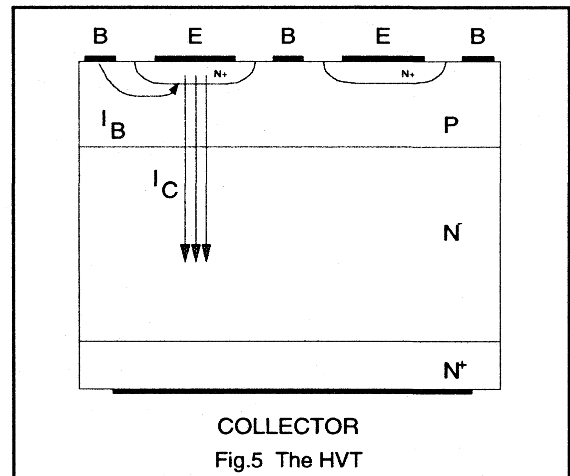


Fig.5 The HVT

Unfortunately the base current required to maintain this condition causes the current gain to drop. For this reason one cannot use a HVT at a very high current density because then the gain would become impractically low.

The on-state voltage of an HVT will be considerably lower than for a MOS or J-FET. This is its main advantage, but the resulting charge stored in the N$^-$ layer has to be delivered and also to be removed. This takes time and the speed of a bipolar transistor is therefore not optimal. To improve speed requires optimisation of a fine emitter structure in the form of fingers or cells.

Both at turn-on and turn-off considerable losses may occur unless care is taken to optimise drive conditions. At turn-on a short peak base current is normally required. At turn-off a negative base current is required and negative drive has to be provided.

A serious limitation of the HVT is the occurrence of *second breakdown* during switch off. The current contracts towards the middle of the emitter fingers and the current density can become very high. The RBSOAR (Reverse Bias Safe Operating Area) graph specifies where the device can be used safely. Device damage may result if the device is not properly used and one normally needs a snubber (dV/dt network) to protect the device. The price of such a snubber is normally in the order of the price of the transistor itself. In resonant applications it is possible to use the resonant properties of the circuit to have a slow dV/dt.

So, the bipolar transistor has the advantage of a very low forward voltage drop, at the cost of lower speed, a considerable energy is required to drive it and there are also limitations in the RBSOAR.

The J-FET.

The *J-FET* (Junction Field Effect Transistor) has a direct resistance between the Source and the Drain via the opening in the P-layer. When the gate-source voltage is zero the device is on. Its on-resistance is determined by the resistance of the silicon and no charge is present to make the resistance lower as in the case of the bipolar transistor. When a negative voltage is applied between Gate and Source, a depletion layer is formed which pinches off the current path. So, the current through the switch is determined by the voltage on the gate. The drive energy is low, it consists mainly of the charging and discharging of the gate-source diode capacitance. This sort of device is normally very fast.

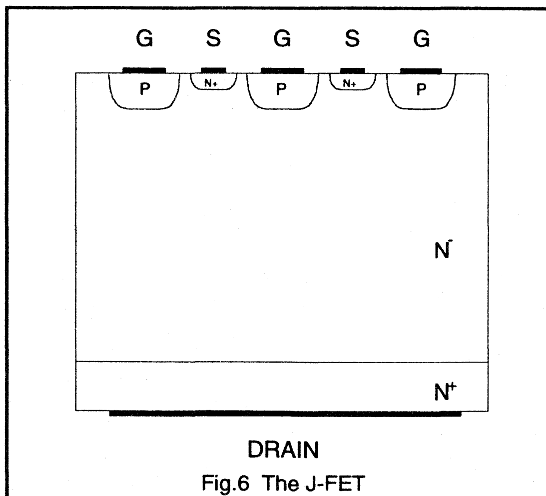


Fig.6 The J-FET

Its main difficulty is the opening in the P-layer. In order to speed up performance and increase current density, it is necessary to make a number of openings and this implies fine geometries which are difficult to manufacture. A solution exists in having the P-layer effectively on the surface, basically a diffused grid as shown in Fig.6. Unfortunately the voltages now required to turn the device off may be very big: it is not uncommon that a voltage of 25 V negative is needed. Obviously this is a major disadvantage which combined with its "normally-on" property and its difficulty to manufacture haven't yet lead to mass production of this device.

The MOS transistor.

The *MOS (Metal Oxide Semiconductor)* transistor is normally off: a positive voltage is required to induce a channel in the P-layer. When a positive voltage is applied to the gate, electrons are attracted to the surface beneath the gate area. In this way an "inverted" N-type layer is forced in the P-material providing a current path between drain and source.

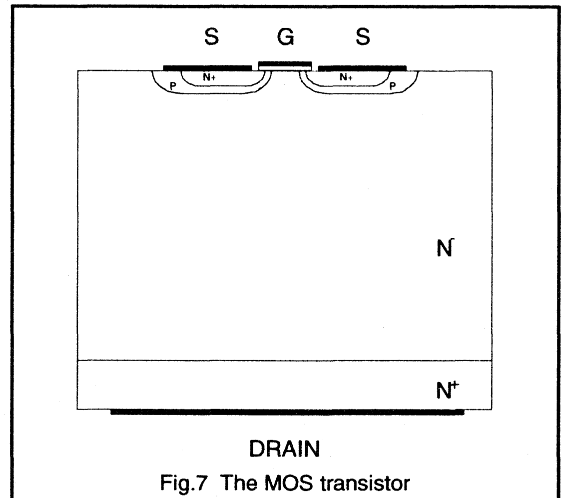


Fig.7 The MOS transistor

Modern technology allows a planar structure with very narrow cells as shown in Fig.7. The properties are quite like the J-FET with the exception that the charge is now across the (normally very thin) gate oxide. Charging and discharging the gate oxide capacitance requires drive currents when turning on and off. Switching speeds can be controlled by controlling the amount of drive charge during the switching interval. Unlike the J-FET it does not require a negative voltage although a negative voltage may help switch the device off quicker.

The MOSFET is the preferred device for higher frequency switching since it combines fast speed, easy drive and wide commercial availability.

Refinements to the basic structure

A number of techniques are possible to improve upon behaviour of the basic device.

First, the use of *finer geometries* can give lower on-state voltages, speed up devices and extend their energy handling capabilities. This has led to improved "Generation 3" devices for bipolars and to lower $R_{DS(ON)}$ for PowerMOS. Secondly, *killing the lifetime* τ in the device can also yield improvements. For bipolar devices, this positively effects the switching times. The gain, however, will drop, and this sets a maximum to the amount of lifetime killing. For MOS a lower value for τ yields the so-called FREDFETs, with an intrinsic diode fast enough for many half bridge applications such as in AC Motor Controllers. The penalty here is that $R_{DS(ON)}$ is adversely effected (slightly). Total losses, however, are decreased considerably.

Four layer devices

The three basic designs from the previous section can be extended with a P^+-layer at the back, thereby generating three basic Four Layer Devices. The addition of this extra layer creates a PNP transistor from the P^+-N^--P-layers. In all cases the 3 layer NPN device will now deliver an electron current into the back P^+-layer which acts as an emitter. The PNP transistor will thus become active which results in a hole current flowing from the P^+-layer into the high resistive region. This in its turn will lead to a *hole charge* in the high resistive region which lowers the on-state voltage considerably, as outlined above for High Voltage Transistors. Again, the penalty is in the switching times which will increase.

All the devices with an added P^+-layer at the back will inject holes into the N^--layer. Since the P^+-layer is much heavier doped than the N^--layer, this hole current will be the major contributor to the main current. This means that the charge in the N^--layer, especially near the N^--P^+-junction, will be large. Under normal operation the hole current will be large enough to influence the injection of electrons from the top N^+-layer. This results in extra electron current being injected from the top, leading to extra hole current from the back etc. This situation is represented in the schematic of Fig.8.

An important point is *latching*. This happens when the internal currents are such that we are not able to turn off the device using the control electrode. The only way to turn it off is by externally removing the current from the device.

The switching behaviour of all these devices is affected by the behaviour of the PNP: as long as a current is flowing through the device, the back will inject holes into the N^--layer. This leads to switching tails which contribute heavily to switching losses. The tail is strongly affected by the lifetime τ and by the application of negative drive current when possible. As previously explained, adjustment of the lifetime affects the on-state voltage. Carefully adjusting the lifetime τ will balance the on-state losses with the switching losses.

All four layer devices show this trade-off between switching losses and on-state losses. When minimising switching losses, the devices are optimised for high frequency applications. When the on-state losses are lowest the current density is normally highest, but the device is only useful at low frequencies. So two variants of the four layer device generally exist. In some cases intermediate speeds are also useful as in the case of very high power GTOs.

The Thyristor

A *thyristor* (or SCR, Silicon Controlled Rectifier) is essentially an HVT with an added P^+-layer. The resulting P^--N^--P^+ transistor is on when the whole device is on and provides enough base current to the N^+-P-N^- transistor to stay on. So after an initial kick-on, no further drive energy is required.

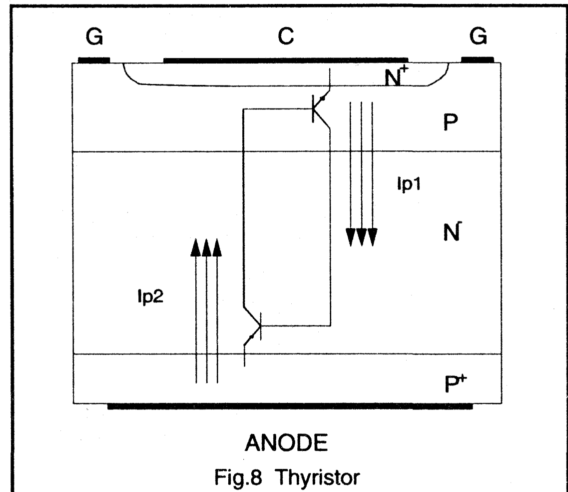


Fig.8 Thyristor

The classical thyristor is thus a latching device. Its construction is normally not very fine and as a result the gate contact is too far away from the centre of the active area to be able to switch it off. Also the current density is much higher than in a bipolar transistor. The switching times however are very long. Its turn-on is hampered by its structure since it takes quite a while for the whole crystal to become active. This seriously limits its dI/dt.

Once a thyristor is on it will only turn-off after having zero current for a few microseconds. This is done by temporarily forcing the current via a so-called commutation circuit.

The charge in the device originates from two sources: The standard NPN transistor structure injects holes in the N^--layer (I_{P1} in Fig.8) and the PNP transistor injects a charge from the back (I_{P2} in Fig.8). Therefore the total charge is big and switching performance is very poor. Due to its slow switching a normal thyristor is only suitable up to a few kHz.

A major variation on the thyristor is the *GTO* (Gate Turn Off Thyristor). This is a thyristor where the structure has been tailored to give better speed by techniques such as accurate lifetime killing, fine finger or cell structures and "anode shorts" (short circuiting P^+ and N^- at the back in order to decrease the current gain of the PNP transistor). As a result, the product of the gain of both NPN and PNP is just sufficient to keep the GTO conductive. A negative gate current is enough to sink the hole current from the PNP and turn the device off.

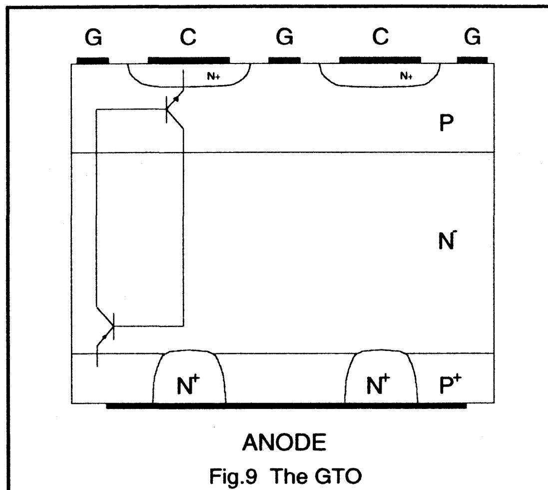


Fig.9 The GTO

A GTO shows much improved switching behaviour but still has the tail as described above. Lower power applications, especially resonant systems, are particularly attractive for the GTO because the turn-off losses are virtually zero.

The SITh

The *SITh* (Static Induction Thyristor) sometimes also referred to as *FCT* (Field Controlled Thyristor) is essentially a J-FET with an added P^+ back layer. In contrast to the standard thyristor, charge is normally only injected from the back, so the total amount of charge is limited. However, a positive gate drive is possible which will reduce on-state resistance.

Active extraction of charge via the gate contact is possible and switching speeds may be reduced considerably by applying an appropriate negative drive as in the case of an HVT. As for the SIT the technological complexity is a severe

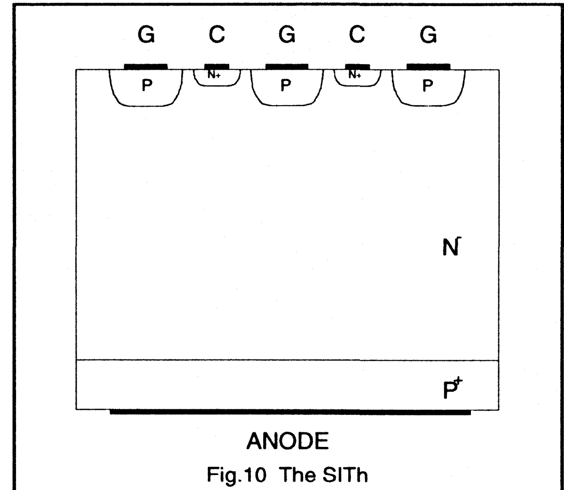


Fig.10 The SITh

drawback, as is its negative drive requirements. Consequently mass production of this device is not available yet.

The IGBT

An *IGBT* (Insulated Gate Bipolar Transistor) is an MOS transistor with P^+ at the back. Charge is injected from the back only, which limits the total amount of charge. Active charge extraction is not possible, so the carrier lifetime τ should be chosen carefully, since that determines the switching losses. Again two ranges are available with both fast and slow IGBTs.

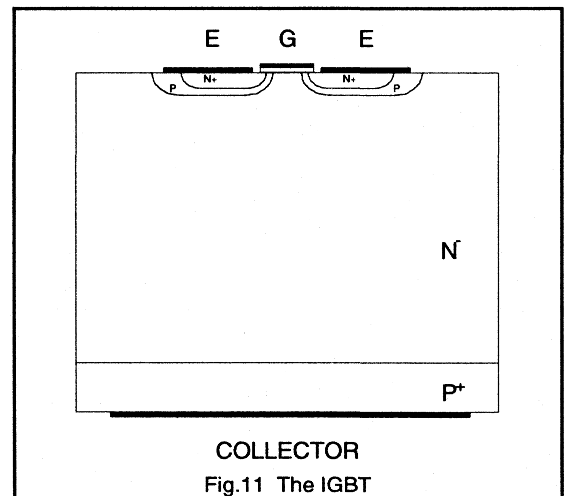


Fig.11 The IGBT

The speed of the fast IGBT is somewhat better than that of a GTO because a similar technology is used to optimise the IGBT but only the back P^+-layer is responsible for the charge.

The IGBT is gaining rapidly in popularity since its manufacturing is similar to producing PowerMOS and an increasing market availability exists. Although the latching of IGBTs was seen as a problem, modern optimised devices don't suffer from latch-up in practical conditions.

Refinements to the basic structure

The refinements outlined for 3 layer devices also apply to 4 layer structures. In addition to these, an N^+-layer may be inserted between the P^+ and N^--layer. Without such a layer the designer is limited in choice of starting material to Case 3 as explained in the diode section. Adding the extra N^+-layer allows another combination of resistivity and thickness to be used, improving device performance. An example of this is the ASCR, the Asymmetric SCR, which is much faster than normal thyristors. The reverse blocking capability, however, is now reduced to a value of 10-20 V.

Comparison of the Basic Devices.

It is important to consider the properties of devices mentioned when choosing the optimum switch for a particular application. Table 2 gives a survey of the essential device properties of devices capable of withstanding 1000 V. IGBTs have been classed in terms of fast and slow devices, however only the fast GTO and slow thyristor are represented. The fast devices are optimised for speed, the slow devices are optimised for On voltage.

Comments

This table is valid for 1000 V devices. Lower voltage devices will always perform better, higher voltage devices are worse.

A dot means an average value in between "+" and "-"

The "(--)" for a thyristor means a "--" in cases where forced commutation is used; in case of natural commutation it is "+"

Most figures are for reference only: in exceptional cases better performance has been achieved, but the figures quoted represent the state of the art.

	HVT	J-FET	MOS	THY	GTO	IGBT slow	IGBT fast	Unit
V(ON)	1	10	5	1.5	3	2	4	V
Positive Drive Requirement	-	+	+	+	+	+	+	+ = Simple to implement
Turn-Off requirement	-	-	+	(--)	-	+	+	+ = Simple to implement
Drive circuit complexity	-	.	+	(-)	.	+	+	- = complex
Technology Complexity	+	.	.	+	-	-	-	- = complex
Device Protection	-	.	+	+	-	-	-	+ = Simple to implement
Delay time (ts, tq)	2	0.1	0.1	5	1	2	0.5	µs
Switching Losses	.	++	++	--	-	-	.	+ = good
Current Density	50	12	20	200	100	50	50	A/cm^2
Max dv/dt (Vin = 0)	3	20	10	0.5	1.5	3	10	V/ns
dI/dt	1	10	10	1	0.3	10	10	A/ns
Vmax	1500	1000	1000	5000	4000	1000	1000	V
Imax	1000	10	100	5000	3000	400	400	A
Over Current factor	5	3	5	15	10	3	3	

Merged devices

Merged devices are the class of devices composed of two or more of the above mentioned basic types. They don't offer any breakthrough in device performance. This is understandable since the basic properties of the discussed devices are not or are hardly effected. They may be beneficial for the user though, primarily because they may result in lower positive and/or negative drive requirements.

Darlingtons and BiMOS

A darlington consists of two bipolar transistors. The emitter current of the first (the driver) forms the base current of the output transistor. The advantages of darlingtons may be summarised as follows. A darlington, obviously, has a higher gain than a single transistor. It also switches faster because the input transistor desaturates the output transistor and lower switching losses are the result. However, the resulting $V_{CE(sat)}$ is higher. The main issue, especially for higher powers is the savings in drive energy. This means that darlingtons can be used at considerably higher output powers than standard transistors. Modern darlingtons in high power packages can be used in 20 kHz motor drives and power supplies.

A BiMOS consists of a MOS driver and a bipolar output transistor. The positive drive is the same as MOS but turn-off is generally not so good. Adding a "speed-up" diode coupled with some negative drive improves things.

MCT

MCT stands for *MOS Controlled Thyristor*. This device is effectively a GTO with narrow tolerances, plus a P-MOS transistor between gate and source (P^+-N-P MOS, the left hand gate in Fig.12) and an extra N-MOS to turn it on, the N-P-N^--MOS shown underneath the right hand gate.

Where the GTO would like to be switched off with a negative gate, the internal GTO in an MCT can turn off by short circuiting its gate-cathode, due to its fine structure. Its drive therefore is like a MOS transistor and its behaviour similar to a GTO. Looking closely at the device it is obvious that a GTO using similar fine geometries with a suitable external drive can always perform better, at the cost of some drive circuitry. The only plus point seems to be its ease of drive.

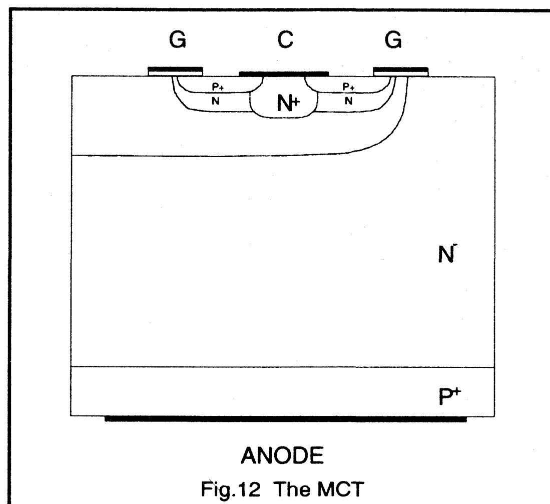


Fig.12 The MCT

IPS

The "ultimate" merged device is the *IPS* (Intelligent Power Switch). It integrates drive circuitry and intelligence with the power switch itself. Current sensing, over voltage detection and over temperature protection as well as status output are amongst the possibilities.

Application areas of the various devices

The following section gives an *indication* of where the various devices are best placed in terms of applications. It is possible for circuit designers to use various tricks to integrate devices and systems in innovative manners, applying devices far outside their 'normal' operating conditions. As an example, it is generally agreed that above 100 kHz bipolars are too difficult to use. However, a 450 kHz converter using bipolars has been already described in the literature.

As far as the maximum frequency is concerned a number of arguments must be taken into account.

First the *delay times*, either occurring at turn-on or at turn-off, will limit the maximum operating frequency. A reasonable rule of thumb for this is $f_{MAX} = 3 / t_{DELAY}$. (There is a danger here for confusion: switching times tend to depend heavily on circuit conditions, drive of the device and on current density. This may lead to a very optimistic or pessimistic expectation and care should be taken to consider reasonable conditions.)

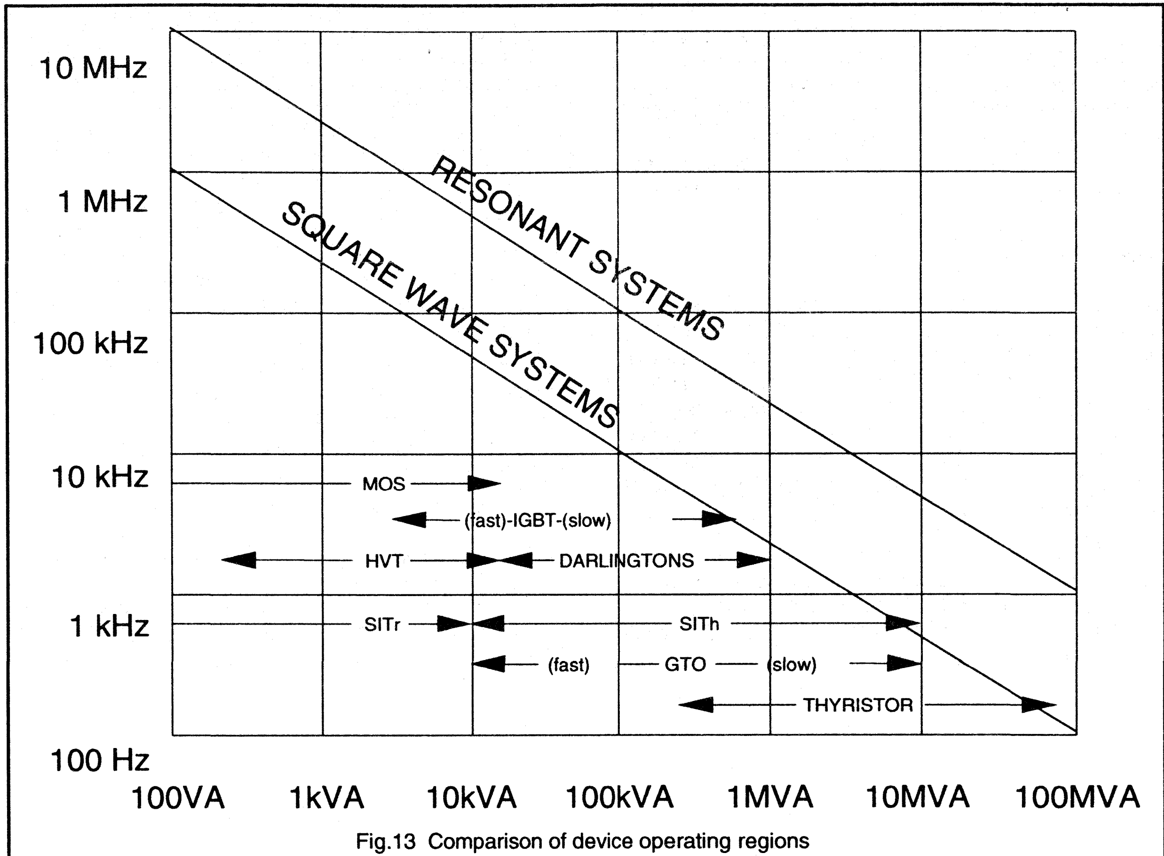


Fig.13 Comparison of device operating regions

Another factor is the *switching losses* which are proportional to the frequency. These power losses may be influenced by optimising the drive or by the addition of external circuits such as dV/dt or dI/dt networks. Alternatively the heatsink size may be increased or one may choose to operate devices at a lower current density in order to decrease power losses. It is clear that this argument is very subjective.

A third point is *manufacturability*. The use of fine structures for example, which improves switching performance, is possible only for small silicon chip sizes: larger chips with very fine MOS-like structures will suffer from unacceptable low factory yields. Therefore high power systems requiring large chip areas are bound to be made with less fine structures and will consequently be slower.

The *operating current density* of the device will influence its physical size. A low current density device aimed at high power systems would need a large outline which tends to be expensive. Large outlines also increase the physical size of the circuit, which leads to bigger parasitic inductances and associated problems.

High power systems will, because of the mechanical size, be restricted in speed as explained earlier in the text . This coincides well with the previously mentioned slower character of higher power devices.

Last but not least it is necessary to take the *application topology* into account. Resonant systems allow the use of considerably higher frequencies, since switching losses are minimised. Square wave systems cause more losses in the devices and thus restrict the maximum frequency. To make a comparison of devices and provide insight into which powers are realistic for which devices we have to take all the above mentioned criteria into account.

Fig.13 shows the optimum working areas of the various switching devices as a function of switchable power and frequency. The *switchable power* is defined as I_{AV} times V_{MAX} as seen by the device.

As an example, darlingtons will work at powers up to 1 MVA i.e. 1000 V devices will switch 1000 A. The frequency is then limited to 2.5 kHz. At lower powers higher frequencies can be achieved however above 50 kHz, darlingtons are not expected to be used. One should use this table only as guidance; using special circuit techniques, darlingtons have actually been used at higher frequencies. Clearly operation at lower powers and frequencies is always possible.

Conclusions

The starting material for active devices aimed at high voltage switching are made on silicon of which the minimum resistivity and thickness are limited. This essentially determines device performance, since all active switches incorporate such a layer. Optimisation can be performed for either minimum thickness, as required in the case of HVTs, or for minimum resistance, as required for MOS and J-FETs. The thickest variation (lowest resistivity) is required in the case of some 4 layer devices.

Basically three ways exist to control current through the devices: feeding a base current into a P-layer (transistor), using a voltage to pinch-off the current through openings in the P-layer (J-FET) and by applying a voltage onto a gate which inverts the underlying P-layer (MOS).

The HVT is severely limited in operating frequency due to its stored hole charge, but this at the same time allows a greater current density and a lower on-state voltage. It also requires more drive energy than both MOS and J-FET.

When we add a P^+-layer at the back of the three basic three layer devices we make three basic four layer devices. The P^+-layer produces a PNP transistor at the back which exhibits hole storage. This leads to much improved current densities and lower on-state losses, at the cost of switching speed. The four layer devices can be optimised for low on-state losses, in which case the switching will be poor, or for fast switching, in which case the on-state voltage will be high.

The properties of all six derived basic devices are determined to a large extent by the design of the high resistive area and can be optimised by applying technological features in the devices such as lifetime killing and fine geometries.

Resonant systems allow devices to be used at much higher frequencies due to the lower switching losses and the minimum on-times which may be longer, compared to square wave switching systems. Figure 13 gives the expected maximum frequency and switching power for the discussed devices. The difference for square wave systems and resonant systems is about a factor of 10.

Power MOSFET

1.2.1 PowerMOS Introduction

Device structure and fabrication

The idea of a vertical channel MOSFET has been known since the 1930s but it was not until the mid 1970s that the technology of diffusion, ion implantation and material treatment had reached the level necessary to produce DMOS on a commercial scale. The vertical diffusion technique uses technology more commonly associated with the manufacture of large scale integrated circuits than with traditional power devices. Figure 1(a) shows the vertical double implanted (DIMOS) channel structure which is the basis for all Philips power MOSFET devices.

An N-channel PowerMOS transistor is fabricated on an N^+substrate with a drain metallization applied to its' underside. Above the N^+substrate is an N^- epi layer, the thickness and resistivity of which depends on the required drain-source breakdown voltage. The channel structure, formed from a double implant in to the surface epi material, is laid down in a cellular pattern such that many thousands of cells go to make a single transistor. The N^+polysilicon gate which is embedded in an isolating silicon dioxide layer, is a single structure which runs between the cells across the entire active region of the device. The source metallization also covers the entire structure and thus parallels all the individual transistor cells on the chip. The layout of a typical low voltage chip is shown in Fig.1(b). The polysilicon gate is contacted by bonding to the defined pad area while the source wires are bonded directly to the aluminium over the cell array. The back of the chip is metallized with a triple layer of titanium/nickel/silver and this enables the drain connection to be formed using a standard alloy bond process.

The active part of the device consists of many cells connected in parallel to give a high current handling capability where the current flow is vertical through the chip. Cell density is determined by photolithographic tolerance requirements in defining windows in the polysilicon and gate-source oxide and also by the width of the polysilicon track between adjacent cells. The optimum value for polysilicon track width and hence cell density varies as a function of device drain-source voltage rating, this is explained in more detail further in the section. Typical cell densities are 1.6 million cells per square inch for low voltage types and 350,000 cells per square inch for high voltage types. The cell array is surrounded by an edge termination structure to control the surface electric field distribution in the device off-state.

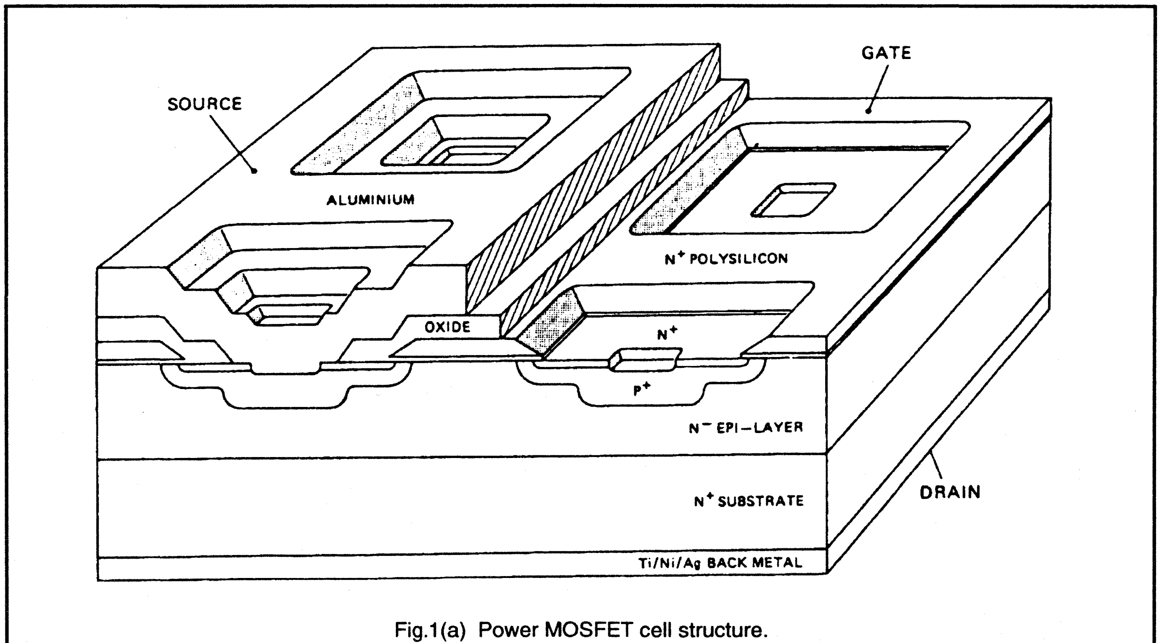


Fig.1(a) Power MOSFET cell structure.

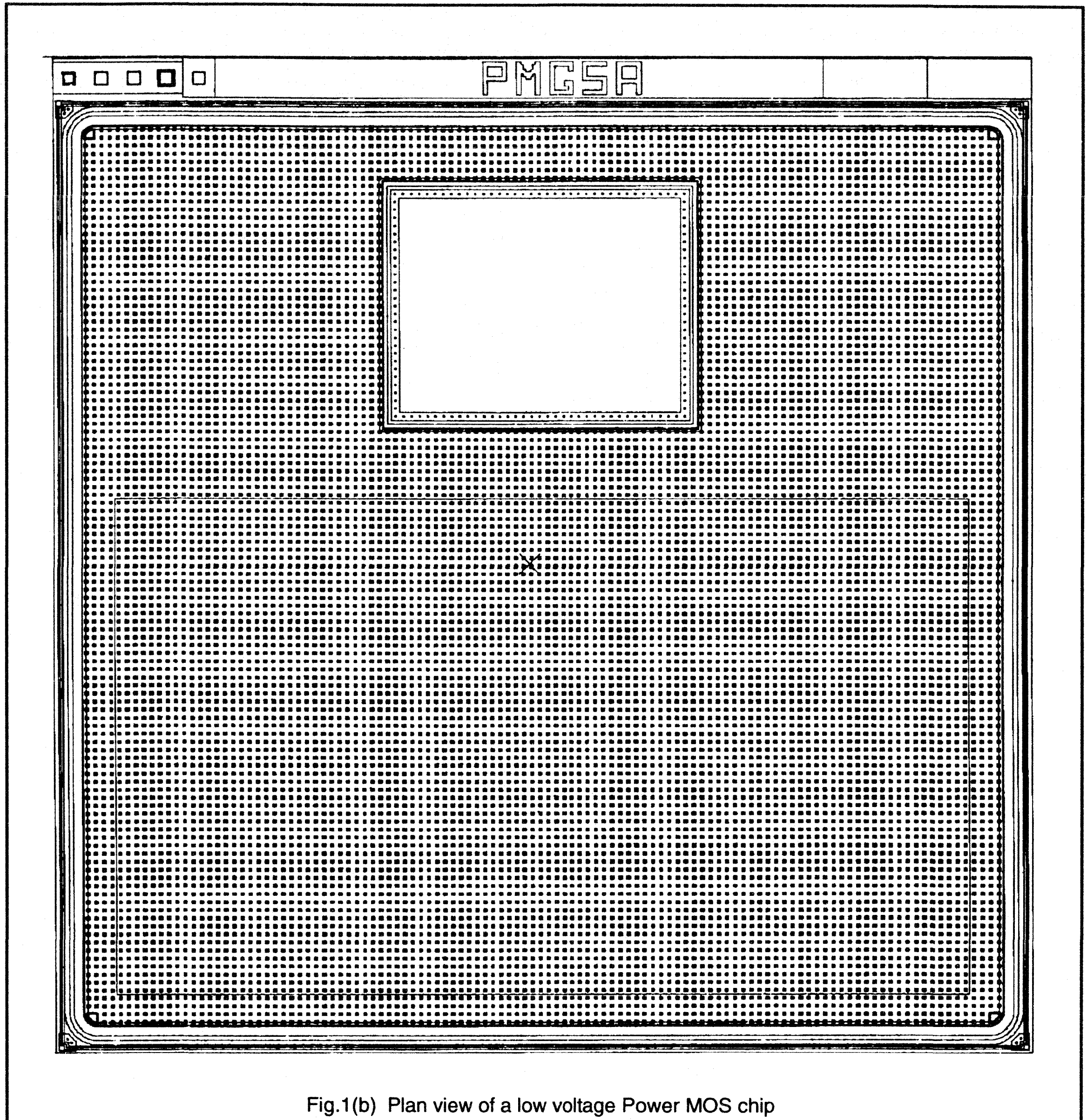


Fig.1(b) Plan view of a low voltage Power MOS chip

A cross-section through a single cell of the array is shown in Fig.2. The channel length is approximately 1.5 microns and is defined by the difference in the sideways diffusion of the N^+ source and the P-body. Both these diffusions are auto-aligned to the edge of the polysilicon gate during the fabrication process. All diffusions are formed by ion implantation followed by high temperature anneal/drive-in to give good parameter reproducibility. The gate is electrically isolated from the silicon by an 800 Angstrom layer of gate oxide (for standard types, 500 Angstrom for Logic level, see 1.1.6) and from the overlying aluminium by a thick layer of phosphorus doped oxide. Windows are defined in the latter oxide layer to enable the aluminium layer to contact the N^+ source and the P^+ diffusion in the centre of each cell. The P^+ diffusion provides a low resistance connection between the P^- body and ground potential, thus inhibiting turn-on of the inherent parasitic NPN bipolar structure.

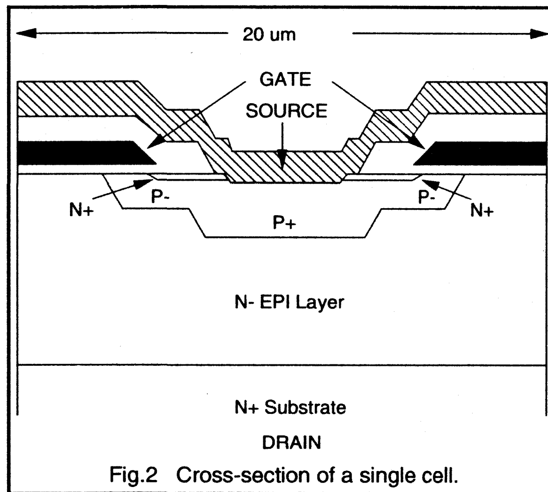


Fig.2 Cross-section of a single cell.

Device operation

Current flow in an enhancement mode power MOSFET is controlled by the voltage applied between the gate and source terminals. The P^- body isolates the source and drain regions and forms two P-N junctions connected back-to-back. With both the gate and source at zero volts there is no source-drain current flow and the drain sits at the positive supply voltage. The only current which can flow from source to drain is the reverse leakage current.

As the gate voltage is gradually made more positive with respect to the source, holes are repelled and a depleted region of silicon is formed in the P^- body below the silicon-gate oxide interface. The silicon is now in a 'depleted' state, but there is still no significant current flow between the source and drain.

When the gate voltage is further increased a very thin layer of electrons is formed at the interface between the P^- body and the gate oxide. This conductive N-type channel enhanced by the positive gate-source voltage, now permits current to flow from drain to source. The silicon in the P^- body is referred to as being in an 'inverted' state. A slight increase in gate voltage will result in a very significant increase in drain current and a corresponding rapid decrease in drain voltage, assuming a normal resistive load is present.

Eventually the drain current will be limited by the combined resistances of the load resistor and the $R_{DS(ON)}$ of the MOSFET. The MOSFET resistance reaches a minimum when V_{GS} = +10 volts (assuming a standard type). Subsequently reducing the gate voltage to zero volts reverses the above sequence of events. There are no stored charge effects since power MOSFETS are majority carrier devices.

Power MOSFET parameters

Threshold voltage

The threshold voltage is normally measured by connecting the gate to the drain and then determining the voltage which must be applied across the devices to achieve a drain current of 1.0 mA. This method is simple to implement and provides a ready indication of the point at which channel inversion occurs in the device.

The P^- body is formed by the implantation of boron through the tapered edge of the polysilicon followed by an anneal and drive-in. The main factors controlling threshold voltage are gate oxide thickness and peak surface concentration in the channel, which is determined by the P-body implant dose. To allow for slight process variation a window is usually defined which is 2.1 to 4.0 volts for standard types and 1.0 to 2.0 volts for logic level types.

Positive charges in the gate oxide, for example due to sodium, can cause the threshold voltage to drift. To minimise this effect it is essential that the gate oxide is grown under ultra clean conditions. In addition the polysilicon gate and phosphorus doped oxide layer provide a good barrier to mobile ions such as sodium and thus help to ensure good threshold voltage stability.

Drain-source on-state resistance

The overall drain-source resistance, $R_{DS(ON)}$, of a power MOSFET is composed of several elements, as shown in Fig.3.

The relative contribution from each of the elements varies with the drain-source voltage rating. For low voltage devices the channel resistance is very important while for

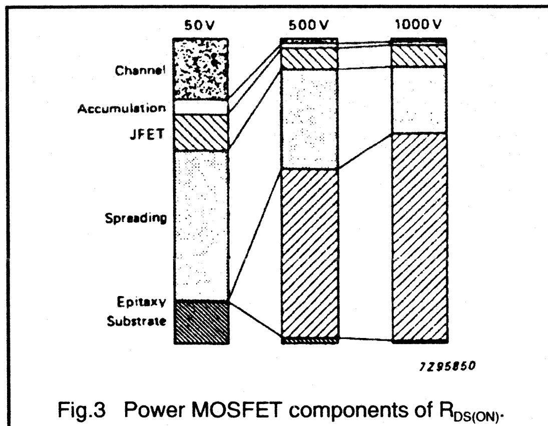


Fig.3 Power MOSFET components of $R_{DS(ON)}$.

the high voltage devices the resistivity and thickness of the epitaxial layer dominates. The properties of the various resistive components will now be discussed:

Channel. The unit channel resistance is determined by the channel length, gate oxide thickness, carrier mobility, threshold voltage, and the actual gate voltage applied to the device. The channel resistance for a given gate voltage can be significantly reduced by lowering the thickness of the gate oxide. This approach is used to fabricate the Logic Level MOSFET transistors and enables a similar value $R_{DS(ON)}$ to be achieved with only 5 volts applied to the gate. Of course, the gate-source voltage rating must be reduced to allow for the lower dielectric breakdown of the thinner oxide layer.

The overall channel resistance of a device is inversely proportional to channel width, determined by the total periphery of the cell windows. Channel width is over 200 cm for a 20 mm^2 low voltage chip. The overall channel resistance can be significantly reduced by going to higher cell densities, since the cell periphery per unit area is reduced.

Accumulation layer. The silicon interface under the centre of the gate track is 'accumulated' when the gate is biased above the threshold voltage. This provides a low resistance path for the electrons when they leave the channel, prior to entering the bulk silicon. This effect makes a significant contribution towards reducing the overall $R_{DS(ON)}$.

Parasitic JFET. After leaving the accumulation layer the electrons flow vertically down between the cells into the bulk of the silicon. Associated with each P-N junction there is a depletion region which, in the case of the high voltage devices, extends several microns into the N epitaxial region, even under zero bias conditions. Consequently the current path for the electrons is restricted by this parasitic JFET structure. The resistance of the JFET structure can be reduced by increasing the polysilicon track width. However this reduces the cell density. The need for compromise leads to an optimum value for the polysilicon track width for a given drain-source voltage rating. Since the zero-bias depletion width is greater for low doped material, then a wider polysilicon track width is used for high voltage chip designs.

Spreading resistance. As the electrons move further into the bulk of the silicon they are able to spread sideways and flow under the cells. Eventually paths overlap under the centre of each cell.

Epitaxial layer. The drain-source voltage rating requirements determine the resistivity and thickness of the epitaxial layer. For high voltage devices the resistance of the epitaxial layer dominates the overall value of $R_{DS(ON)}$.

Substrate. The resistance of the N^+ substrate is only significant in the case of 50 V devices.

Wires and leads. In a completed device the wire and lead resistances contribute a few milli-ohms to the overall resistance.

For all the above components the actual level of resistance is a function of the mobility of the current carrier. Since the mobility of holes is much lower than that of electrons the resistance of P-Channel MOSFETs is significantly higher than that of N-Channel devices. For this reason P-Channel types tend to be unattractive for most applications.

Drain-source breakdown voltage

The voltage blocking junction in the PowerMOS transistor is formed between the P-body diffusion and the N^- epi layer. For any P-N junction there exists a maximum theoretical breakdown voltage, which is dependent on doping profiles and material thickness. For the case of the N-channel PowerMOS transistor nearly all the blocking voltage is supported by the N^- epi layer. The ability of the N^- epi layer to support voltage is a function of its resistivity and thickness where both must increase to accommodate a higher breakdown voltage. This has obvious consequences in terms of drain-source resistance with $R_{DS(ON)}$ being approximately proportional to $B_{VDSS}^{2.5}$. It is therefore important to design PowerMOS devices such that the breakdown voltage is as close as possible to the theoretical maximum otherwise thicker, higher resistivity material has to be used. Computer models are used to investigate the influence of cell design and layout on breakdown voltage. Since these factors also influence the 'on-state' and switching performances a degree of compromise is necessary.

To achieve a high percentage of the theoretical breakdown maximum it is necessary to build edge structures around the active area of the device. These are designed to reduce the electric fields which would otherwise be higher in these regions and cause premature breakdown.

For low voltage devices this structure consists of a field plate design, Fig.4. The plates reduce the electric field intensity at the corner of the P^+ guard ring which surrounds the active cell area, and spread the field laterally along the surface of the device. The polysilicon gate is extended to form the first field plate, whilst the aluminium source metallization forms the second plate. The polysilicon termination plate which is shorted to the drain in the corners of the chip (not shown on the diagram) operates as a channel stopper. This prevents any accumulation of positive charge at the surface of the epi layer and thus improves stability. Aluminium overlaps the termination plate and provides a complete electrostatic screen against any external ionic charges, hence ensuring good stability of blocking performance.

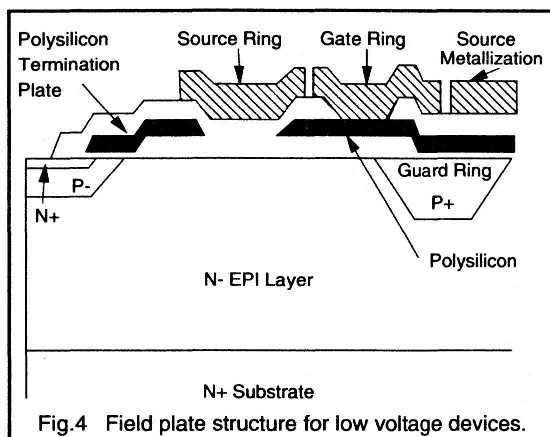


Fig.4 Field plate structure for low voltage devices.

For high voltage devices a set of floating P^+ rings, see Fig.5, is used to control the electric field distribution around the device periphery. The number of rings in the structure depends on the voltage rating of the device, eight rings are used for a 1000 volt type such as the BUK456-1000A. A three dimensional computer model enables the optimum ring spacing to be determined so that each ring experiences a similar field intensity as the structure approaches avalanche breakdown. The rings are passivated with polydox which acts as an electrostatic screen and prevents external ionic charges inverting the lightly doped N^- interface to form P^- channels between the rings. The polydox is coated with layers of silicon nitride and phosphorus doped oxide.

All types have a final passivation layer of plasma nitride, which acts as a further barrier to mobile charge and also gives anti-scratch protection to the top surface.

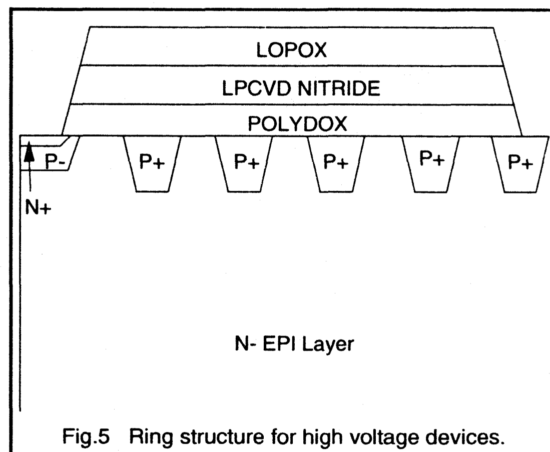


Fig.5 Ring structure for high voltage devices.

Electrical characteristics

The DC characteristic

If a dc voltage source is connected across the drain and source terminals of an N channel enhancement mode MOSFET, with the positive terminal connected to the drain, the following characteristics can be observed. With the gate to source voltage held below the threshold level negligible current will flow when sweeping the drain source voltage positive from zero. If the gate to source voltage is taken above the threshold level, increasing the drain to source voltage will cause current to flow in the drain. This current will increase as the drain-source voltage is increased up to a point known as the pinch off voltage. Increasing the drain-source terminal voltage above this value will not produce any significant increase in drain current.

The pinch off voltage arises from a rapid increase in resistance which for any particular MOSFET will depend on the combination of gate voltage and drain current. In its simplest form, pinch off will occur when the ohmic drop across the channel region directly beneath the gate becomes comparable to the gate to source voltage. Any further increase in drain current would now reduce the net voltage across the gate oxide to a level which is no longer sufficient to induce a channel. The channel is thus pinched off at its edge furthest from the source N^+ (see Fig.6).

A typical set of output characteristics is shown in Fig.7. The two regions of operation either side of the pinch off voltage can be seen clearly. The region at voltages lower than the pinch off value is usually known as the ohmic region. Saturation region is the term used to describe that part of the characteristic above the pinch-off voltage. (NB This definition of saturation is different to that used for bipolar devices.)

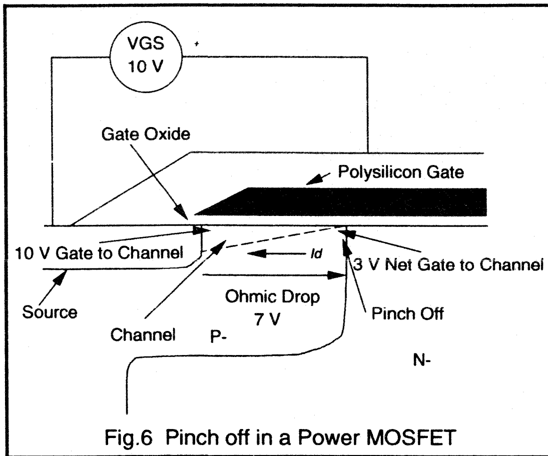


Fig.6 Pinch off in a Power MOSFET

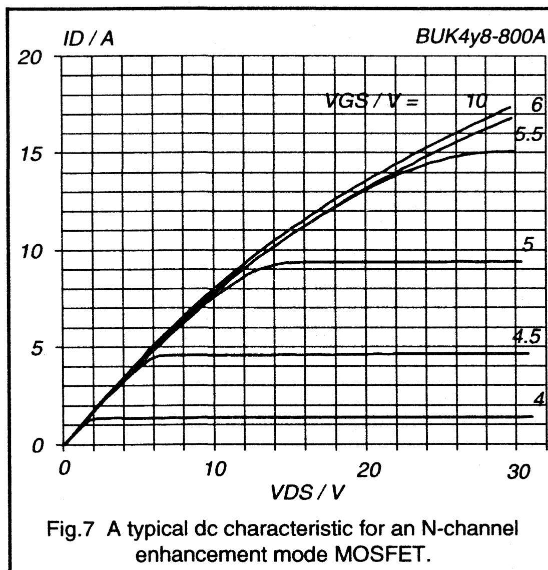


Fig.7 A typical dc characteristic for an N-channel enhancement mode MOSFET.

The switching characteristics

The switching characteristics of a Power MOSFET are determined largely by the various capacitances inherent in its' structure. These are shown in Fig.8.

To turn the device on and off the capacitances have to be charged and discharged, the rate at which this can be achieved is dependent on the impedance and the current sinking/sourcing capability of the drive circuit. Since it is only the majority carriers that are involved in the conduction process, MOSFETs do not suffer from the same storage time problems which limit bipolar devices where minority carriers have to be removed during turn-off. For most applications therefore the switching times of the Power

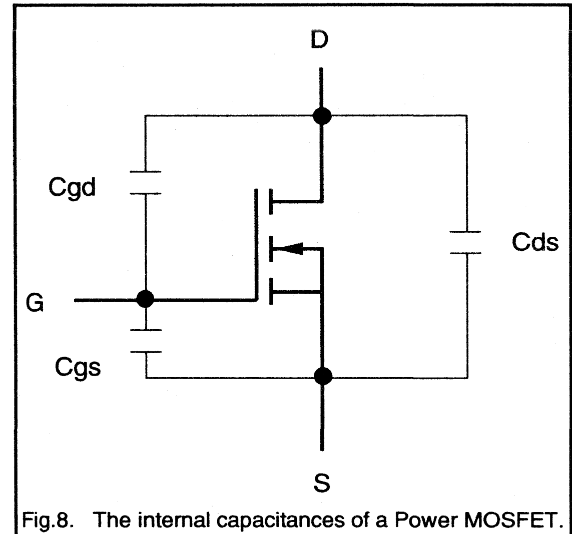


Fig.8. The internal capacitances of a Power MOSFET.

MOSFET are limited only by the drive circuit and can be very fast. Temperature has only a small effect on device capacitances therefore switching times are independent of temperature.

In Fig.9 typical gate-source and drain-source voltages for a MOSFET switching current through a resistive load are shown. The gate source capacitance needs to be charged up to a threshold voltage of about 3 V before the MOSFET begins to turn on. The time constant for this is $C_{GS}(R_{DR}+R_G)$ and the time taken is called the turn-on delay time ($t_{D(ON)}$). As V_{GS} starts to exceed the threshold voltage the MOSFET begins to turn on and V_{DS} begins to fall. C_{GD} now needs to be discharged as well as C_{GS} being charged so the time constant is increased and the gradient of V_{GS} is reduced. As V_{DS} becomes less than V_{GS} the value of C_{GD} increases sharply since it is depletion dependent. A plateau thus occurs in the V_{GS} characteristic as the drive current goes into the charging of C_{GD}.

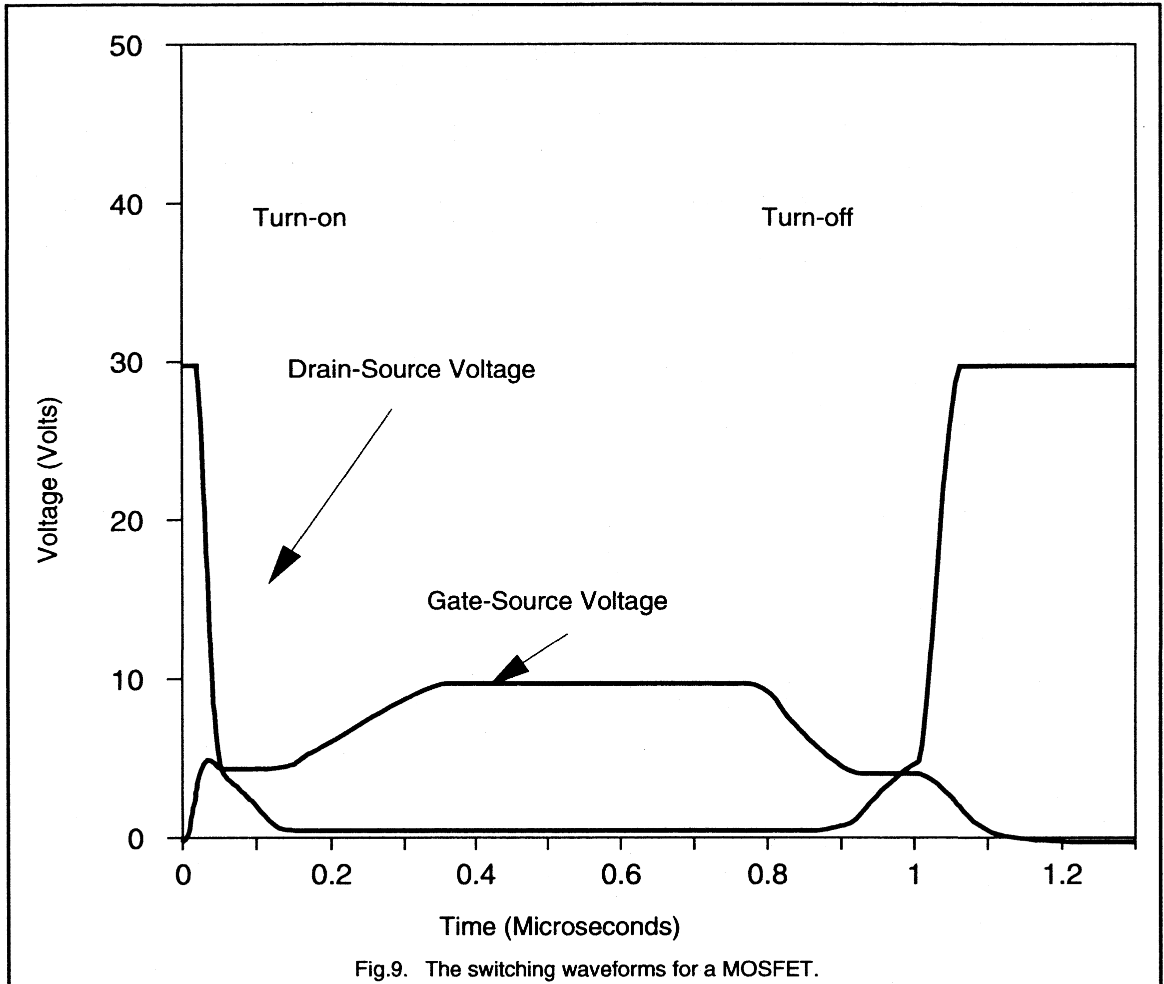


Fig.9. The switching waveforms for a MOSFET.

When V_{DS} has collapsed V_{GS} continues to rise as overdrive is applied. Gate overdrive is necessary to reduce the on-resistance of the MOSFET and thereby keep power loss to a minimum.

To turn the MOSFET off the overdrive has first to be removed. The charging path for C_{GD} and C_{DS} now contains the load resistor (R_L) and so the turn-off time will be generally longer than the turn-on time.

The Safe Operating Area

Unlike bipolar devices Power MOSFETs do not suffer from second breakdown phenomena when operated within their voltage rating. Essentially therefore the safe operating area of a Power MOSFET is determined only by the power necessary to raise its junction temperature to the rated maximum of 150 ˚C or 175 ˚C (which T_{JMAX} depends on package and voltage rating). Whether a MOSFET is being operated safely with respect to thermal stress can thus be determined directly from knowledge of the power function applied and the thermal impedance characteristics.

A safe operating area calculated assuming a mounting base temperature of 25 ˚C is shown in Fig.10 for a BUK438-800 device. This plot shows the constant power curves for a variety of pulse durations ranging from dc to 10 µs. These curves represent the power levels which will raise T_j up to the maximum rating. Clearly for mounting base temperatures higher than 25 ˚C the safe operating area is smaller. In addition it is not usually desirable to operate the

device at its T_{JMAX} rating. These factors can be taken into account quite simply where maximum power capability for a particular application is calculated from:

$$P_{max} = \frac{(T_j - T_{mb})}{Z_{th}}$$

T_j is the desired operating junction temperature (must be less than T_{jmax})
T_{mb} is the mounting base temperature
Z_{th} is the thermal impedance taken from the data curves

The safe operating area is bounded by a peak pulse current limit and a maximum voltage. The peak pulse current is based on a current above which internal connections may be damaged. The maximum voltage is an upper limit above which the device may go into avalanche breakdown.

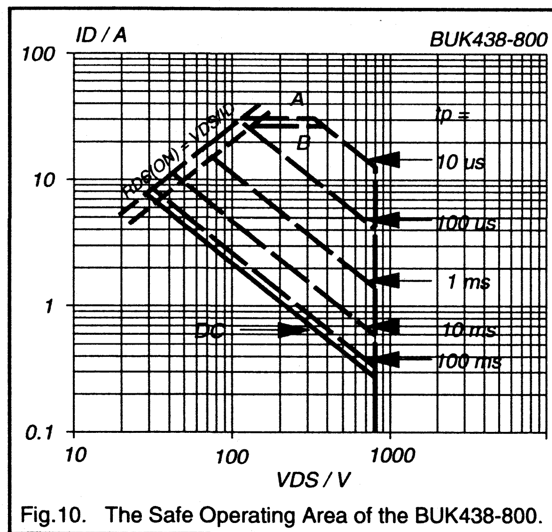


Fig.10. The Safe Operating Area of the BUK438-800.

In a real application the case temperature will be greater than 25 ˚C because of the finite thermal impedance of practical heatsinks. Also a junction temperature of between 80 ˚C and 125 ˚C would be preferable since this improves reliability. If a nominal junction temperature of 80 ˚C instead of 150 ˚C is used then the ability of the MOSFET to withstand current spikes is improved.

Causes of Power Loss

There are four main causes of power dissipation in MOSFETs.

Conduction losses - The conduction losses (P_C) are given by equation (1).

$$P_C = I_D^2 . R_{DS(ON)} \qquad (1)$$

It is important to note that the on-resistance of the MOSFET when it is operated in the Ohmic region is dependent on the junction temperature. On-resistance roughly doubles between 25 ˚C and 150 ˚C, the exact characteristics are shown in the data sheets for each device.

Switching losses - When a MOSFET is turned on or off it carries a large current and sustains a large voltage at the same time. There is therefore a large power dissipation during the switching interval. Switching losses are negligible at low frequencies but are dominant at high frequencies. The cross-over frequency depends on the circuit configuration. For reasons explained in the section on switching characteristics, a MOSFET usually turns off more slowly than it turns on so the losses at turn-off will be larger than at turn-on. Switching losses are very dependent on circuit configuration since the turn-off time is affected by the load impedance.

Turn-off losses may be reduced by the use of snubber components connected across the MOSFET which limit the rate of rise of voltage. Inductors can be connected in series with the MOSFET to limit the rate of rise of current at turn-on and reduce turn-on losses. With resonant loads switching can take place at zero crossing of voltage or current so switching losses are very much reduced.

Diode losses - These losses only occur in circuits which make use of the antiparallel diode inherent in the MOSFET structure. A good approximation to the dissipation in the diode is the product of the diode voltage drop which is typically less than 1.5 V and the average current carried by the diode. Diode conduction can be useful in such circuits as pulse width modulated circuits used for motor control, in some stepper motor drive circuits and in voltage fed circuits feeding a series resonant load.

Gate losses - The losses in the gate are given in equation 2 where R_G is the internal gate resistance, R_{DR} is the external drive resistance, V_{GSD} is the gate drive voltage and C_{IP} is the capacitance seen at the input to the gate of the MOSFET.

$$P_G = \frac{C_{IP} . V_{GSD}^2 . f . R_G}{(R_G + R_{DR})} \qquad (2)$$

The input capacitance varies greatly with the gate drain voltage so the expression in equation 3 is more useful.

$$P_G = \frac{Q_G . V_{GSD} . f . R_G}{(R_G + R_{DR})} \qquad (3)$$

(3)

Where Q_G is the peak gate charge.

Parallel Operation

If power requirements exceed those of available devices then increased power levels can be achieved by parallelling devices. Parallelling of devices is made easier using

MOSFETs because they have a positive temperature coefficient of resistance. If one parallelled MOSFET carries more current than the others it becomes hotter. This causes the on-resistance of that particular device to become greater than that of the others and so the current in it reduces. This mechanism opposes thermal runaway in one of the devices. The positive temperature coefficient also helps to prevent hot spots within the MOSFET itself.

Applications of Power MOSFETs

Power MOSFETs are ideally suited for use in many applications, some of which are listed below. Further information on the major applications is presented in subsequent chapters.

Chapter 2: Switched mode power supplies (SMPS)

Chapter 3: Variable speed motor control.

Chapter 5: Automotive switching applications.

Conclusions

It can be seen that the operation of the Power MOSFET is relatively easy to understand. The advantages of fast switching times, ease of parallelling and low drive power requirements make the device attractive for use in many applications.

1.2.2 Understanding Power MOSFET Switching Behaviour

Power MOSFETs are well known for their ease of drive and fast switching behaviour. Being majority carrier devices means they are free of the charge storage effects which inhibit the switching performance of bipolar products. How fast a Power MOSFET will switch is determined by the speed at which its internal capacitances can be charged and discharged by the drive circuit. MOSFET switching times are often quoted as part of the device data however as an indication as to the true switching capability of the device, these figures are largely irrelevant. The quoted values are only a snapshot showing what will be achieved under the stated conditions.

This report sets out to explain the switching characteristics of Power MOSFETs. It will consider the main features of the switching cycle distinguishing between what is device determinant and what can be controlled by the drive circuit. The requirements for the drive circuit are discussed in terms of the energy that it must supply as well as the currents it is required to deliver. Finally, how the drive circuit influences switching performance, in terms of switching times, dV/dt and dI/dt will be reviewed.

Voltage dependent capacitance

The switching characteristics of the Power MOSFET are determined by its capacitances. These capacitances are not fixed but are a function of the relative voltages between each of the terminals. To fully appreciate Power MOSFET switching, it is necessary to understand what gives rise to this voltage dependency.

Parallel plate capacitance is expressed by the well known equation

$$C = E\frac{a}{d} \qquad 1$$

where 'a' is the area of the plates, d is the separating distance and E is the permittivity of the insulating material between them. For a parallel plate capacitor, the plates are surfaces on which charge accumulation / depletion occurs in response to a change in the voltage applied across them. In a semiconductor, static charge accumulation / depletion can occur either across a PN junction or at semiconductor interfaces either side of a separating oxide layer.

i) P-N junction capacitance

The voltage supporting capability of most power semiconductors is provided by a reverse biased P-N junction. The voltage is supported either side of the junction by a region of charge which is exposed by the applied voltage. (Usually referred to as the depletion region because it is depleted of majority carriers.) Fig.1 shows how the electric field varies across a typical P-N$^-$ junction for a fixed dc voltage. The shaded area beneath the curve must be equal to the applied voltage. The electric field gradient is fixed, independent of the applied voltage, according to the concentration of exposed charge. (This is equal to the background doping concentration used during device manufacture.) A slight increase in voltage above this dc level will require an extension of the depletion region, and hence more charge to be exposed at its edges, this is illustrated in Fig.1. Conversely a slight reduction in voltage will cause the depletion region to contract with a removal of exposed charge at its edge. Superimposing a small ac signal on the dc voltage thus causes charge to be added and subtracted at either side of the depletion region of width d1. The effective capacitance per unit area is

$$C1 = \frac{E}{d1} \qquad 2$$

Since the depletion region width is voltage dependent it can be seen from Fig.1 that if the dc bias is raised to say V2, the junction capacitance becomes

$$C2 = \frac{E}{d2} \qquad 3$$

Junction capacitance is thus dependent on applied voltage with an inverse relationship.

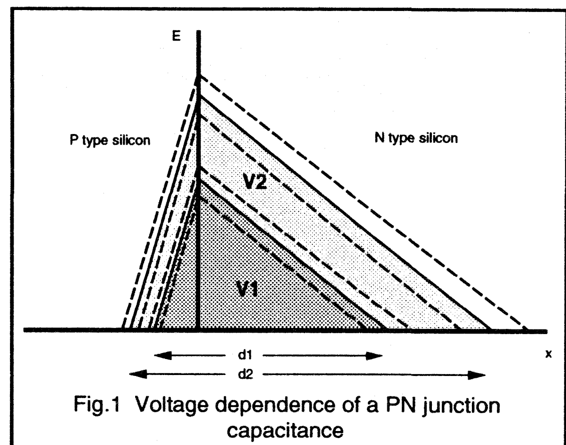


Fig.1 Voltage dependence of a PN junction capacitance

ii) Oxide capacitance

Fig.2 shows two semiconductor layers separated by an insulating oxide. In this case the surface layer is polysilicon

(representative of the PowerMOS gate structure) and the lower layer is a P-type substrate. Applying a negative voltage to the upper layer with respect to the lower will cause positive charge accumulation at the surface of the P-doped material (positively charged holes of the P material are attracted by the negative voltage). Any changes in this applied voltage will cause a corresponding change in the accumulation layer charge. The capacitance per unit area is thus

$$Cox = \frac{E}{t} \quad 4$$

where t = oxide thickness

Applying a positive voltage to the gate will cause a depletion layer to form beneath the oxide, (ie the positively charged holes of the P-material are repelled by the positive voltage). The capacitance will now decrease with increasing positive gate voltage as a result of widening of the depletion layer. Increasing the voltage beyond a certain point results in a process known as inversion; electrons pulled into the conduction band by the electric field accumulate at the surface of the P-type semiconductor. (The voltage at which this occurs is the threshold voltage of the power MOSFET.) Once the inversion layer forms, the depletion layer width will not increase with additional dc bias and the capacitance is thus at its minimum value. (NB the electron charge accumulation at the inversion layer cannot follow a high frequency ac signal in the structure of Fig.2, so high frequency capacitance is still determined by the depletion layer width.) The solid line of Fig.3 represents the capacitance-voltage characteristic of an MOS capacitor.

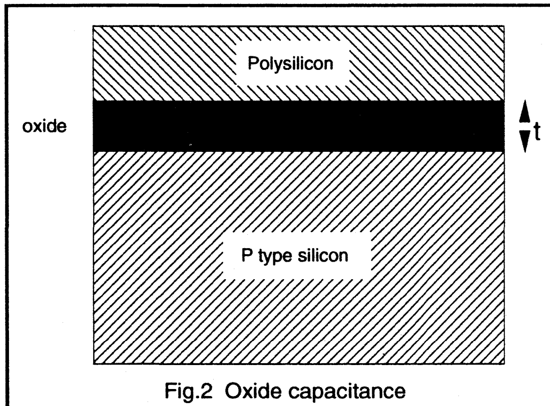


Fig.2 Oxide capacitance

In a power MOSFET the solid line is not actually observed; the formation of the inversion layer in the P-type material allows electrons to move from the neighbouring N^+-source, the inversion layer can therefore respond to a high frequency gate signal and the capacitance returns to its maximum value, dashed line of Fig.3.

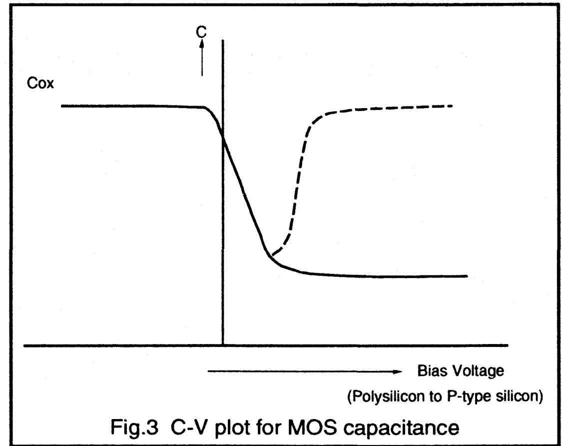


Fig.3 C-V plot for MOS capacitance

Power MOSFET capacitances

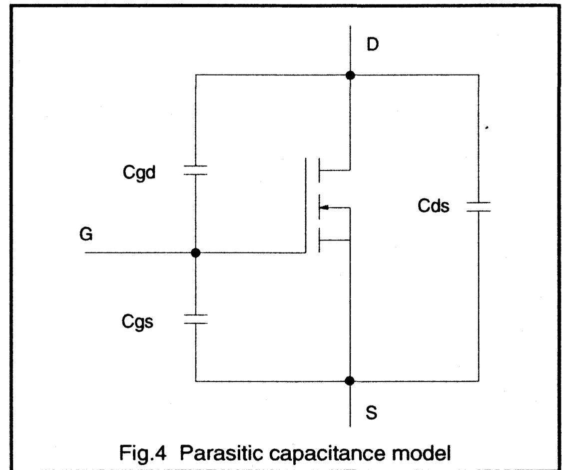


Fig.4 Parasitic capacitance model

The circuit model of Fig.4 illustrates the parasitic capacitances of the Power MOSFET. Most PowerMOS data sheets do not refer to these components but to input capacitance Ciss, output capacitance Coss and feedback capacitance Crss. The data sheet capacitances relate to the primary parasitic capacitances of Fig.4 as follows:

Ciss: Parallel combination of Cgs and Cgd
Coss: Parallel combination of Cds and Cgd
Crss: Equivalent to Cgd

Fig.5 shows the cross section of a power MOSFET cell indicating where the parasitic capacitances occur internally.

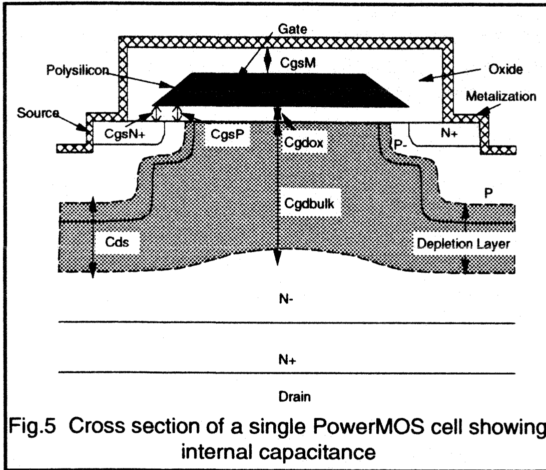


Fig.5 Cross section of a single PowerMOS cell showing internal capacitance

The capacitance between drain and source is a P-N junction capacitance, varying in accordance with the width of the depletion layer, which in turn depends on the voltage being supported by the device. The gate source capacitance consists of the three components, CgsN$^+$, CgsP and CgsM. Of these CgsP is across the oxide which will vary according to the applied gate source voltage as described above.

Of particular interest is the feedback capacitance Cgd. It is this capacitance which plays a dominant role during switching and which is also the most voltage dependent. Cgd is essentially two capacitors in series such that

$$\frac{1}{Cgd} = \frac{1}{Cgdox} + \frac{1}{Cgdbulk} \qquad 5$$

Fig.6 How Cgd is affected by voltage

Fig.6 illustrates how this capacitance is affected by the drain to gate voltage. With a large voltage drain to gate, Cgdbulk is very small due to the wide depletion region and thus maintains Cgd at a low value. As the voltage is reduced the depletion region shrinks until eventually the oxide semiconductor interface is exposed. This occurs as Vdg approaches 0 V. Cgdox now dominates Cgd. As Vdg is further reduced the drain will become negative with respect to the gate (normal on-state condition) an increasing area of the oxide-semiconductor interface is exposed and an accumulation layer forms at the semiconductor surface. The now large area of exposed oxide results in a large value for Cgdox and hence Cgd. Fig.7 shows Cgd plotted as a function of drain to gate voltage. This illustrates the almost step increase in capacitance at the point where Vgs = Vgd.

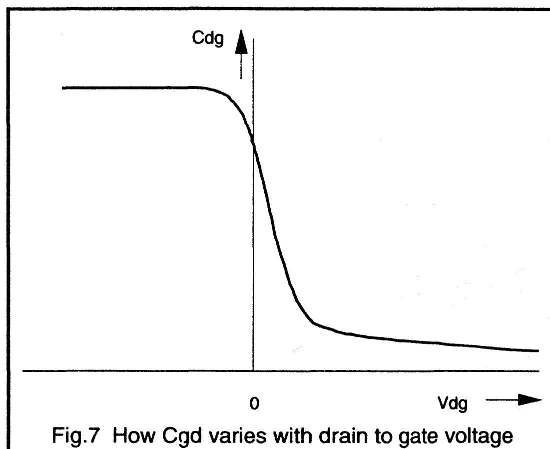


Fig.7 How Cgd varies with drain to gate voltage

Charging cycle - The Gate Charge Oscillogram

The switching cycle of a power MOSFET can be clearly observed by applying a constant current to the gate and using a constant current source as the load, Fig.8. In this circuit the MOSFET is turned on by feeding a constant current of 1 mA on to the gate, conversely the device is turned off by extracting a constant current of 1 mA from the gate. The gate and drain voltages with respect to source can be monitored on an oscilloscope as a function of time. Since Q = it, a 1 µsec period equates to 1 nc of charge applied to the gate. The gate source voltage can thus be plotted as a function of charge on the gate. Fig.9 shows such a plot for the turn-on of a BUK555-100A, also shown is the drain to source voltage. This gate voltage plot shows the characteristic shape which results from charging of the power MOSFETs input capacitance. This shape arises as follows: (NB the following analysis uses the two circuit models of Fig.10 to represent a MOSFET operating in the active region (a) and the ohmic region (b). In the active region the MOSFET is a constant current source where the current is a function of the gate-source voltage. In the ohmic region the MOSFET is in effect just a resistance.)

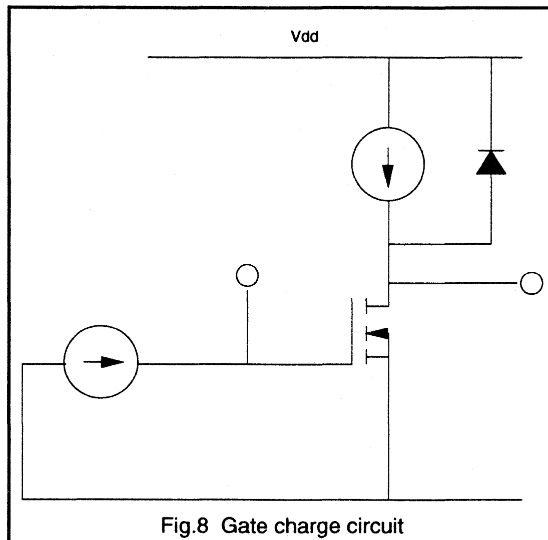


Fig.8 Gate charge circuit

At time, t0 (Fig.9), the gate drive is activated. Current flows into the gate as indicated in Fig.11(a), charging both Cgs and Cgd. After a short period the threshold voltage is reached and current begins to rise in the MOSFET. The equivalent circuit is now as shown in Fig.11(b). The drain source voltage remains at the supply level as long as id < I0 and the free wheeling diode D is conducting.

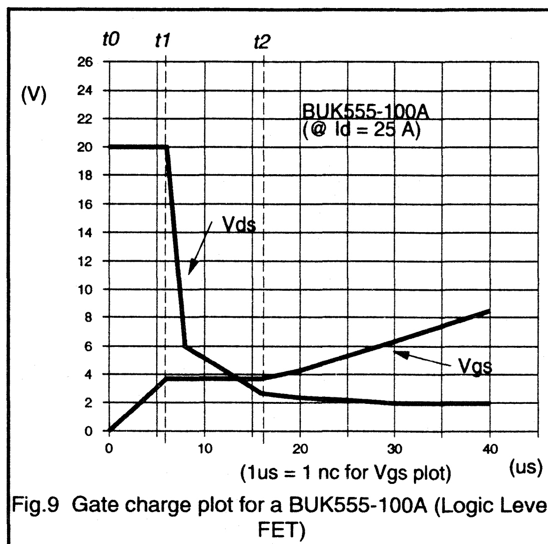


Fig.9 Gate charge plot for a BUK555-100A (Logic Level FET)

The current in the MOSFET continues to rise until id = I0, since the device is still in its active region, the gate voltage becomes clamped at this point, (t1). The entire gate current now flows through Cgd causing the drain-source voltage to drop as Cgd is discharged, Fig.11(c). The rate at which Vds falls is given by:

$$\frac{dVds}{dt} = \frac{dVdg}{dt} = \frac{ig}{Cgd} \qquad 6$$

As Vdg approaches zero, Cgd starts to increase dramatically, reaching its maximum as Vdg becomes negative. dVds/dt is now greatly reduced giving rise to the voltage tail.

Once the drain-source voltage has completed its drop to the on-state value of $I0.R_{DS(ON)}$, (point t2), the gate source voltage becomes unclamped and continues to rise, Fig.11(d). (NB dVgs/dQ in regions 1 and 3 indicates the input capacitance values.)

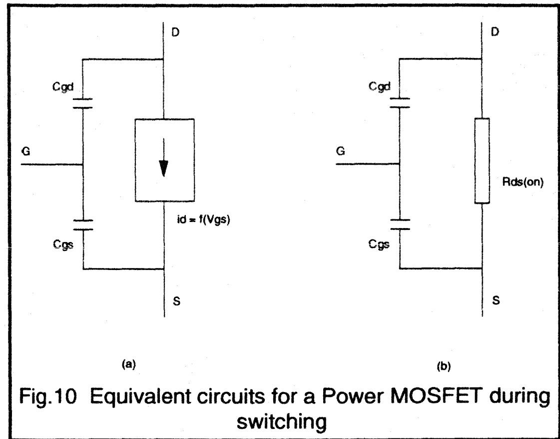


Fig.10 Equivalent circuits for a Power MOSFET during switching

Fig.11 Charging the parasitic capacitance during turn-on

The gate charge oscillogram can be found in the data for all Philips PowerMOS devices. This plot can be used to determine the required average gate drive current for a particular switching speed. The speed is set by how fast the charge is supplied to the MOSFET.

Energy consumed by the switching event

In the majority of applications the power MOSFET will be driven not from a constant current source but via a fixed gate drive impedance from a voltage source. Fig.13 shows the voltage on a voltage independent capacitor as a function of charge. The area beneath the charge vs voltage curve equals the stored energy (E = Q.V/2). The area above the charge vs voltage curve (bounded by the supply voltage) is the amount of energy dissipated during the charging cycle from a fixed voltage source. The total energy delivered by the supply is therefore Q.V, where 1/2 Q.V is stored on the capacitor to be dissipated during the discharge phase.

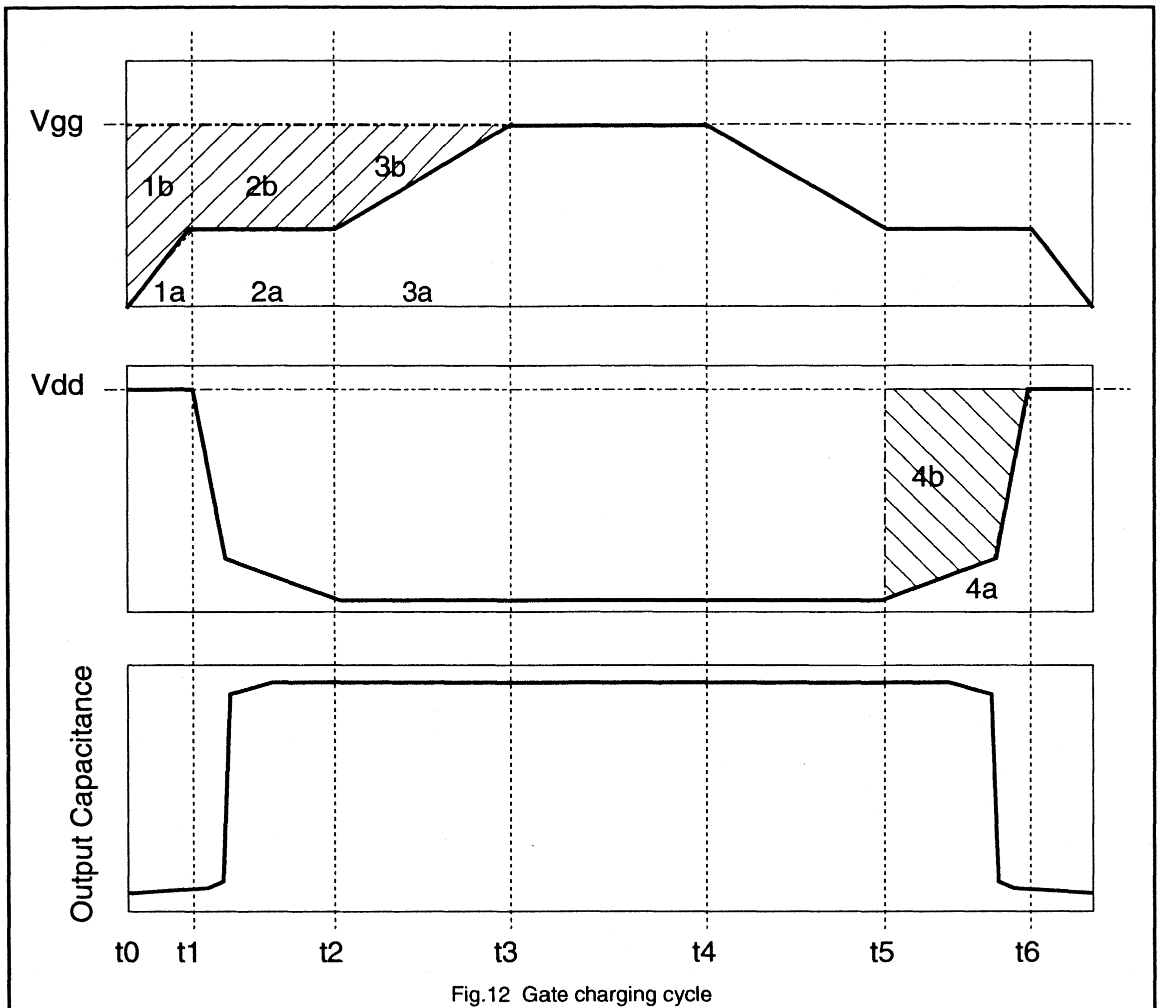


Fig.12 Gate charging cycle

Although the voltage vs charge relationship for the MOSFETs gate is not linear, energy loss is easily identified. The following discussion assumes a simple drive circuit consisting of a voltage source and drive resistance.

From t0 to t1 energy is stored in the gate capacitance which is equal to the area of region 1a. Since this charge has fallen through a voltage Vgg - Vgs(t), the area of region 1b represents the energy dissipated in the drive resistance during its delivery. Between t1 and t2 all charge enters Cgd, the area of region 2a represents the energy stored in Cgd while 2b again corresponds with the energy dissipation in the drive resistor. Finally, between t2 and t3 additional energy is stored by the input capacitance equal to the area of region 3a.

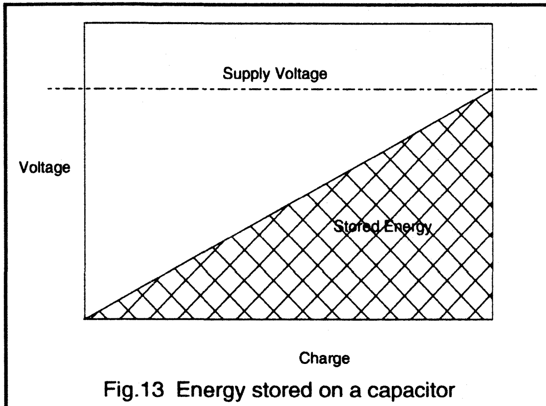


Fig.13 Energy stored on a capacitor

The total energy dissipated in the drive resistance at turn-on is therefore equal to the area 1b + 2b + 3b. The corresponding energy stored on the input capacitance is 1a + 2a + 3a, this energy will be dissipated in the drive resistance at turn-off. The total energy expended by the gate drive for the switching cycle is Q.Vgg.

As well as energy expended by the drive circuit, a switching cycle will also require energy to be expended by the drain circuit due to the charging and discharging of Cgd and Cds between the supply rail and $V_{DS(ON)}$. Moving from t5 to t6 the drain side of Cgd is charged from $Io.R_{DS(ON)}$ to Vdd. The drain circuit must therefore supply sufficient current for this charging event. The total charge requirement is given by the plateau region, Q6 - Q5. The area 4a (Fig.12) under the drain-source voltage curve represents the energy stored by the drain circuit on Cgd during turn-on. Region 4b represents the corresponding energy delivered to the load during this period. The energy consumed from the drain supply to charge and discharge Cgd over one switching cycle is thus given by:

$$W_{DD} = (Q_6 - Q_5).(V_{DD} - V_{DS(ON)}) \qquad 7$$

(The energy stored on Cgd during turn-off is dissipated internally in the MOSFET during turn-on.) Additional energy is also stored on Cds during turn-off which again is dissipated in the MOSFET at turn-on.

The energy lost by both the gate and drain supplies in the charging and discharging of the capacitances is very small over 1 cycle; Fig.9 indicates 40 nc is required to raise the gate voltage to 10 V, delivered from a 10 V supply this equates to 400 nJ; to charge Cgd to 80 V from an 80 V supply will consume 12 nc x 80 V = 1.4 µJ. Only as switching frequencies approach 1 MHz will this energy loss start to become significant. (NB these losses only apply to square wave switching, the case for resonant switching is some-what different.)

Switching performance

1) Turn-on

The parameters likely to be of most importance during the turn-on phase are,

turn-on time
turn-on loss
peak dV/dt
peak dI/dt.

Turn-on time is simply a matter of how quickly the specified charge can be applied to the gate. The average current that must be supplied over the turn-on period is

$$I_{on} = \frac{Q}{t_{on}} \qquad 8$$

For repetitive switching the average current requirement of the drive is

$$I = Q.f \qquad 9$$

where f = frequency of the input signal

Turn-on loss occurs during the initial phase when current flows in the MOSFET while the drain source voltage is still high. To minimise this loss, a necessary requirement of high frequency circuits, requires the turn-on time to be as small as possible. To achieve fast switching the drive circuit must be able to supply the initial peak current, given by equation 10.

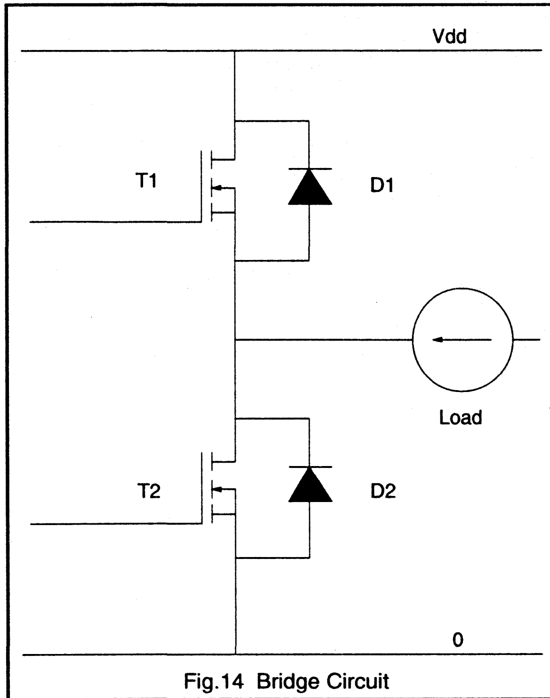


Fig.14 Bridge Circuit

$$I_{pk} = \frac{V_{GG}}{R_g} \qquad 10$$

One of the main problems associated with very fast switching MOSFETs is the high rates of change in voltage and current. High values of dV/dt can couple through parasitic capacitances to give unwanted noise on signal lines. Similarly a high dI/dt may react with circuit inductance to give problematic transients and overshoot voltages in the power circuit. dI/dt is controlled by the time taken to charge the input capacitance up to the plateau voltage, while dV/dt is governed by the rate at which the plateau region is moved through.

$$\frac{dVds}{dt} = \frac{ig}{Cgd} = \frac{V_{GG} - V_{GT}}{R_G.Cgd} \qquad 11$$

Particular care is required regarding dV/dt when switching in bridge circuits, (Fig.14). The free wheeling diode will have associated with it a reverse recovery current. When the opposing MOSFET switches on, the drain current rises beyond the load current value Io to a value Io + Irr. Consequently Vgs increases beyond Vgt(Io) to Vgt(Io + Irr) as shown in Fig.15. Once the diode has recovered there is a rapid decrease in Vgs to Vgt(Io) and this rapid decrease provides additional current to Cgd on top of that being supplied by the gate drive. This in turn causes Vdg and Vds to decrease very rapidly during this recovery period. The dV/dt in this period is determined by the recovery properties of the diode in relation to the dI/dt imposed upon it by the turn-on of the MOSFET, (reducing dI/dt will reduce this dV/dt, however it is best to use soft recovery diodes).

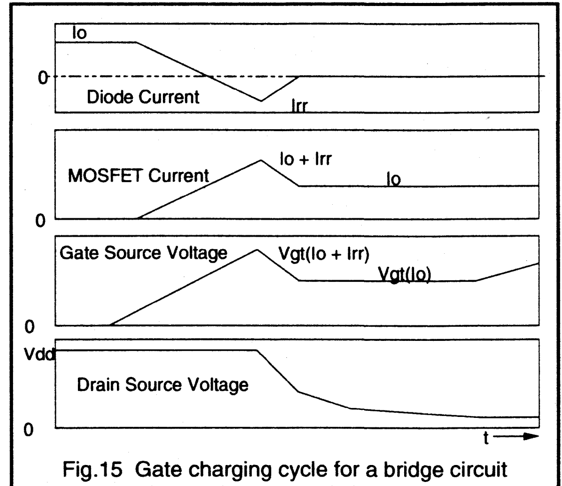


Fig.15 Gate charging cycle for a bridge circuit

ii) Turn-off

The parameters of most importance during the turn-off phase are,

turn-off time
turn-off loss
peak dVds/dt
peak dId/dt.

Turn-off of a power MOSFET is more or less the inverse of the turn-on process. The main difference is that the charging current for Cgd during turn-off must flow through both the gate circuit impedance and the load impedance. A high load impedance will thus slow down the turn-off speed.

The speed at which the plateau region is moved through determines the voltage rise time. In most applications the charging current for Cgd will be limited by the gate drive circuitry. The charging current, assuming no negative drive, is simply

$$i = \frac{Vgt}{R_G} \qquad 12$$

and the length of the plateau region will be

$$tp = \frac{Q.R_G}{Vgt} \qquad 13$$

The implications for low threshold (Logic Level) MOSFETs are clear from the above equations. The lower value of Vgt will mean a slower turn-off for a given gate impedance when compared to an equivalent standard threshold device. Equivalent switching therefore requires a lower drive impedance to be used.

Conclusions

In theory the speed of a power MOSFET is limited only by the parasitic inductances of its internal bond wires. The speed is essentially determined by how fast the internal capacitances can be charged and discharged by the drive circuit. Switching speeds quoted in data should be treated with caution since they only reflect performance for one particular drive condition. The gate charge plot is a more useful way of looking at switching capability since it indicates how much charge needs to be supplied by the drive to turn the device on. How fast that charge should be applied depends on the application and circuit performance requirements.

1.2.3 Power MOSFET Drive Circuits

MOSFETs are being increasingly used in many switching applications because of their fast switching times and low drive power requirements. The fast switching times can easily be realised by driving MOSFETs with relatively simple drive circuits. The following paragraphs outline the requirements of MOSFET drive circuits and present various circuit examples. A look at the special requirements of very fast switching circuits is also presented, this can be found in the latter part of this article.

The requirements of the drive circuit

The switching of a MOSFET involves the charging and discharging of the capacitance between the gate and source terminals. This capacitance is related to the size of the MOSFET chip used typically about 1-2 nF. A gate-source voltage of 6V is usually sufficient to turn a standard MOSFET fully on. However further increases in gate-to-source voltage are usually employed to reduce the MOSFETs on-resistance. Therefore for switching times of about 50 ns, applying a 10 V gate drive voltage to a MOSFET with a 2 nF gate-source capacitance would require the drive circuit to sink and source peak currents of about 0.5 A. However it is only necessary to carry this current during the switching intervals.

The gate drive power requirements are given in equation (1)

$$P_G = Q_G \cdot V_{GS} \cdot f \qquad 1$$

where Q_G is the peak gate charge, V_{GS} is the peak gate source voltage and f is the switching frequency.

In circuits which use a bridge configuration, the gate terminals of the MOSFETs in the circuit need to float relative to each other. The gate drive circuitry then needs to incorporate some isolation.

The impedance of the gate drive circuit should not be so large that there is a possibility of dV/dt turn on. dV/dt turn on can be caused by rapid changes of drain to source voltage. The charging current for the gate-drain capacitance C_{GD} flows through the gate drive circuit. This charging current can cause a voltage drop across the gate drive impedance large enough to turn the MOSFET on.

Non-isolated drive circuits

MOSFETs can be driven directly from a CMOS logic IC as shown in Fig.1.

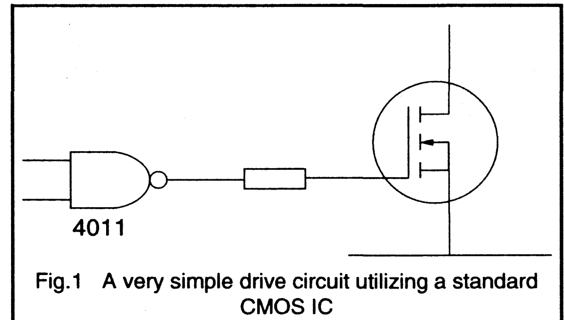


Fig.1 A very simple drive circuit utilizing a standard CMOS IC

Faster switching speeds can be achieved by parallelling CMOS hex inverting (4049) or non-inverting (4050) buffers as shown in Fig.2.

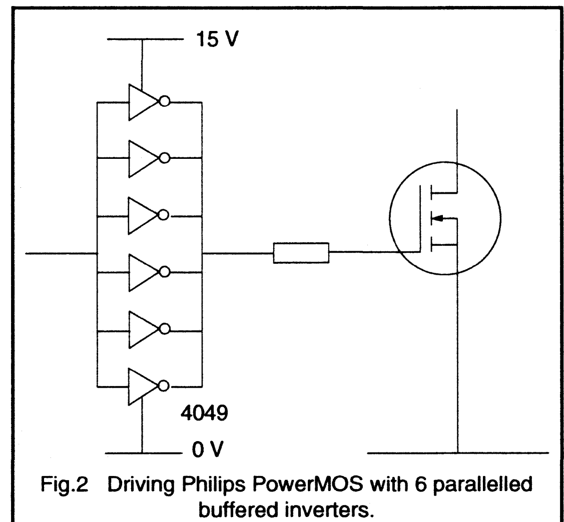


Fig.2 Driving Philips PowerMOS with 6 parallelled buffered inverters.

A push pull circuit can also be used as shown in Fig.3.

The connections between the drive circuit and the MOSFET should be kept as short as possible and twisted together if the shortest switching times are required. If both the drive circuit and the terminals of the MOSFET are on the same PCB, then the inductance of tracks, between the drive transistors and the terminals of the MOSFETs, should be kept as small as possible. This is necessary to reduce the impedance of the drive circuit in order to reduce the switching times and lessen the susceptibility of the circuit

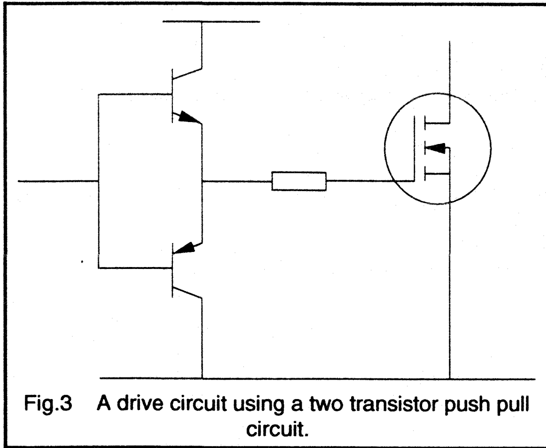


Fig.3 A drive circuit using a two transistor push pull circuit.

to dV/dt turn-on of the MOSFET. Attention to layout also improves the immunity to spurious switching by interference.

One of the advantages of MOSFETs is that their switching times can easily be controlled. For example it may be required to limit the rate of change of drain current to reduce overshoot on the drain source voltage waveform. The overshoot may be caused by switching current in parasitic lead or transformer leakage inductance. The slower switching can be achieved by increasing the value of the gate drive resistor.

The supply rails should be decoupled near to fast switching elements such as the push-pull transistors in Fig.3. An electrolytic capacitor in parallel with a ceramic capacitor are recommended since the electrolytic capacitor will not be a low enough impedance to the fast edges of the MOSFET drive pulse.

Isolated drive circuits

Some circuits demand that the gate and source terminals of MOSFETs are floating with respect to those of other MOSFETs in the circuit. Isolated drive to these MOSFETs can be provided in the following way:

(a) **Opto-isolators.**

A drive circuit using an opto-isolator is shown in Fig.4.

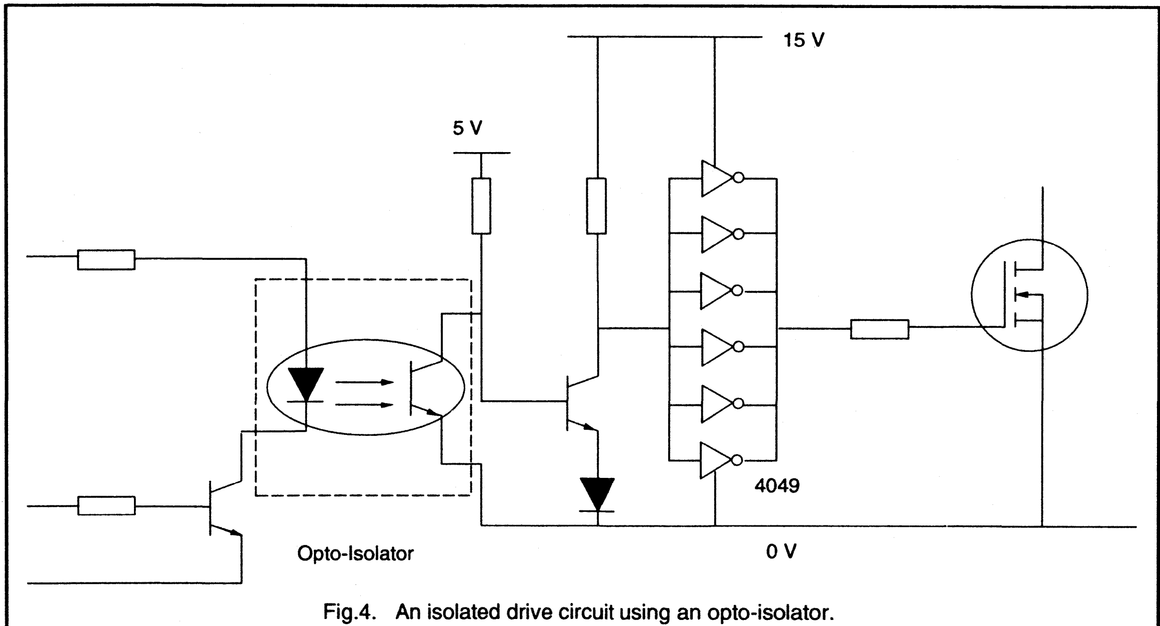


Fig.4. An isolated drive circuit using an opto-isolator.

A diode in the primary side of the opto-isolator emits photons when it is forward biased. These photons impinge on the base region of a transistor in the secondary side. This causes photogeneration of carriers sufficient to satisfy the base requirement for turn-on. In this way the opto-isolator provides isolation between the primary and secondary of the opto-isolator. An isolated supply is required for the circuitry on the secondary side of the opto-isolator. This supply can be derived, in some cases, from the drain-to-source voltage across the MOSFET being driven as shown in Fig.5. This is made possible by the low drive power requirements of MOSFETs.

Some opto-isolators incorporate an internal screen to improve the common mode transient immunity. Values as high as 1000 V/µs are quoted for common mode rejection which is equivalent to rejecting a 300V peak-to-peak sinewave.

The faster opto-isolators work off a maximum collector voltage on the secondary side of 5V so some form of level shifting may be required.

(b) **Pulse transformers.**

A circuit using a pulse transformer for isolation is shown in Fig.6(a).

When T2 switches on, voltage is applied across the primary of the pulse transformer. The current through T2 consists of the sum of the gate drive current for T1 and the magnetising current of the pulse transformer. From the waveforms of current and voltage around the circuit shown in Fig.6(b), it can be seen that after the turn off of T2 the voltage across it rises to $V_D + V_Z$, where V_Z is the voltage across the zener diode Z_D. The zener voltage V_Z applied across the pulse transformer causes the flux in the core to be reset. Thus the net volt second area across the pulse transformer is zero over a switching cycle. The minimum number of turns on the primary is given by equation (2).

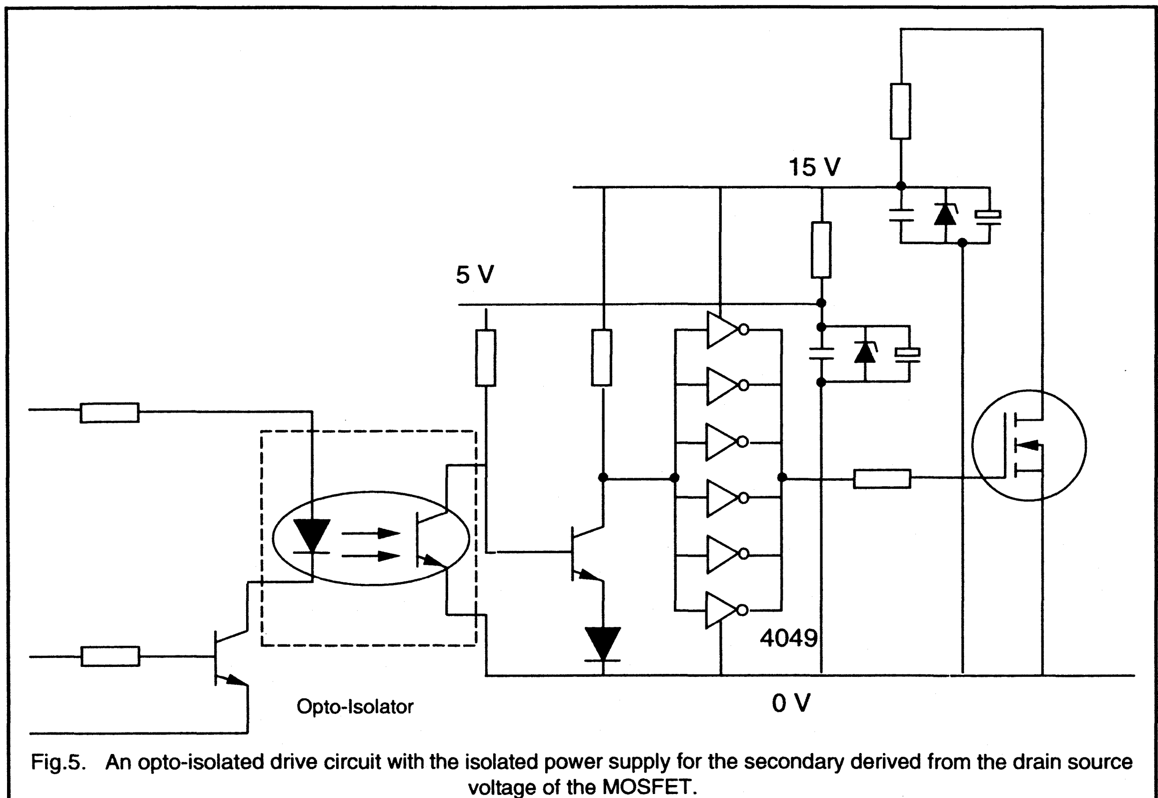


Fig.5. An opto-isolated drive circuit with the isolated power supply for the secondary derived from the drain source voltage of the MOSFET.

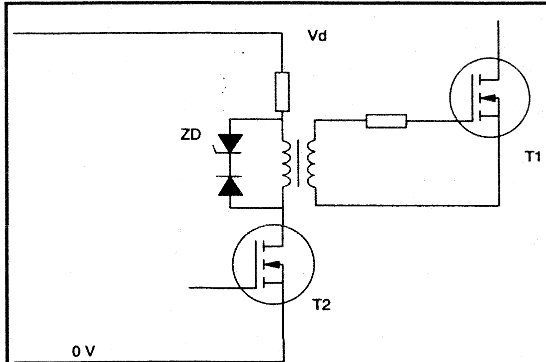


Fig.6(a) A circuit using a pulse transformer for isolation.

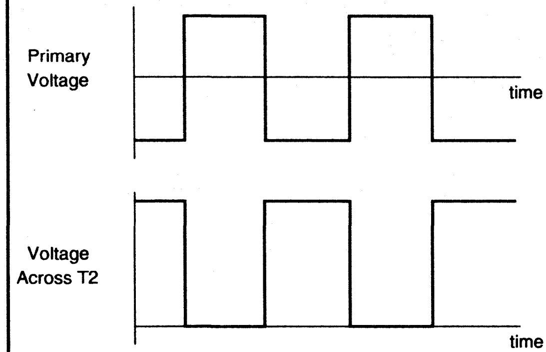


Fig.6(b) Waveforms associated with pulse transformer.

$$N = \frac{V.t}{B.A_e} \qquad 2$$

where B is the maximum flux density, A_e is the effective cross sectional area of the core and t is the time that T2 is on for.

The circuit in Fig.6(a) is best suited for fixed duty cycle operation. The zener diode has to be large enough so that the flux in the core will be reset during operation with the maximum duty cycle. For any duty cycle less than the maximum there will be a period when the voltage across the secondary is zero as shown in Fig.7.

In Fig.8 a capacitor is used to block the dc components of the drive signal.

Drive circuits using pulse transformers have problems if a widely varying duty cycle is required. This causes widely varying gate drive voltages when the MOSFET is off. In consequence there are variable switching times and varying levels of immunity to dV/dt turn on and interference. There are several possible solutions to this problem, some examples are given in Figs.9 - 12.

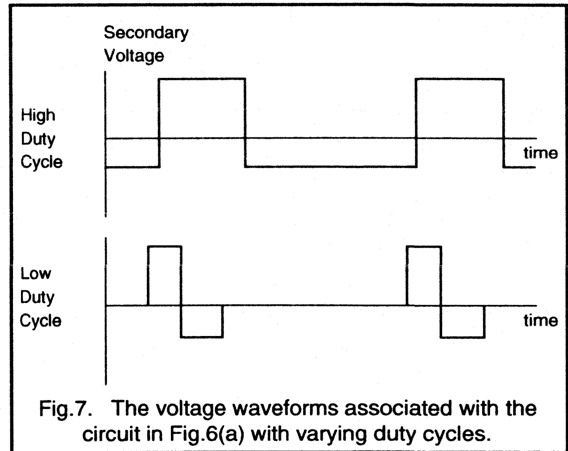


Fig.7. The voltage waveforms associated with the circuit in Fig.6(a) with varying duty cycles.

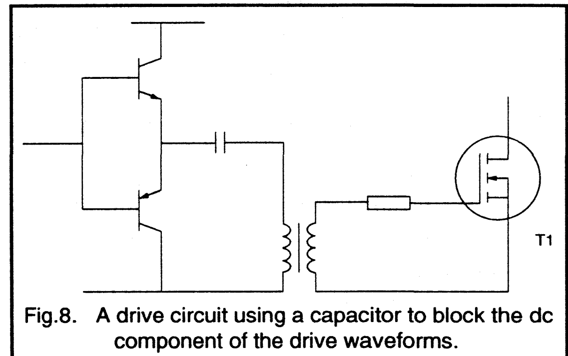


Fig.8. A drive circuit using a capacitor to block the dc component of the drive waveforms.

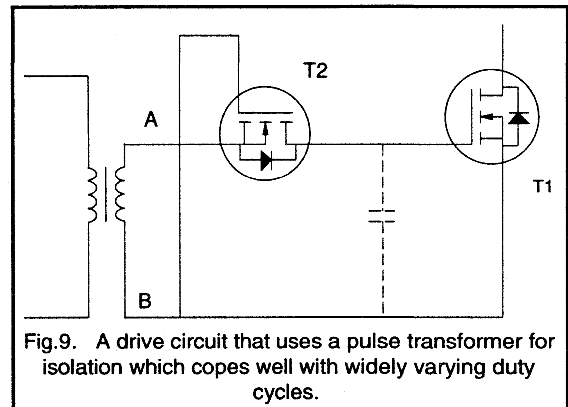


Fig.9. A drive circuit that uses a pulse transformer for isolation which copes well with widely varying duty cycles.

In the circuit shown in Fig.9 when A is positive with respect to B the input capacitance of T1 is charged through the parasitic diode of T2. The voltage across the secondary of the pulse transformer can then fall to zero and the input capacitance of T1 will remain charged. (It is sometimes necessary to raise the effective input capacitance with an external capacitor as indicated by the dashed lines.) When B becomes positive with respect to A T2 will turn on and the input capacitance of T2 will be discharged. The noise immunity of the circuit can be increased by using another MOSFET as shown in Fig.10.

In Fig.10 the potential at A relative to B has to be sufficient to charge the input capacitance of T3 and so turn T3 on before T1 can begin to turn on.

In Fig.11 the drive signal is ANDed with a hf clock. If the clock has a frequency much higher than the switching frequency of T1 then the size of the pulse transformer is reduced. The hf signal on the secondary of the pulse transformer is rectified. Q1 provides a low impedance path for discharging the input capacitance of T1 when the hf signal on the secondary of the pulse transformer is absent.

Figure 12 shows a hex non-inverting buffer connected on the secondary side, with one of the six buffers configured as a latch. The circuit operates such that the positive going edge of the drive pulse will cause the buffers to latch into the high state. Conversely the negative going edge of the

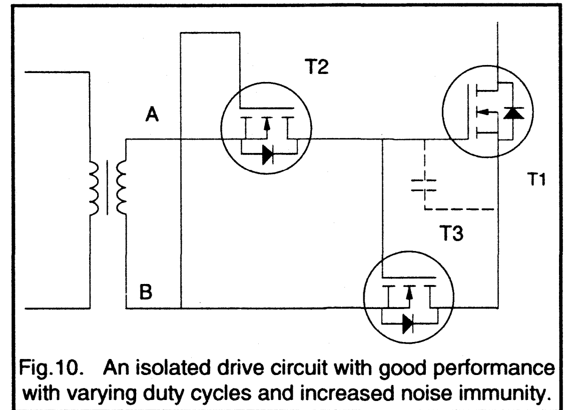


Fig.10. An isolated drive circuit with good performance with varying duty cycles and increased noise immunity.

drive pulse causes the buffers to latch into the low state. With the component values indicated on the diagram this circuit can operate with pulse on-times as low as 1 µs. The impedance Z represents either the low side switch in a bridge circuit (which can be a MOSFET configured with identical drive) or a low side load.

The impedance of the gate drive circuit may be used to control the switching times of the MOSFET. Increasing gate drive impedance however can increase the risk of dv/dt turn-on. To try and overcome this problem it may be necessary to configure the drive as outlined in Fig.13.

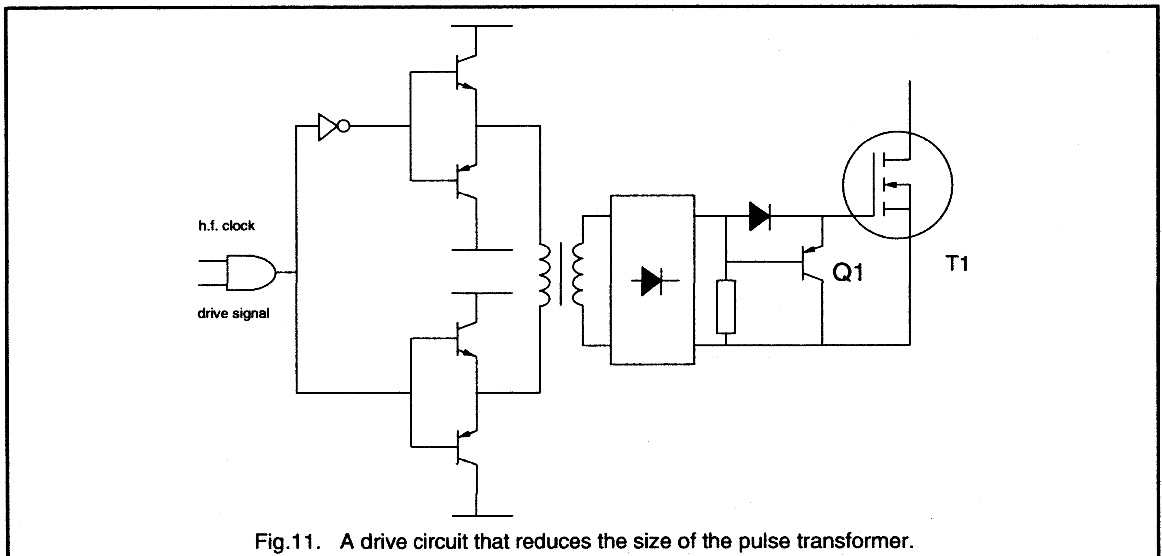


Fig.11. A drive circuit that reduces the size of the pulse transformer.

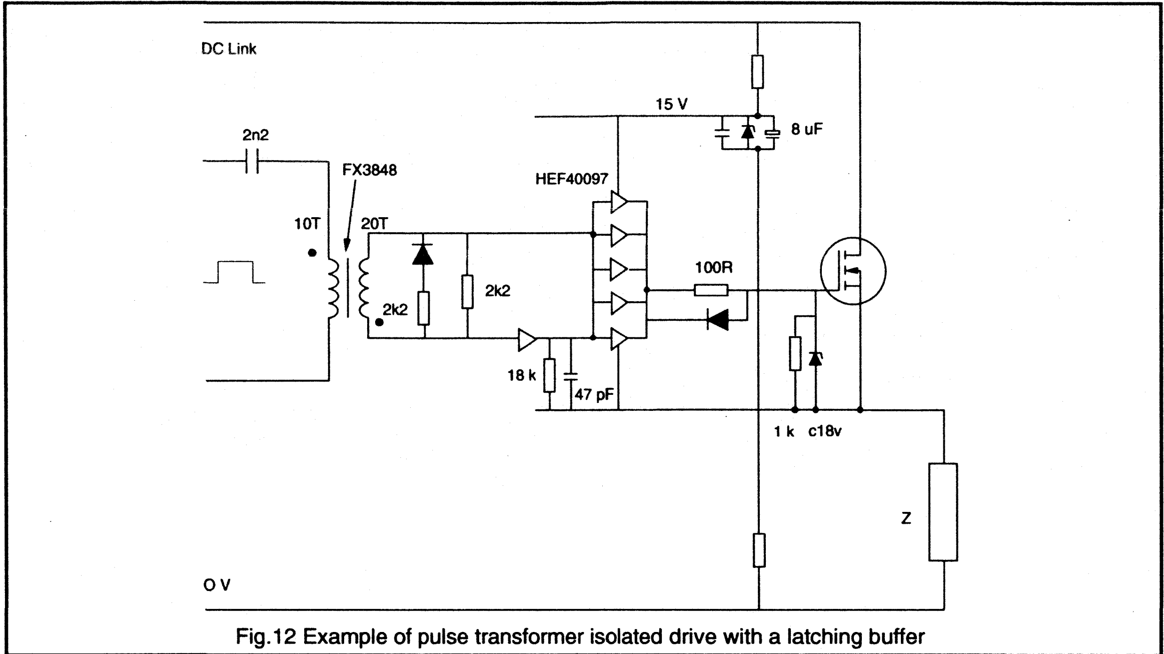


Fig.12 Example of pulse transformer isolated drive with a latching buffer

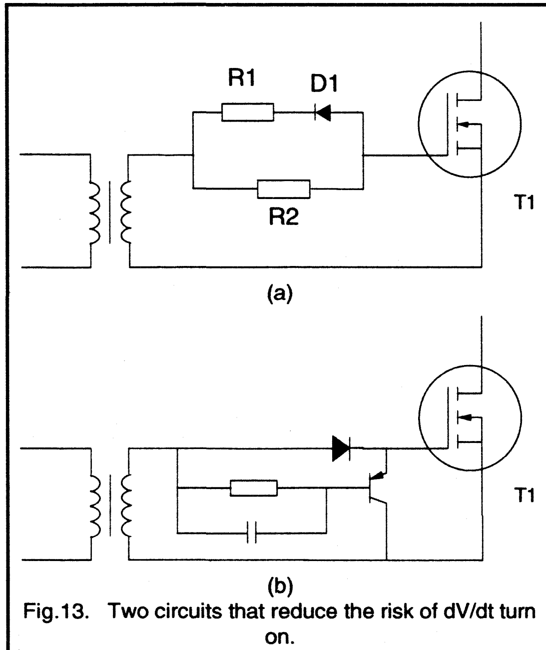


Fig.13. Two circuits that reduce the risk of dV/dt turn on.

The diode in Fig.13(a) reduces the gate drive impedance when the MOSFET is turned off. In Fig.13(b) when the drive pulse is taken away the pnp transistor is turned on. When the pnp transistor is on it short-circuits the gate to the source and so reduces the gate drive impedance.

High side drive circuits

The isolated drive circuits in the previous section can be used for either high or low side applications. Not all high side applications however require an isolated drive. Two examples showing how a high side drive can be achieved simply with a boot strap capacitor are shown in Fig.14. Both these circuits depend upon the topping up of the charge on the boot strap capacitor while the MOSFET is off. For this reason these circuits cannot be used for dc switching. The minimum operating frequency is determined by the size of the boot strap capacitor (and R1 in circuit (a)), as the operating frequency is increased so the value of the capacitor can be reduced. The circuit example in Fig. 14(a) has a minimum operating frequency of 500 Hz.

At high frequencies it may be necessary to replace R1 with the transistor T3 as shown in Fig.14(b). This enables very fast turn-off times which would be difficult to achieve with circuit (a) since reducing R1 to a low value would cause the

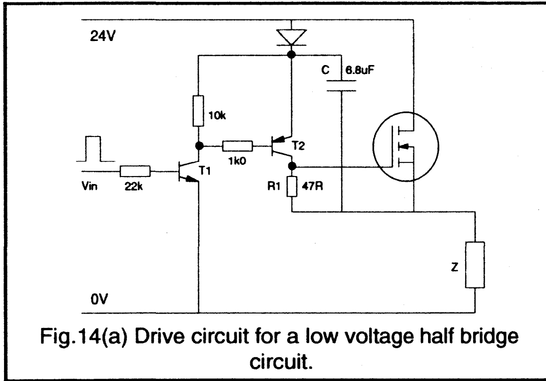


Fig.14(a) Drive circuit for a low voltage half bridge circuit.

boot strap capacitor to discharge during the on-period. The impedance Z represents either the low side switch part of the bridge or the load.

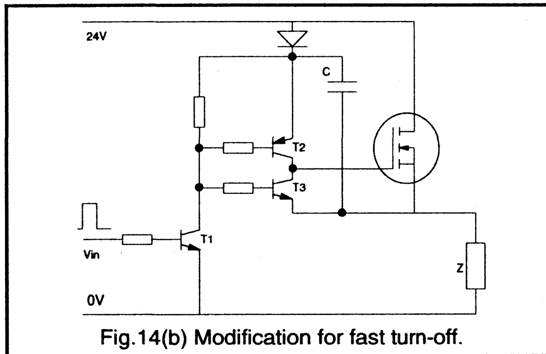


Fig.14(b) Modification for fast turn-off.

Very fast drive circuits for frequencies up to 1 MHz

The following drive circuits can charge the gate source capacitance particularly fast and so realise extremely short switching times. These fast transition times are necessary to reduce the switching losses. Switching losses are directly proportional to the switching frequency and are greater than conduction losses above a frequency of about 500 kHz, although this crossover frequency is dependent on circuit configuration. Thus for operation above 500 kHz it is important to have fast transition times.

At frequencies below 500 kHz the circuit in Fig.15 is often used. Above 500 kHz the use of the DS0026 instead of the 4049 is recommended. The DS0026 has a high current sinking and sourcing capability which is 2.5 A. It is a National Semiconductor device and is capable of charging a capacitance of 100 pF in as short a time as 25 ns.

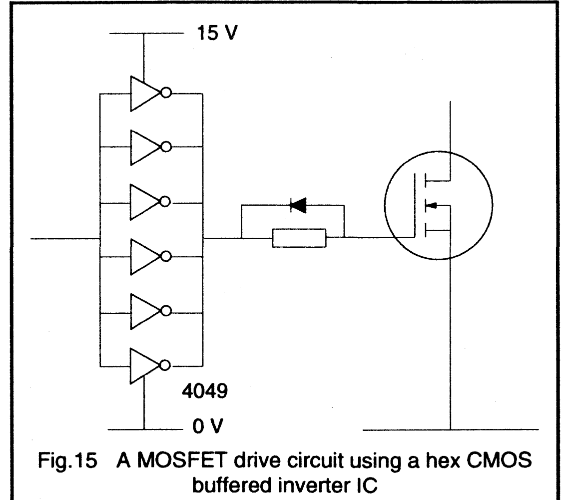


Fig.15 A MOSFET drive circuit using a hex CMOS buffered inverter IC

In Fig.16 the value of capacitor C1 is made approximately equal to the input capacitance of the driven MOSFET. Thus the RC time constant for the charging circuit is approximately halved. The disadvantage of this arrangement is that a drive voltage of 30V instead of 15V is needed because of the potential divider action of C1 and the input capacitance of the driven MOSFET. A small value of C1 would be ideal for a fast turn on time and a large value of C1 would produce a fast turn off. The circuit in Fig.17 replaces C1 by two capacitors and enables fast turn on and fast turn off.

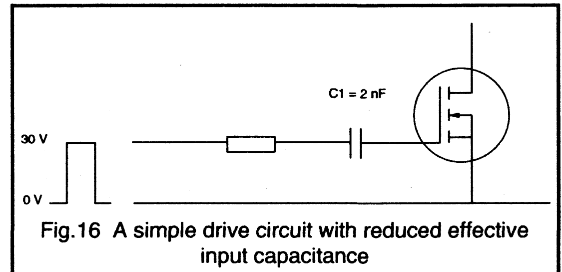


Fig.16 A simple drive circuit with reduced effective input capacitance

For the circuit in Fig.17 when MOSFET T1 is turned on the driven MOSFET T3 is driven initially by a voltage V_{DD} feeding three capacitors in series, namely C1, C2 and the input capacitance of T3. Since the capacitors are in series their equivalent capacitance will be low and so the RC time constant of the charging circuit will be low. C1 is made low to make the turn on time very fast.

The voltage across C2 will then settle down to $(V_{DD} - V_{ZD1})$ R2/(R1 + R2). Therefore the inclusion of resistors R1 and R2 means that C2 can be made larger than C1 and still have a large voltage across it before the

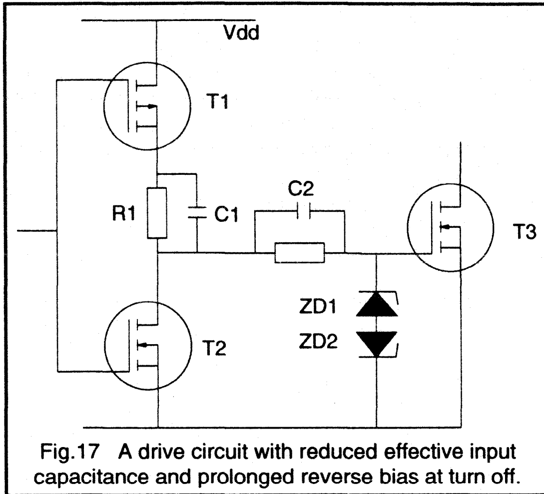


Fig.17 A drive circuit with reduced effective input capacitance and prolonged reverse bias at turn off.

turn off of T3. Thus C2 can sustain a reverse voltage across the gate source of T3 for the whole of the turn off time. The initial discharging current will be given by Equation 3,

$$I = \frac{V_{ZDI} + \frac{R_2 \cdot (V_{DD} - V_{ZDI})}{(R_1 + R_2)}}{R_{STRAY} + R_{DS(ON)T2}} \quad 3$$

Making V_{DD} large will make turn on and turn off times very small.

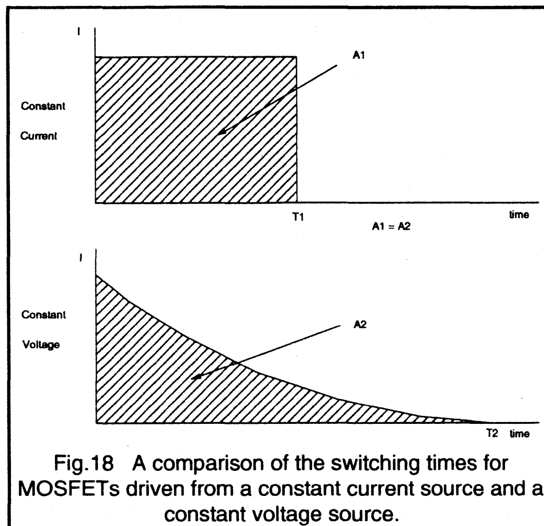


Fig.18 A comparison of the switching times for MOSFETs driven from a constant current source and a constant voltage source.

Fast switching speeds can be achieved with the push pull circuit of Fig.19. A further improvement can be made by replacing the bipolar devices by MOSFETs as shown in Fig.20. The positions of the P and N channel MOSFETs may be interchanged and connected in the alternative arrangement of Fig.21. However it is likely that one MOSFET will turn on faster than the other turns off and so the circuit in Fig.21 may cause a current spike during the switching interval. The peak to average current rating of MOSFETs is excellent so this current spike is not usually a problem. In the circuit of Fig.20 the input capacitance of the driven MOSFET is charged up to V_{DD} - V_T, where V_T is the threshold voltage, at which point the MOSFET T1 turns off. Therefore when T2 turns on there is no current spike.

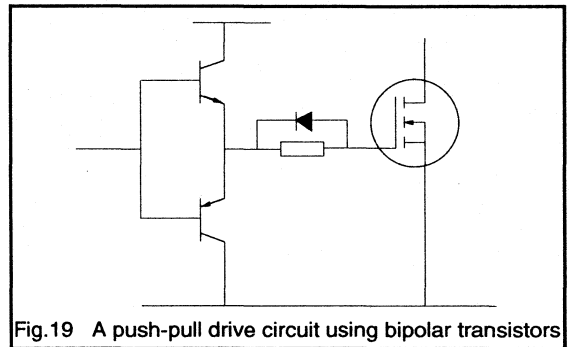


Fig.19 A push-pull drive circuit using bipolar transistors

There may well be some advantages in charging the input capacitance of the MOSFET from a constant current source rather than a constant voltage source. For a given drain source voltage a fixed amount of charge has to be transferred to the input capacitance of a MOSFET to turn it on. As illustrated in Fig.18 this charge can be transferred more quickly with a constant current of magnitude equal to the peak current from a constant voltage source.

A few other points are worthy of note when discussing very fast drive circuits.

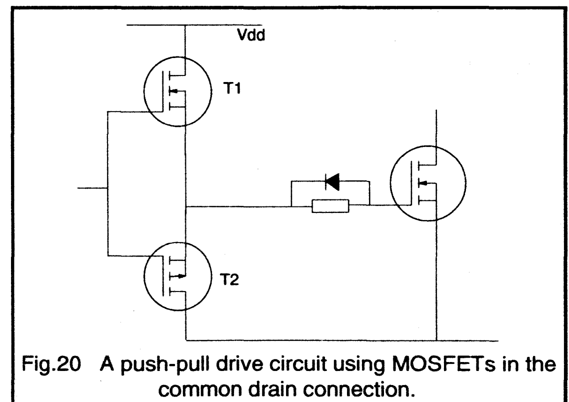


Fig.20 A push-pull drive circuit using MOSFETs in the common drain connection.

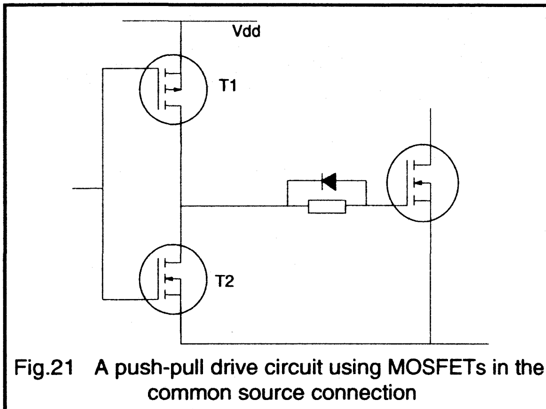


Fig.21 A push-pull drive circuit using MOSFETs in the common source connection

(1) SMPS working in the 1 - 15 MHz range sometimes use resonant drive circuits. These SMPS are typically QRC (Quasi Resonant Circuits). The resonant drive circuits do not achieve faster switching by the fact that they are resonant. But by being resonant, they recoup some of the drive energy and reduce the gate drive power. There are two main types of QRC - zero voltage and zero current switching circuits. In one of these types, fall times are not critical and in the other, rise times are not critical. On the critical switching edge, a normal, fast switching edge is provided by using a circuit similar to those given above. For the non-critical edge there is a resonant transfer of energy. Thus drive losses of $Q_G.V_{GS}.f$ become $0.5.Q_G.V_{GS}.f$.

(2) It is usual to provide overdrive of the gate source voltage. This means charging the input capacitance to a voltage which is more than sufficient to turn the MOSFET fully on. This has advantages in achieving lower on-resistance and increasing noise immunity. The gate power requirements are however increased when overdrive is applied. It may well be a good idea therefore to drive the gate with only 12 V say instead of 15 V.

(3) It is recommended that a zener diode be connected across the gate source terminals of a MOSFET to protect against over voltage. This zener can have a capacitance which is not insignificant compared to the input capacitance of small MOSFETs. The zener can thus affect switching times.

Parallel operation

Power MOSFETs lend themselves readily to operation in parallel since their positive temperature coefficient of resistance opposes thermal runaway. Since MOSFETs have low gate drive power requirements it is not normally necessary to increase the rating of drive circuit components if more MOSFETs are connected in parallel. It is however recommended that differential resistors are used in the drive circuits as shown in Fig.22.

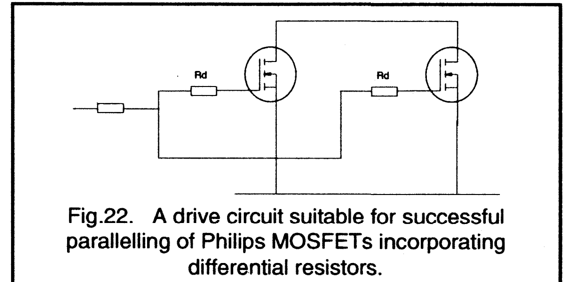


Fig.22. A drive circuit suitable for successful parallelling of Philips MOSFETs incorporating differential resistors.

These differential resistors (R_D) damp down possible oscillations between reactive components in the device and in connections around the MOSFETs, with the MOSFETs themselves, which have a high gain even up to 200 MHz.

Protection against gate-source overvoltages

It is recommended that zener diodes are connected across the gate-source terminals of the MOSFET to protect against voltage spikes. One zener diode or two back-to-back zener diodes are necessary dependent on whether the gate-source is unipolar or bipolar, as shown in Fig.23.

The zener diodes should be connected close to the terminals of the MOSFET to reduce the inductance of the connecting leads. If the inductance of the connecting leads is too large it can support sufficient voltage to cause an overvoltage across the gate-source oxide.

In conclusion the low drive power requirement of Philips PowerMOS make provision of gate drive circuitry a relatively straightforward process as long as the few guide-lines outlined in this note are heeded.

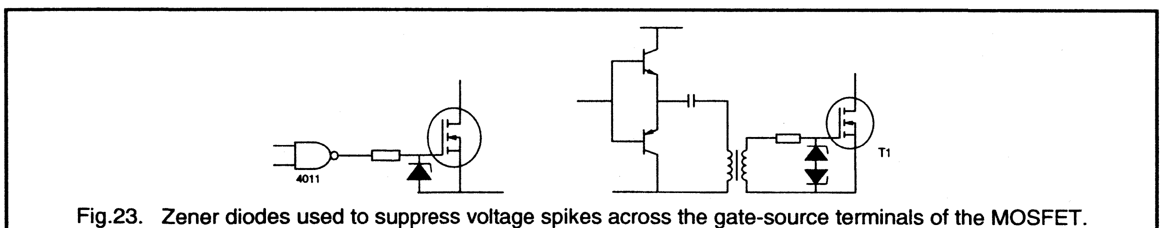


Fig.23. Zener diodes used to suppress voltage spikes across the gate-source terminals of the MOSFET.

1.2.4 Parallel Operation of Power MOSFETs

This section is intended as a guide to the successful parallelling of Power MOSFETs in switching circuits.

Advantages of operating devices in parallel

Increased power handling capability

If power requirements exceed those of available devices then increased power levels can be achieved by parallelling devices. The alternative means of meeting the power requirements would be to increase the area of die. The processing of the larger die would have a lower yield and so the relative cost of the die would be increased. The larger die may also require a more expensive package.

Standardisation

Parallelling devices can mean that only one package, say the TO220 package, needs to be used. This can result in reduced production costs.

Increased operating frequency

Packages are commercially available which contain upto five die connected in parallel. The switching capabilities of these packages are typically greater than 10 kVA. The parasitic inductances of connections to the parallelled dies are different for each die. This means that the current rating of the package has to be derated at high frequencies to allow for unequal current sharing. The voltage rating of the multiple die package has to be derated for higher switching speeds. This is because the relatively large inductances of connections within the package sustain appreciable voltages during the switching intervals. This means that the voltages at the drain connections to the dice will be appreciably greater than voltages at the terminals of the package. By parallelling discrete devices these problems can be overcome.

Faster switching speeds are achieved using parallelled devices than using a multiple die package. This is because switching times are adversely affected by the impedance of the gate drive circuit. When devices are parallelled these impedances are parallelled and so their effect is reduced. Hence faster switching times and so reduced switching losses can be achieved.

Faster switching speeds improve parallelling. During switching intervals one MOSFET may carry more current than other MOSFETs in parallel with it. This is caused by differences in electrical parameters between the parallelled MOSFETs themselves or between their drive circuits. The increased power dissipation in the MOSFET which carries more current will be minimised if switching speeds are increased. The inevitable inductance in the source connection, caused by leads within the package, causes a negative feedback effect during switching. If the rate of rise of current in one parallelled MOSFET is greater than in the others then the voltage drop across inductances in its drain and source terminals will be greater. This will oppose the build up of current in this MOSFET and so have a balancing effect. This balancing effect will be greater if switching speeds are faster. This negative feedback effect reduces the deleterious effect of unequal impedances of drive circuit connections to parallelled MOSFETs. The faster the switching speeds then the greater will be the balancing effect of the negative feedback. Parallelling devices enables higher operating frequencies to be achieved than using multiple die packages. The faster switching speeds possible by parallelling at the device level promote better current sharing during switching intervals.

Increased power dissipation capability

If two devices, each rated for half the total required current, are parallelled then the sum of their individual power dissipation capabilities will be more than the possible power dissipation in a single device rated for the total required current. This is especially useful for circuits operating above 100 kHz where switching losses predominate.

Advantages of power MOSFETs for parallel operation

Reduced likelihood of thermal runaway

If one of the parallelled devices carries more current then the power dissipation in this device will be greater and its junction temperature will increase. The temperature coefficient of $R_{DS(ON)}$ for Power MOSFETs is positive as shown in Fig.1. Therefore there will be rise in $R_{DS(ON)}$ for the device carrying more current. This mechanism will oppose thermal runaway in parallelled devices and also in parallelled cells in the device.

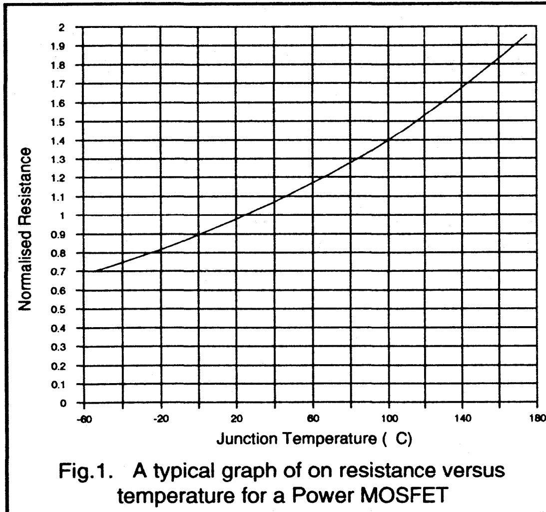


Fig.1. A typical graph of on resistance versus temperature for a Power MOSFET

Low Drive Power Requirements

The low drive power requirements of power MOSFETs mean that many devices can be driven from the same gate drive that would be used for one MOSFET.

Very good tolerance of dynamic unbalance

The peak to average current carrying capability of power MOSFETs is very good. A device rated at 8A continuous drain current can typically withstand a peak current of about 30A. Therefore, for the case of three 8A devices in parallel, if one of the devices switches on slightly before the others no damage will result since it will be able to carry the full load current for a short time.

Design points

Derating

Since there is a spread in on-resistance between devices from different batches it is necessary to derate the continuous current rating of parallelled devices by about 20%.

Layout

There are two aspects to successful parallelling which are static and dynamic balance. Static balance refers to equal sharing of current between parallelled devices when they have been turned on. Dynamic balance means equal sharing of current between parallelled transistors during switching intervals.

Unsymmetrical layout of the circuit causes static imbalance. If the connections between individual MOSFETs and the rest of the power circuit have different impedances then there will be static imbalance. The connections need to be kept as short as possible to keep their inductance as small as possible. Symmetrical layout is particularly important in resonant circuits where MOSFETs carry a sinusoidal current e.g. in a voltage fed inverter feeding a series resonant circuit. In a current fed inverter, where switching in the inversion stage causes a rectangular wave of current to be passed through a parallel resonant tank circuit, the voltage sustained by MOSFETs when they are off will be half sinusoid. A component of the current carried by MOSFETs will be a charging current for snubber capacitors which will be sinusoidal so again symmetrical layout will be important.

Unsymmetrical layout of the gate drive circuitry causes dynamic imbalance. Connections between the gate drive circuitry and the MOSFETs need to be kept short and twisted together to reduce their inductance. Further to this the connections between the gate drive circuit and parallelled MOSFETs need to be approximately the same length.

Figures 2 and 3 illustrate the effect of unsymmetrical layout on the current sharing of two parallelled MOSFETs. The presence of 50 nH in the source connection of one of the two parallelled BUK453-50A MOSFETs causes noticeable imbalance. A square shaped loop of 1 mm diameter wire and side dimension only 25 mm is sufficient to produce an inductance of 50 nH.

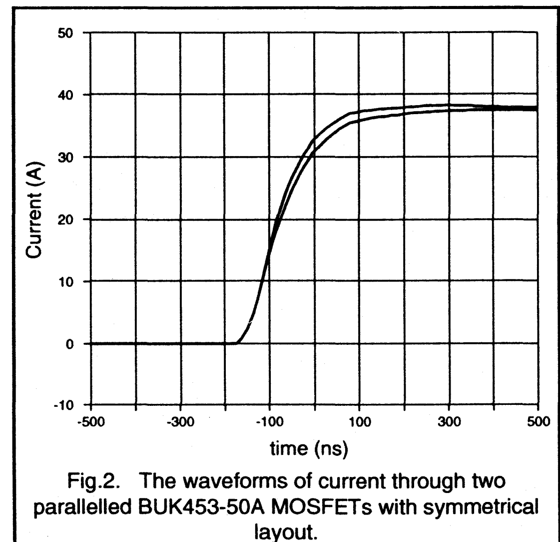


Fig.2. The waveforms of current through two parallelled BUK453-50A MOSFETs with symmetrical layout.

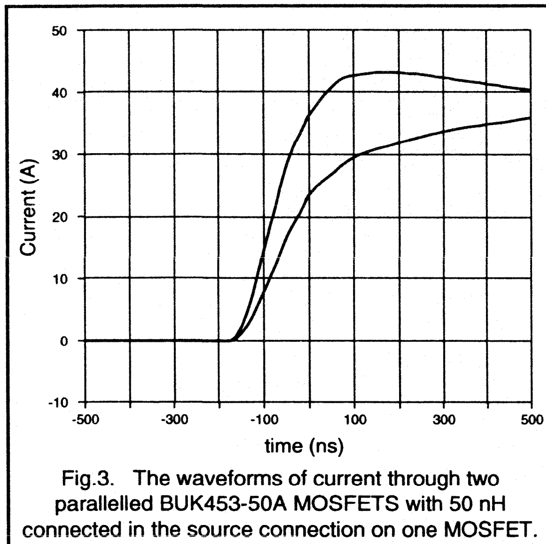


Fig.3. The waveforms of current through two parallelled BUK453-50A MOSFETS with 50 nH connected in the source connection on one MOSFET.

Symmetrical layout becomes more important if more MOSFETs are parallelled, e.g. if a MOSFET with an $R_{DS(ON)}$ of 0.7 Ohm was connected in parallel with a MOSFET with an $R_{DS(ON)}$ of 1 Ohm then the MOSFET with the lower $R_{DS(ON)}$ would carry 25% more current that if both MOSFETs had an $R_{DS(ON)}$ of 1 ohm. If the MOSFET with an $R_{DS(ON)}$ of 0.7 ohm was connected in parallel with a hundred MOSFETs with $R_{DS(ON)}$ of 1 ohm it would carry 50% more current than if all the MOSFETs had an $R_{DS(ON)}$ 1 Ohm.

Good Thermal Coupling

There should be good thermal coupling between parallelled MOSFETs. This is achieved by mounting parallelled MOSFETs on the same heatsink or on separate heatsinks which are in good thermal contact with each other.

If poor thermal coupling existed between parallelled MOSFETs and the positive temperature coefficient of resistance was relied on to promote static balance, then the total current carried by the MOSFETs would be less than with good thermal coupling. Some MOSFETs would also have relatively high junction temperatures and so their reliability would be reduced. The temperature coefficient of MOSFETs is not large enough to make poor thermal coupling tolerable.

The Suppression of Parasitic Oscillations

Parasitic oscillations can occur. MOSFETs have transition frequencies typically in excess of 200 MHz and parasitic reactances are present both in the MOSFET package and circuit connections, so the necessary feedback conditions for parasitic oscillations exist. These oscillations typically occur at frequencies above 100 MHz so a high bandwidth oscilloscope is necessary to investigate them. The likelihood of these parasitic oscillations occurring is very much reduced if small differential resistors are connected in the leads to each parallelled MOSFET. A common gate source drive resistor of between 10 and 100 Ohms with differential resistors of about 10 Ohm are recommended as shown in Fig.4.

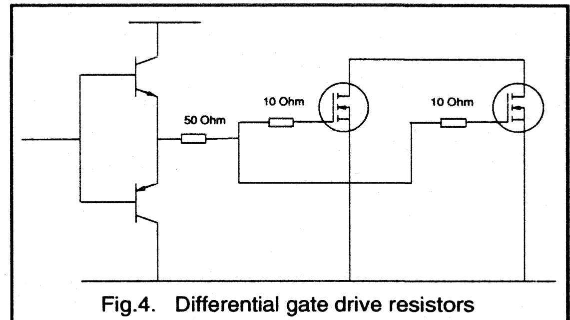


Fig.4. Differential gate drive resistors

The suppression of parasitic oscillations between parallelled MOSFETs can also be aided by passing the connections from the gate drive circuit through ferrite beads. The effect of these beads below 1 MHz is negligible. The ferrite beads however damp the parasitic oscillations which occur at frequencies typically above 100 MHz. An example of parasitic oscillations is shown in Fig.5.

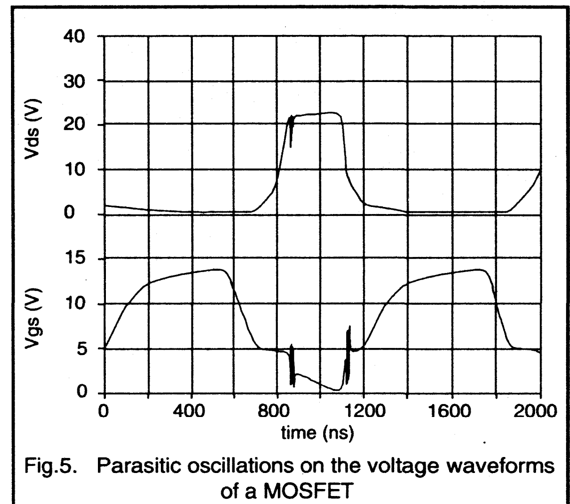


Fig.5. Parasitic oscillations on the voltage waveforms of a MOSFET

If separate drive circuits with closely decoupled power supplies are used for each parallelled device then parasitic oscillations will be prevented. This condition could be satisfied by driving each parallelled MOSFET from 3 buffers in a CMOS Hex buffer ic.

To take this one stage further, separate push pull transistor drivers could be used for each MOSFET. (A separate base resistor is needed for each push-pull driver to avoid a MOSFET with a low threshold voltage clamping the drive voltage to all the push pull drivers). This arrangement also has the advantage that the drive circuits can be positioned very close to the terminals of each MOSFET. The impedance of connections from the drive circuits to the MOSFETs will be minimised and so there will be a reduced likelihood of spurious turn on. Spurious turn on can occur when there is a fast change in the drain to source voltage. The charging current for the gate drain capacitance inherent in the MOSFET structure can cause a voltage drop across the gate drive impedance large enough to turn the MOSFET on. The gate drive impedance needs to be kept as low as possible to reduce the likelihood of spurious turn on.

Resonant power supplies

If a resonant circuit is used then there will be reduced interference and switching losses. The reduced interference is achieved because sinusoidal waveforms are present in resonant circuits rather than rectangular waveforms. Rectangular waveforms have large high frequency harmonic components.

MOSFETs are able to switch at a zero crossing of either the voltage or the current waveform and so switching losses are ideally zero. For example, in the case of a current fed inverter feeding a parallel resonant load switching can take place at a zero crossing of voltage so switching losses are negligible. In this case the sinusoidal drain source voltage sustained by MOSFETs reduces the likelihood of spurious dv/dt turn on. This is because the peak charging current for the internal gate to drain capacitance of the MOSFET is reduced.

The current fed approach

Switch mode power supplies using the current fed topology have a d.c. link which contains a choke to smooth the current in the link. Thus a high impedance supply is presented to the inversion stage. Switching in the inversion stage causes a rectangular wave of current to be passed through the load. The current fed approach has many advantages for switch mode power supplies. It causes reduced stress on devices caused by the slow reverse recovery time of the parasitic diode inherent in the structure of MOSFETs.

The current fed approach can also reduce problems caused by dynamic imbalance. If more than three MOSFETs are parallelled then it is advantageous to use more than one choke in the d.c. link rather than wind a single choke out of thicker gauge wire. One of the connections to each choke is connected to the output of the rectification stage. The other connection of each choke is connected to a group of three MOSFETs. This means that if one MOSFET switches on before the others it will carry a current less than its peak pulse value even when many MOSFETs are parallelled.

The parallel operation of MOSFETs in the linear mode

The problems of parallelling MOSFETs which are being used in the linear mode are listed below.

(a) The parallelled devices have different threshold voltages and transconductances. This leads to poor sharing.

(b) MOSFETs have a positive temperature coefficient of gain at low values of gate to source voltage. This can lead to thermal runaway.

The imbalance caused by differences in threshold voltage and transconductance can be reduced by connecting resistors (R_S) in the source connections. These resistors are in the gate drive circuit and so provide negative feedback. The negative feedback reduces the effect of different values of VT and g_m. The effective transconductance gm of the MOSFET is given in Equation 1.

$$g_m = \frac{1}{R_s + \frac{1}{g_m}} \qquad 1$$

R_S must be large compared to $1/g_m$ to reduce the effects of differences in g_m. Values of $1/g_m$ typically vary between 0.1 and 1.0 Ohm. Therefore values of R_S between 1 ohm and 10 ohm are recommended.

Differential heating usually has a detrimental effect on sharing and so good thermal coupling is advisable.

Conclusions

Power MOSFETs can successfully be parallelled to realise higher power handling capability if a few guidelines are followed.

1.2.5 Series Operation of Power MOSFETs

The need for high voltage switches can be well illustrated by considering the following examples. In flyback converters the leakage inductance of an isolating transformer can cause a large voltage spike across the switch when it switches off. If high voltage MOSFETs are used the snubber components can be reduced in size and in some cases dispensed with altogether.

For industrial equipment operation from a supply of 415 V, 550 V or 660 V is required. Rectification of these supply voltages produces d.c. rails of approximately 550 V, 700 V and 800 V. The need for high voltage switches in these cases is clear.

Resonant topologies are being increasingly used in switching circuits. These circuits have advantages of reduced RFI and reduced switching losses. To reduce the size of magnetic components and capacitors the switching frequency of power supplies is increased. RFI and switching losses become more important at high frequencies so resonant topologies are more attractive. Resonant circuits have the disadvantage that the ratio of peak to average voltage can be large. For example a Parallel Resonant Power Supply for a microwave oven operating off a 240 V supply can be most easily designed using a switch with a voltage rating of over 1000 V.

In high frequency induction heating power supplies capacitors are used to resonate the heating coil. The use of high voltage switches in the inversion bridge can result in better utilisation of the kVAr capability of these capacitors. This is advantageous since capacitors rated at tens of kVAr above 100 kHz are very expensive.

In most TV deflection and monitor circuits peak voltages of up to 1300 V have to be sustained by the switch during the flyback period. This high voltage is necessary to reset the current in the horizontal deflection coil. If the EHT flashes over, the switch will have to sustain a higher voltage so 1500 V devices are typically required.

The Philips range of PowerMOS includes devices rated at voltages up to 1000 V to cater for these requirements. However in circuits, particularly in resonant applications where voltages higher than this are required, it may be necessary to operate devices in series.

Series operation can be attractive for the following reasons:

Firstly, the voltage rating of a PowerMOS transistor cannot be exceeded. A limited amount of energy can be absorbed by a device specified with a ruggedness rating (eg device can survive some overvoltage transients), but a 1000 V device cannot block voltages in excess of 1000 V.

Secondly, series operation allows flexibility as regards on-resistance and so conduction losses.

The following are problems that have to be overcome for successful operation of MOSFETs in series. If one device turns off before another it may be asked to block a voltage greater than its breakdown voltage. This will cause a reduction in the lifetime of the MOSFET. Also there is a requirement for twice as many isolated gate drive circuits in many circuits.

The low drive power requirements of Philips PowerMOS mean that the provision of more isolated gate drive circuits is made easier. Resonant circuits can have advantages in reducing the problems encountered if one MOSFET turns off before another. The current fed full bridge inverter is one such circuit.

To illustrate how devices can be operated in series, a current fed full bridge inverter is described where the peak voltage requirement is greater than 1200 V.

The current fed inverter

A circuit diagram of the full bridge current fed inverter is shown in Fig.1. A choke in the d.c. link smooths the link current. Switching in the inversion bridge causes a rectangular wave of current to be passed through the load. The load is a parallel resonant tank circuit. Since the Q of the tank circuit is relatively high the voltage across the load is a sinewave. MOSFETs sustain a half sinusoid of voltage when they are off. Thus series operation of MOSFETs is made easier because if one MOSFET turns off before another it only has to sustain a small voltage. To achieve the best sharing, the gate drive to MOSFETs connected in series should be as similar as possible. In particular the zero crossings should be synchronised. The MOSFET drive circuit shown in Fig.2 has been found to be excellent in this respect. For current fed resonant circuits in which the duty cycle varies over large ranges the circuit in Fig.3 will perform well. A short pulse applied to the primary of the pulse transformer is sufficient to turn MOSFET M4 on. This short pulse can be achieved by designing the pulse transformer so that it saturates during the time that M1 is on. The gate source capacitance of M4 will remain charged until M2 is turned on. M3 will then be turned on and the gate source capacitance of M4 will be discharged and so

Fig.1. Circuit diagram of the full bridge current-fed inverter feeding a parallel resonant load.

M4 is turned off. Thus this circuit overcomes problems of resetting the flux in the core of the pulse transformer for large duty cycles.

Each leg of the inverter consists of two MOSFETs, type BUK456-800B, connected in series. The ideal rating of the two switches in each leg is therefore 1600 V and 3.5 A. The inverter is fed into a parallel resonant circuit with values of L = 120 µH (Q = 24 at 150 kHz) and C = 2.2 nF.

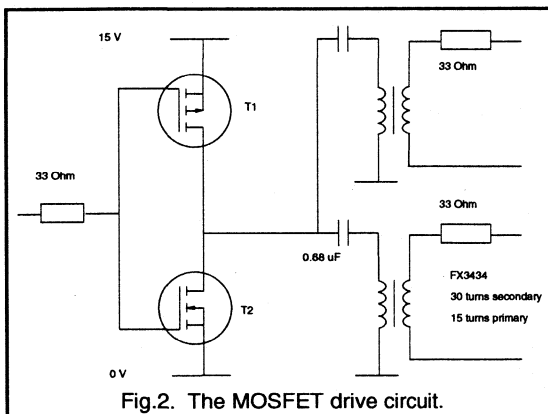


Fig.2. The MOSFET drive circuit.

Capacitors are shown connected across the drain source terminals of MOSFETs. The value of the capacitor across the drain to source of each MOSFET is 6.6 nF. (Six 10 nF polypropylene capacitors, type 2222 376 92103.) This gives a peak voltage rating of about 850 V at 150 kHz for the capacitor combination across each MOSFET. (This voltage rating takes into account that the capacitors will only have to sustain voltage when the MOSFET is off). The function of these capacitors is twofold. Firstly they suppress spikes caused by switching off current in parasitic lead inductance. Secondly they improve the sharing of voltage between the MOSFETs connected in series. These capacitors are effectively in parallel with the tank circuit capacitor. However only half of the capacitors across MOSFETs are in circuit at any one time. This is because half of the capacitors are shorted out by MOSFETs which have been turned on. The resonant frequency of the tank circuit and drain source capacitors is given by Equation 1.

$$f = \frac{1}{2\pi\sqrt{L.C_{tot}}} \qquad 1$$

Where C_{tot} is the equivalent capacitance of the tank circuit capacitor and the drain source capacitors and is given by Equation 2.

$$C_{tot} = C_t + C_{DS} \quad (2)$$

Therefore the resonant frequency of the tank circuit is 155 kHz.

An expression for the impedance at resonance of the parallel resonant circuit (Z_D) is given in Equation 3.

$$Z_D = \frac{L}{C_{tot}.R} \quad (3)$$

The Q of the circuit is given by Equation 4.

$$Q = \frac{1}{R}.\sqrt{\frac{L}{C_{tot}}} \quad (4)$$

Substituting Equation 3.

$$Z_D = Q.\sqrt{\frac{L}{C_{tot}}} \quad (5)$$

Thus Z_D for the parallel resonant load was 2.7 kOhms.

In a conventional rectangular switching circuit the connection of capacitors across MOSFETs will cause additional losses. These losses are caused because when a MOSFET turns on, the energy stored in the drain source capacitance is dissipated in the MOSFET and in a series resistor. This series resistor is necessary to limit the current spike in the MOSFET at turn on. These losses are appreciable at 150 kHz, e.g. the connection of 1 nF across a MOSFET switching 600 V would cause losses of more than 25 W at 150 kHz. In the current fed inverter described in this article the MOSFETs turn on when the voltage across the capacitor is ideally zero. Thus there is no need for a series resistor and the turn on losses are ideally zero.

In this case the supply to the inverter was 470 V rms. This means that the peak voltage in the d.c. link was 650 V.

Equating the power flowing in the d.c. link to the power dissipated in the tank circuit produces an expression for the peak voltage across the tank circuit (V_T) as given in Equation 6.

$$V_T = 2 \times \sqrt{2} \times 1.11 \times V_{dclink} \quad (6)$$

Therefore the peak to peak voltage across the tank circuit was ideally 2050 V

The voltage across each MOSFET should be 512 V.

Circuit performance

The switching frequency of this circuit is 120 kHz. Thus the load is fed slightly below its resonant frequency. This means that the load looks inductive and ensures that the MOSFETs do not switch on when the capacitors connected across their drain source terminals are charged.

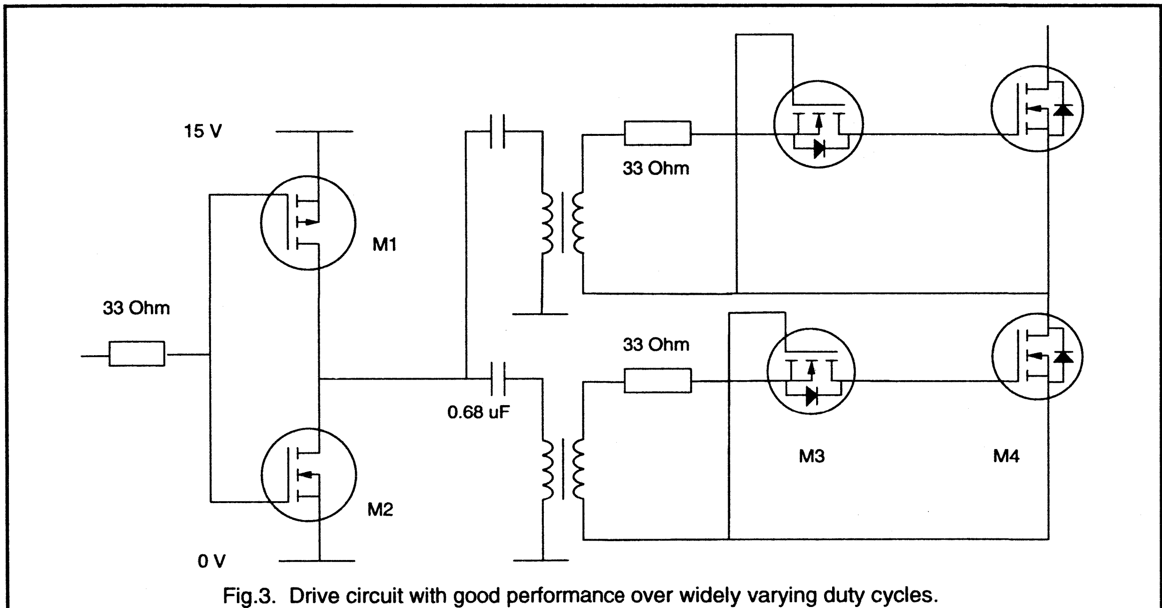


Fig.3. Drive circuit with good performance over widely varying duty cycles.

The waveforms of the voltage across two MOSFETs in series in a leg of the inversion bridge are shown in Fig.4. It can be seen that the sharing is excellent. The peak voltage across each MOSFET is 600 V. This is higher than 512 V because of ringing between parasitic lead inductance and the drain source capacitance of MOSFETs when they switch off.

The MOSFETs carry two components of current. The first component is the d.c. link current. The second component is a fraction of the circulating current of the tank circuit. The size of the second component is dependent on the relative sizes of the drain source capacitance connected across MOSFETs and the tank circuit capacitor.

In this circuit the peak value of charging current for drain source capacitors, which is carried by the MOSFET, is 4 A. The on-resistance of the BUK456-800B is about 5 Ohms at 80 ˚C. This explains the rise in $V_{DS(ON)}$ of about 20 V seen in Fig.4 just above the turn off of the MOSFETs.

The sharing of Philips PowerMOS in this configuration is so good that the value of drain source capacitance is not determined by its beneficial effect on sharing. The minimum value of drain source capacitance will be selected to reduce ringing. The value is dependent on power output and layout. The increased current levels associated with increased power output make the ringing worse. A higher power output usually involves a larger number of MOSFETs connected in parallel. Therefore a value of drain source capacitance for each MOSFET can be specified independent of the power output of the supply. A value of between 5 and 10 nF is sufficient if sensible practice as regards layout is adopted e.g. twisting leads to reduce loop inductance.

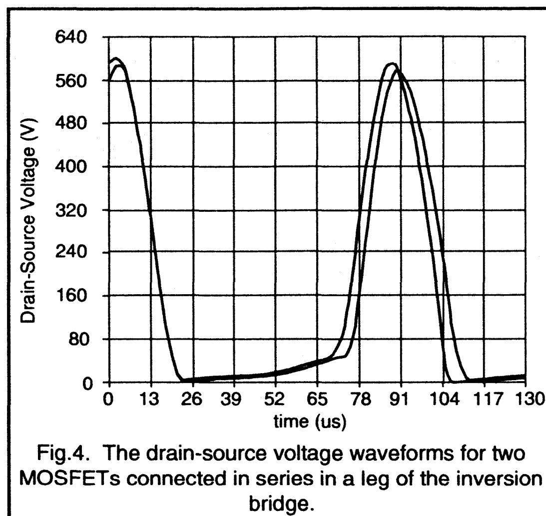


Fig.4. The drain-source voltage waveforms for two MOSFETs connected in series in a leg of the inversion bridge.

Conclusions

It has been shown that MOSFETs can be connected in series to realise a switch that is as high as 90% of the sum of the voltage sustaining capabilities of the individual transistors.

1.2.6 Logic Level FETS

Standard Power MOSFETs require a gate-source voltage of 10 V to be fully ON. With Logic Level FETs (L^2FETs) however, the same level of conduction is possible with a gate-source voltage of only 5 V. They can, therefore, be driven directly from 5 V TTL/CMOS ICs without the need for the level shifting stages required for standard MOSFETs, see Fig.1. This makes them ideal for today's sophisticated electrical systems, where microprocessors are used to drive switching circuits.

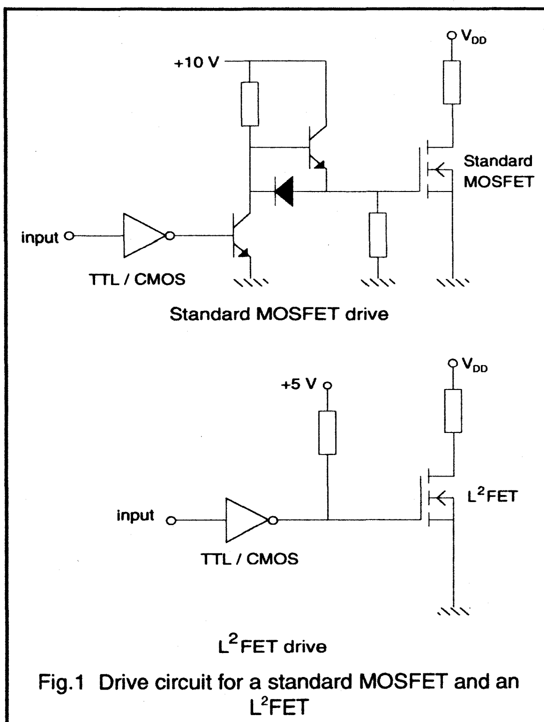


Fig.1 Drive circuit for a standard MOSFET and an L^2FET

This characteristic of L^2FETs is achieved by reducing the gate oxide thickness from - 800 Angstroms to - 500 Angstroms, which reduces the threshold voltage of the device from the standard 2.1-4.0 V to 1.0-2.0 V. However the result is a reduction in gate-source voltage ratings, from ±30 V for a standard MOSFET to ±15 V for the L^2FET. The ±15 V rating is an improvement over the 'industry standard' of ±10 V, and permits Philips L^2FETs to be used in demanding applications such as automotive.

Although a 5 V gate-drive is ideal for L^2FETs, they can be used in circuits with gate-drive voltages of up to 10 V. Using a 10 V gate-drive results in a reduced $R_{DS(ON)}$ (see Fig.2) but the turn-off delay time is increased. This is due to excessive charging of the L^2FET's input capacitance.

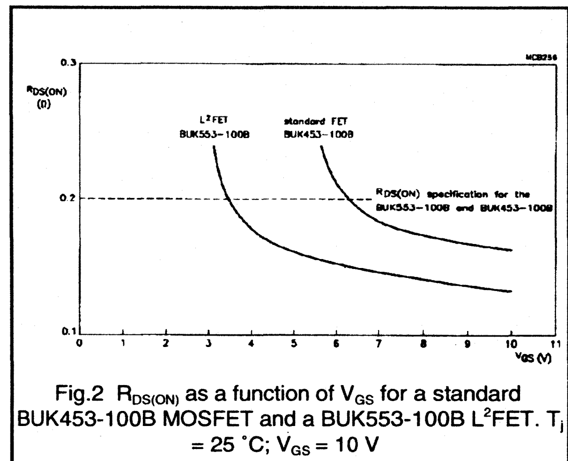


Fig.2 $R_{DS(ON)}$ as a function of V_{GS} for a standard BUK453-100B MOSFET and a BUK553-100B L^2FET. T_j = 25 ˚C; V_{GS} = 10 V

Capacitances, Transconductance and Gate Charge

Figure 3 shows the parasitic capacitances areas of a typical Power MOSFET cell. Both the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} increase due to the reduction in gate oxide thickness, although the increase in C_{gd} is only significant at low values of V_{DS}, when the depletion layer is narrow. Increases of the order of 25% in input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss} result for the L^2FET, compared with a similar standard type, at V_{DS} = 0 V. However at the standard measurement condition of V_{DS} = 25 V the differences are virtually negligible.

Forward transconductance g_{fs} is a function of the oxide thickness so the g_{fs} of an L^2FET is typically 40% - 50% higher than a standard MOSFET. This increase in g_{fs} more than offsets the increase in capacitance of an L^2FET, so the turn on charge requirement of the L^2FET is lower than the standard type see Fig.4. For example, the standard BUK453-100B MOSFET requires about 17 nC to be fully switched on (at a gate voltage of 10 V) while the BUK553-100B L^2FET only needs about 12 nC (at a gate source voltage of 5 V).

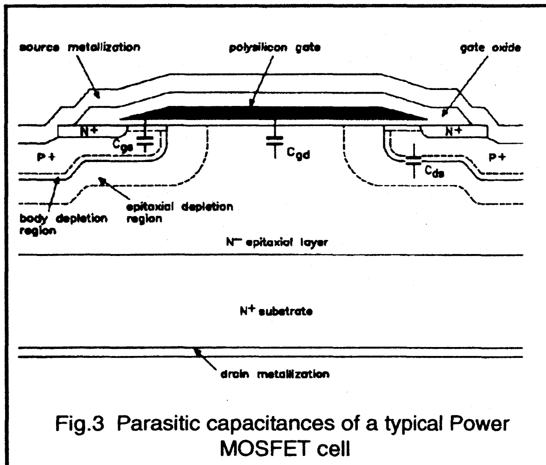


Fig.3 Parasitic capacitances of a typical Power MOSFET cell

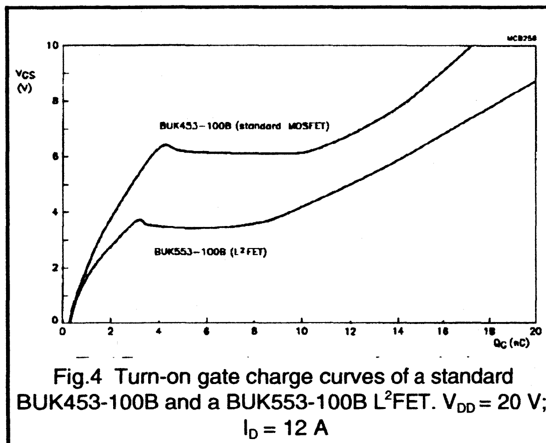


Fig.4 Turn-on gate charge curves of a standard BUK453-100B and a BUK553-100B L^2FET. V_{DD} = 20 V; I_D = 12 A

Switching speed.

Figure 5 compares the turn-on performance of the standard BUK453-100B MOSFET and the BUK553-100B L^2FET, under identical drive conditions of 5 V from a 50 Ω generator using identical loads. Thanks to its lower gate threshold voltage V_{GST}, the L^2FET can be seen to turn on in a much shorter time from the low level drive.

Figure 6 shows the turn-off performance of the standard BUK453-100B MOSFET and the BUK553-100B L^2FET, again with the same drive. This time the L^2FET is slower to switch. The turn-off times are determined mainly by the time required for C_{gd} to discharge. The C_{gd} is higher for the L^2FET at low V_{DS}, and the lower value of V_{GST} leads to a lower discharging current. The net result is an increase in turn off time.

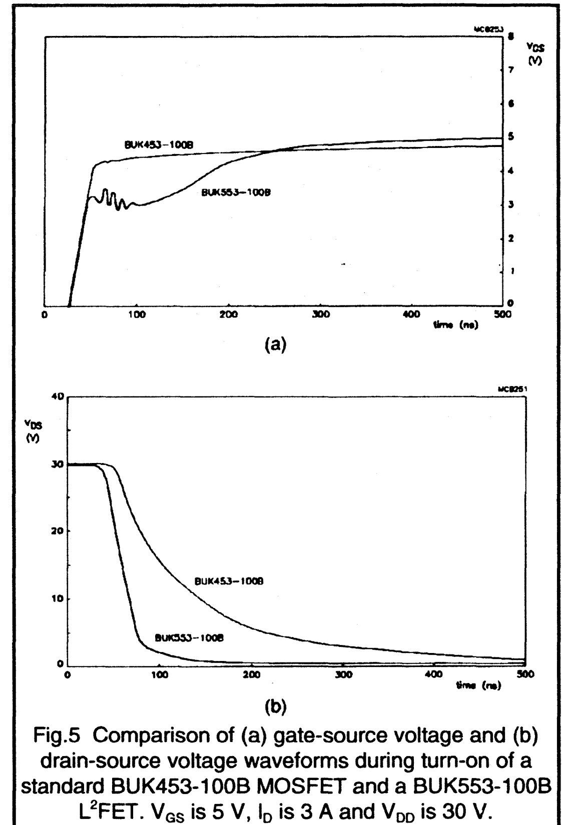


Fig.5 Comparison of (a) gate-source voltage and (b) drain-source voltage waveforms during turn-on of a standard BUK453-100B MOSFET and a BUK553-100B L^2FET. V_{GS} is 5 V, I_D is 3 A and V_{DD} is 30 V.

Fast switching in many applications, for example automotive circuits, is not important. In areas where it is important however the drive conditions should be examined. For example, for a given drive power, a 10 V drive with a 50 Ω source impedance is equivalent to a 5 V drive with a source impedance of only 12 Ω. This results in faster switching for the L^2FET compared with standard MOSFETs.

Ruggedness and reliability

MOSFETs are frequently required to be able to withstand the energy of an unclamped inductive load turn-off. Since this energy is dissipated in the bulk of the silicon, stress is avoided in the gate oxide. This means that the ruggedness performance of L^2FETs is comparable with that of standard MOSFETs. The use of thinner gate oxide in no way compromises reliability. Good control of key process parameters such as pinhole density, mobile ion content, interface state density ensures good oxide quality. The projected MTBF is 2070 years at 90˚C, at a 60% confidence level.

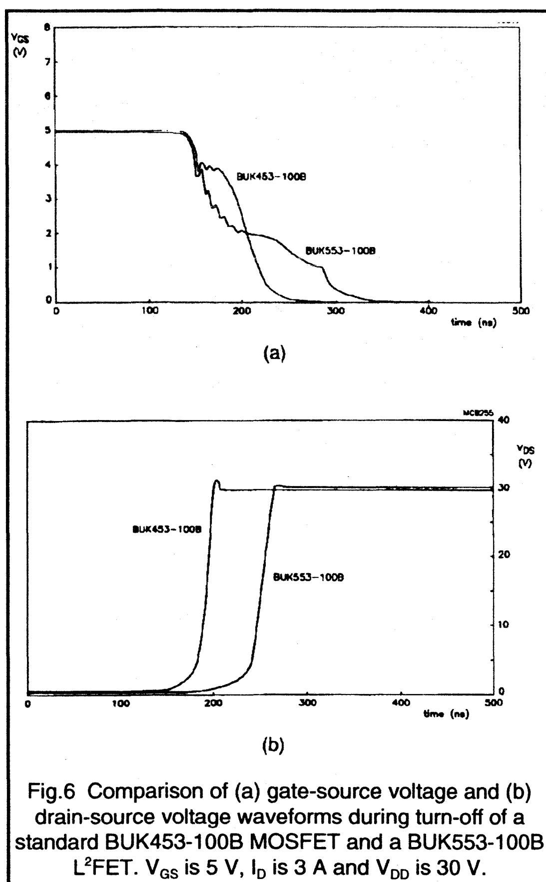


Fig.6 Comparison of (a) gate-source voltage and (b) drain-source voltage waveforms during turn-off of a standard BUK453-100B MOSFET and a BUK553-100B L^2FET. V_{GS} is 5 V, I_D is 3 A and V_{DD} is 30 V.

The V_{GS} rating of an L^2FET is about half that of a standard MOSFET, but this does not affect the V_{DS} rating. In principle, an L^2FET version of any standard MOSFET is feasible.

Temperature stability

In general threshold voltage decreases with increasing temperature. Although the threshold voltage of L^2FETs is lower than that of standard MOSFETs, so is their temperature coefficient of threshold voltage (about half in fact), so their temperature stability compares favourably with standard MOSFETs. Philips low voltage L^2FETs ($\leq$200v) in TO220 all feature T_{jmax} of 175˚C, rather than the industry standard of 150˚C.

Applications

The Philips Components range of rugged Logic Level MOSFETs enable cost effective drive circuit design without compromising ruggedness or reliability. Since they enable power loads to be driven directly from ICs they may be considered to be the first step towards intelligent power switching. Thanks to their good reliability and 175˚C T_{jmax} temperature rating, they are displacing mechanical relays in automotive body electrical functions and are being designed in to such safety critical areas as ABS.

1.2.7 Current Sensing MOSFETs

The increasing popularity of current mode control in switched mode power supply and motor drive applications, has lead to the widespread use of current sensing techniques in power conditioning circuits. Such techniques have traditionally involved the use of either a series resistor or current transformer to monitor the instantaneous current in the switching device. Both techniques present serious disadvantages to the designer. Insertion of a series resistor results in power loss to the circuit which must be dissipated by the resistor. A high power, low resistance, non-inductive component is thus generally required which can add appreciable cost to the system. The alternative method of using a current transformer can also be costly and is usually inconvenient.

The Philips SensorFET is a Power MOSFET which divides the load current into power and sense components. The sense current can be monitored with a cheap, signal level resistor, thus avoiding power loss and presenting circuit designers with a simple and efficient means of current sampling.

SensorFET operation

A PowerMOS transistor is essentially an I.C. comprising many thousands of small individual transistors connected in parallel. Each of the transistor elements within the device is identical and current distributes equally between equal on-resistances. It is possible to isolate the source connections to several cells from those of all the other cells and bring them out to a separate bond pad. The PowerMOS is now effectively two transistors; a low R_{DSON} Power transistor and a high R_{DSON} sense transistor. Current will share between the two parts according to the ratio of the on-resistances of each, which is the principle of operation of the Philips SensorFET.

The relative sizes of the two FETs is determined by the ratio of the number of sense cells to the number of Power cells. This figure is of the order 1:1500. The distribution of current between sense and power parts is given by the drain to measure current ratio, I_D/I_M. This ratio is defined for the condition where the measure and source terminals are held at the same potential. Since this ratio is of the order 1500:1, the drain current and current in the source power lead may be considered the same.

The SensorFET is assembled in a standard 5-pin TO220 plastic encapsulated package; the two extra pins being the measure terminal and a kelvin source connection. The symbol for a SensorFET is illustrated in Fig.1. The equivalent circuit of the SensorFET is shown in Fig.2 illustrating two parallel FETs with separate source connections but common gate and drain connections. The separate source connection is termed the measure terminal.

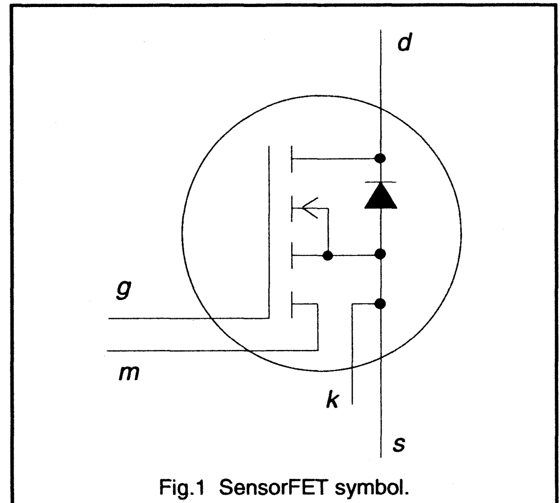


Fig.1 SensorFET symbol.

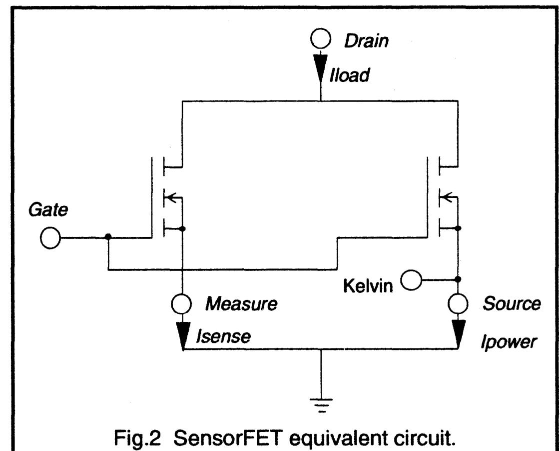


Fig.2 SensorFET equivalent circuit.

Current sensing is achieved with the insertion of a signal level resistor between the measure and kelvin source terminals, avoiding the necessity for a measure resistor in the power circuit. The calculation of load current, is straightforward provided certain design rules are adhered to. The derivation of these rules is easily understood when considering the on-state model of the SensorFET as described below.

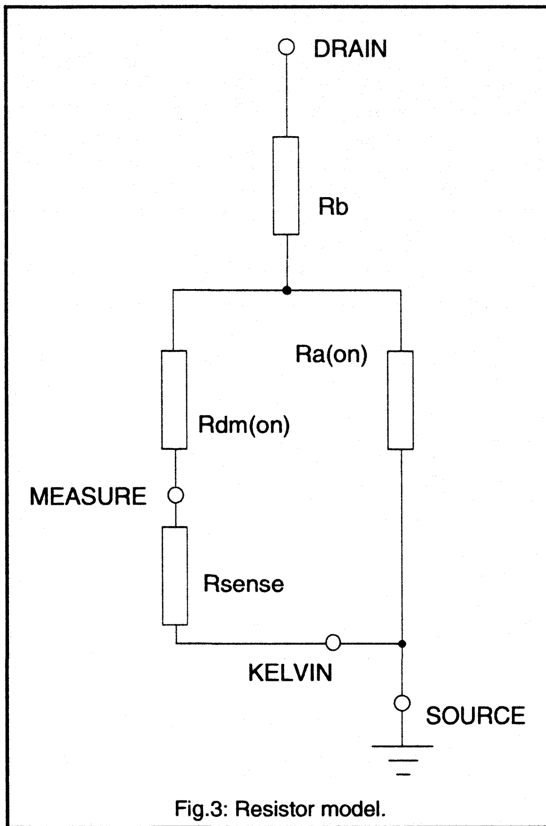


Fig.3: Resistor model.

A SensorFET in its on-state may be represented by the model shown in Fig.3. The device is separated into its resistive components distinguishing between the bulk drain resistance, R_B, common to both devices and the active components $R_{DM(ON)}$ and $R_{A(ON)}$. $R_{DM(ON)}$ is the drain to measure on-state resistance with $R_{A(ON)}$ being the active component for the power part. R_{sense} represents the external sense resistor. Using this model the equation which describes the sense voltage is simply:

$$V_{SENSE} = R_{SENSE} \cdot \frac{I_D \cdot R_{A(ON)}}{(R_{DM(ON)} + R_{SENSE})} \quad .....1$$

Equation (1) may be re-arranged to give expressions for R_{sense} and I_D, equations 2 and 3.

$$R_{SENSE} = \frac{V_{SENSE} \cdot R_{DM(ON)}}{\{(I_D \cdot R_{A(ON)}) - V_{SENSE}\}} \quad ......2$$

$$I_D = V_{SENSE} \cdot \frac{(R_{SENSE} + R_{DM(ON)})}{(R_{A(ON)} \cdot R_{SENSE})} \quad ......3$$

From equation 1, if R_{SENSE} is made very large compared to $R_{DM(ON)}$, V_{SENSE} becomes equal to I_D $R_{A(ON)}$. This value is clearly the maximum sense voltage that can be obtained and as such represents the compliance of the measure terminal. A value for $R_{A(ON)}$ may be determined from the potential between the measure and Kelvin terminals with the measure terminal open circuit, $R_{A(ON)} = V_{SENSE} / I_D$. A value for $R_{DM(ON)}$ can be gained from $R_{DM(ON)} = R_{A(ON)} \cdot n$ where n is the drain to measure current ratio. Since R_B will be very small compared to $R_{DM(ON)}$, the latter may also be measured directly as the drain to measure on-state resistance. Typical values for the BUK795-60 (60 V, 36 A) are $R_{A(ON)}$ 21 mΩ, R_B = 24 mΩ and $R_{DM(ON)}$ = 35 Ω with n = 1645.

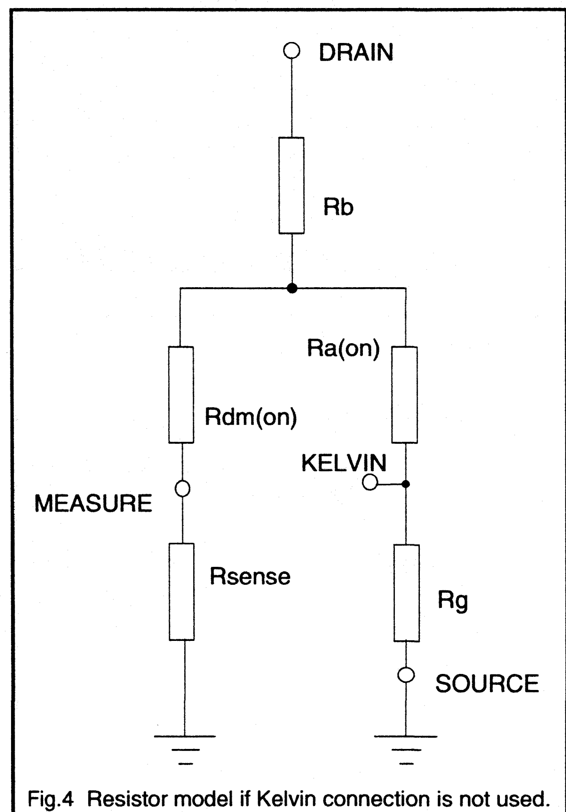


Fig.4 Resistor model if Kelvin connection is not used.

In order to maintain accuracy it is important that the sense voltage be measured with respect to the kelvin terminal as depicted in Fig.3. To understand the necessity for the kelvin terminal consider the situation if the low side of the sense resistor and the Power source were connected to a common ground. The equivalent circuit would then be as shown in Fig.4 with the additional resistance R_G representing wire resistance, contact resistance and ground loop resistance in the power circuit. This resistance adds to the active

component $R_{A(ON)}$ and renders equation 1 inaccurate. The kelvin source terminal which connects direct to the source metallisation allows for R_G to be by-passed which is essential for the correct application of the above equations.

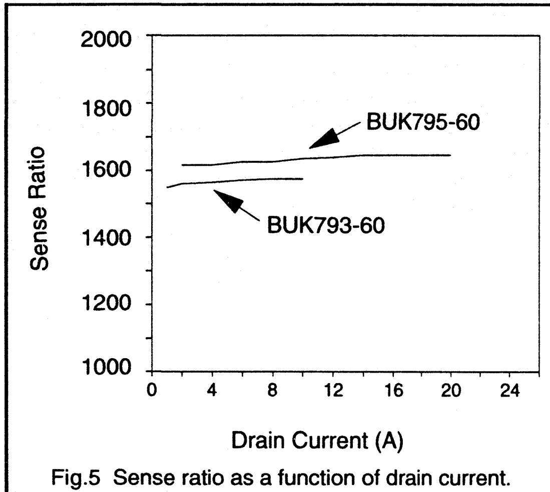


Fig.5 Sense ratio as a function of drain current.

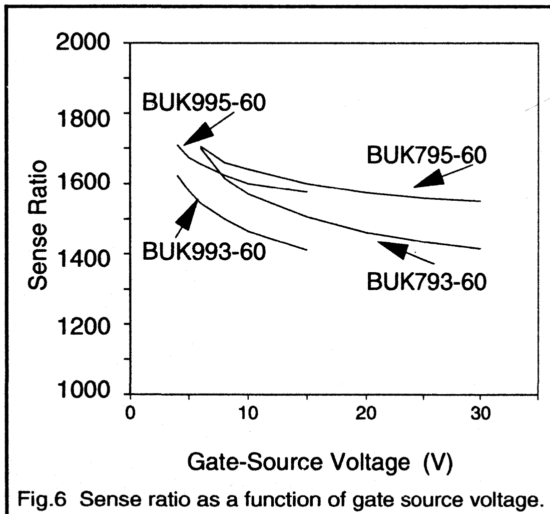


Fig.6 Sense ratio as a function of gate source voltage.

Properties of the current sense

The drain to measure current ratio, I_D/I_M (V_{MK} = 0 V) is primarily determined by the ratio of the sense and power cell areas. Some of the properties of this ratio are now considered.

Examples of current sense ratio as a function of drain current, gate source voltage and junction temperature are given in Figs.5-7. Sense ratio is observed to be essentially independent of current and junction temperature. In the latter case the change between 25 ˚C and 175 ˚C is less than 2%. The effect of reducing gate source voltage is shown for both Logic Level and Standard SensorFET types and is observed to increase slightly the sense ratio. Sense ratio as a function of temperature and gate voltage are device characteristics supplied with the SensorFET data.

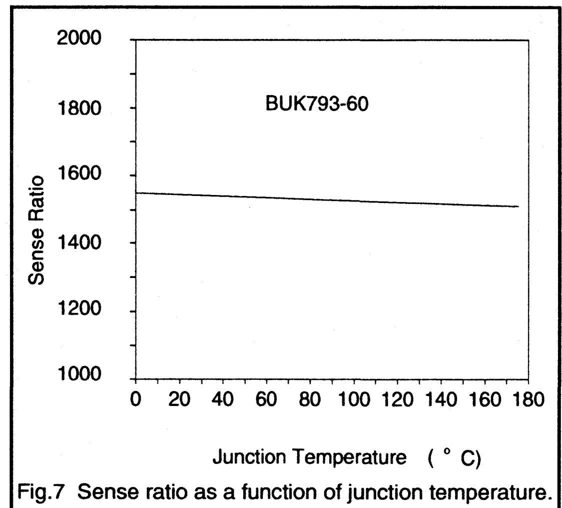


Fig.7 Sense ratio as a function of junction temperature.

Current sensing

A typical SensorFET application is illustrated in Fig.8. A resistor connected between the measure and kelvin terminals converts the sense current into a sense voltage which is then fed into a comparator for the purpose of short circuit detection. The effectiveness of this type of circuit and others using resistive current sensing clearly depends on the accuracy with which the load current may be predicted from the sense voltage.

Equation 3 may be re-arranged to express the effective current ratio n', equation 4.

$$n' = n \cdot \left(1 + \frac{R_{SENSE}}{R_{DM(ON)}}\right) \quad \text{......4}$$

Equation 4 demonstrates an important point, that the achieved current sense ratio is a function of the ratio of sense resistor to the drain measure resistance of the SensorFET.

The on-resistance of a Power MOSFET is a function of junction temperature, approximately doubling in value between 25 ˚C and 150 ˚C. The value of $R_{DM(ON)}$ is therefore temperature sensitive as described by equation (5).

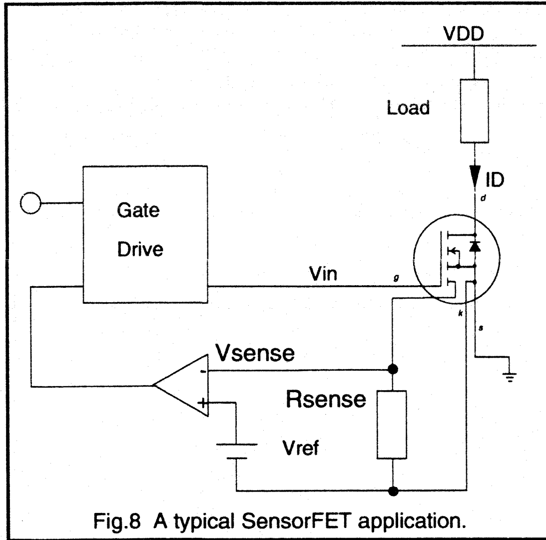


Fig.8 A typical SensorFET application.

$$R_{DM(ON)}[T] = R_{DM(ON)}[25°C] \cdot \exp\{k(T-25)\} ......5$$

$$\text{where } k = \left(\frac{1}{125}\right) \cdot \ln\left\{\frac{R_{DM(ON)}[150°C]}{R_{DM(ON)}[25°C]}\right\}$$

Inclusion of the temperature sensitive expression for $R_{DM(ON)}$ in equation 4 yields n' as a function of sense resistance and junction temperature.

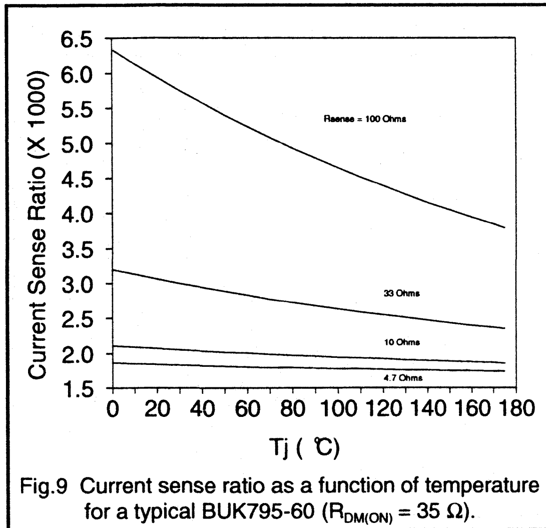


Fig.9 Current sense ratio as a function of temperature for a typical BUK795-60 ($R_{DM(ON)} = 35\ \Omega$).

Plotting this expression, Fig.9, demonstrates how the current sense ratio becomes increasingly temperature dependant as the value of R_{SENSE} becomes comparable to and greater than $R_{DM(ON)}$(25 ˚C). Modifying equation 1 to include temperature variation in a similar fashion yields equation (6).

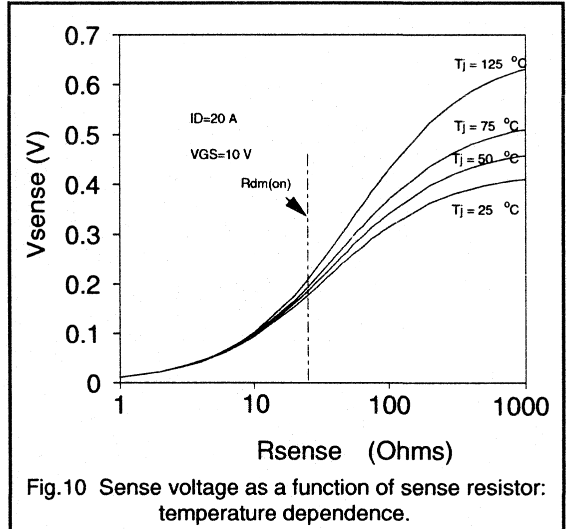


Fig.10 Sense voltage as a function of sense resistor: temperature dependence.

$$V_{SENSE}[T] = \frac{I_{LOAD} \cdot R_{SENSE}}{n \cdot \left\{1 + \frac{R_{SENSE}}{R_{DM(ON)}[25C] \cdot \exp\{k(T-25)\}}\right\}} ......6$$

The increasing temperature dependency of sense voltages for values of R_{SENSE} greater than $R_{DM(ON)}$ is shown clearly in Fig.10.

Figure 11 shows a comparison between measured and calculated values of V_{SENSE} as a function of drain current. Results for both the BUK795-60 and BUK793-60 are presented for several values of R_{SENSE} at a Tj of 25 ˚C and 125 ˚C. Equation 6 is seen to accurately predict sense voltage for values of R_{SENSE} less than or comparable to $R_{DM(ON)}$. Above this value some discrepancy is observed when sensing at high currents. This is explained by the effects of internal heating and the difference in the power dissipation for the sense cells compared to the power cells. Once R_{SENSE} starts to exceed $R_{DM(ON)}$ the current flowing in the sense cells is significantly reduced compared to that in the power cells and hence the degree of internal heating in the power and sense parts differs. As a result the ratio of the power and sense resistances is subject to a slight decrease such that the value of the sense current is increased.

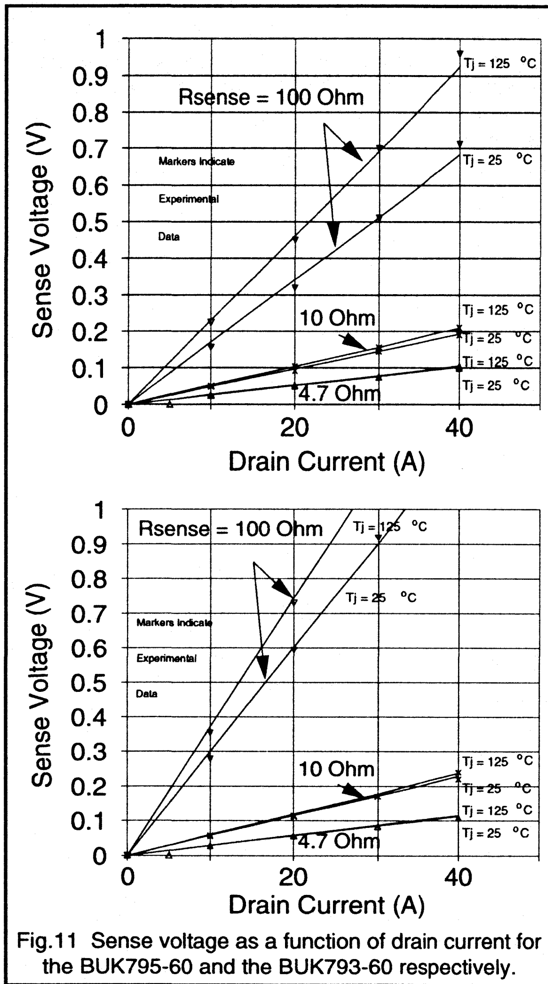


Fig.11 Sense voltage as a function of drain current for the BUK795-60 and the BUK793-60 respectively.

As well as the variation with temperature, device to device spreads in $R_{DM(ON)}$) and drain to measure current ratio must also be considered in relation to effect on sensing accuracy. The sensing parameters for the BUK795-60 are given below.

	MIN	TYP	MAX
$R_{DM(ON)}$ (Ω)		35	50
I_D/I_M	1560	1645	1730

Sense voltage as a function of R_{SENSE} for typical and limit devices is shown in Fig.12. Sense resistor values less than $R_{DM(ON)}$ are observed to generate sense voltages insensitive to any spread in device parameter which may occur. For R_{SENSE} greater than $R_{DM(ON)}$ sense voltage becomes increasingly susceptible to device variation.

The above results demonstrate how good accuracy is achieved for resistive current sensing when the sense resistor is chosen to be less than the drain to measure on-resistance $R_{DM(ON)}$. For the majority of applications such a constraint is not a problem. There may however be some circumstances when current sensing at low currents requires a larger sense voltage than can be generated by a resistor of the above magnitude. In such cases it may be necessary to employ the virtual earth current sensing method.

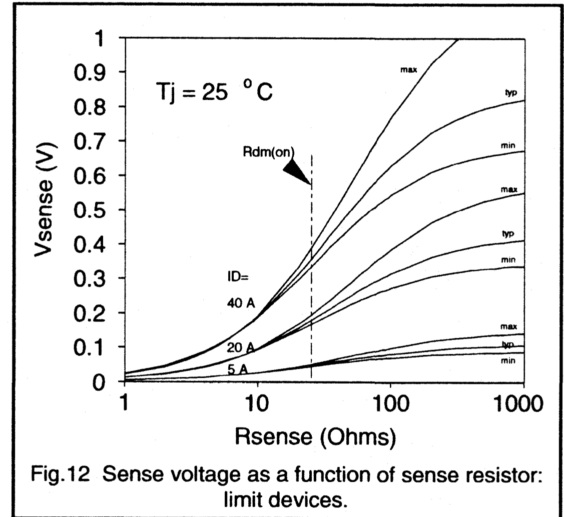
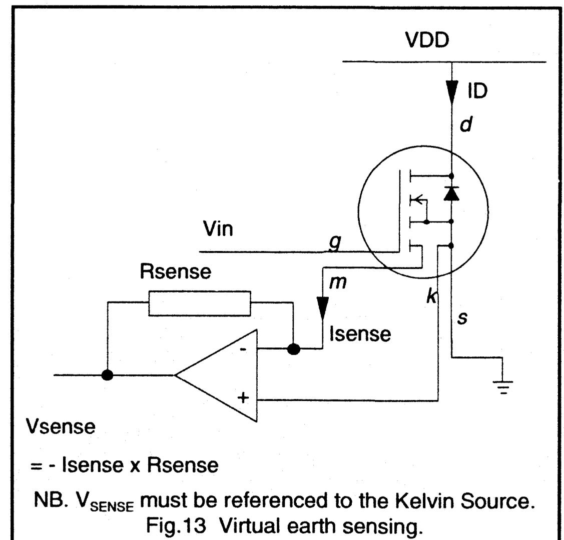


Fig.12 Sense voltage as a function of sense resistor: limit devices.



NB. V_{SENSE} must be referenced to the Kelvin Source.
Fig.13 Virtual earth sensing.

The circuit for virtual earth current sensing is shown in Fig.13. The equation which describes the sense voltage is now given as:

$$V_{SENSE} = \frac{I_{LOAD} \cdot R_{SENSE}}{n} \quad \ldots\ldots 7$$

A major advantage of the virtual earth method is that the drain to measure current ratio becomes independent of the sense resistance and junction temperature. The ratio is equal to the data sheet value. The primary constraint of the virtual earth circuit is the need for the op-amp to sink the sense current. Attention to this point is only required should virtual earth sensing be employed at high currents.

Noise suppression

During the switching interval the sense current is not well defined and can appear noisy. Current spikes are evident which originate from the charging of the gate source capacitance and the circuit stray capacitance and inductance. To avoid false information feeding through from the current sense a simple RC filter can be used to remove turn-on transients.

Special operating modes

Diode conduction

The sense and power parts of the SensorFET are structurally identical both having a built in anti parallel diode. Certain applications, such as ac motor control, use this diode as an integral part of the circuit operation (Fig.14). For the SensorFET, during the conduction cycle of the internal diode, reverse sense current will flow. If a virtual earth sense circuit is being used then the sense voltage is a true reflection of the load current. Diode conduction is however, bipolar and as such the on-resistance is modulated by the current flow. Consequently the presence of a sense resistor between measure and kelvin has a direct influence on the value of $R_{DM(ON)}$ and hence the current ratio. Current sensing during the diode conducting cycle is thus inaccurate using the resistive method.

Recovery current overshoot

MOSFETs in bridge circuits can experience high current overshoot at turn-on due to the recovery current of the flywheel diode in the opposing leg. Using the circuit of Fig.14 as an example, starting with current flow in the flywheel diode of the upper leg. When the MOSFET in the lower leg is switched on a large current overshoot gives rise to a high peak sense voltage. The size of the overshoot is a function of the original current in the diode and the speed of turn-on of the SensorFET. The sense voltage will therefore pass through a peak at turn-on which may be more than double the on-state level. Again low pass filtering should be used to avoid any false triggering of over-current protection circuitry.

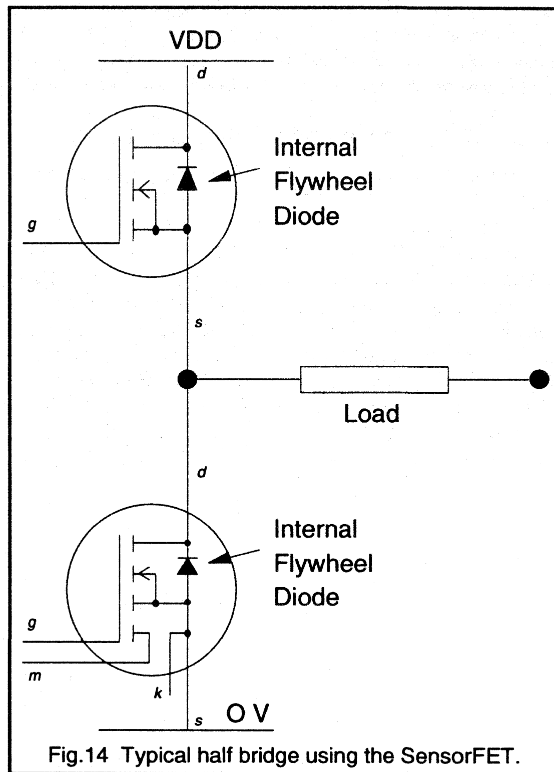


Fig.14 Typical half bridge using the SensorFET.

Avalanche operation

The ability of a SensorFET to dissipate energy while operating in its avalanche mode, is independent of the sense circuitry used between the measure and kelvin terminals. The SensorFET is however unable to provide accurate current sensing during a period of avalanche operation. While the SensorFET is supporting its avalanche voltage it is operating outside its linear mode and hence the on-state model of Fig.3 is not applicable. Consequently the sense voltage during the inductive turn-off period is not representative of the avalanche current flowing in the device.

High Speed Switching

The kelvin source connection provides for a very fast switching capability. Theoretically the switching speed of a MOSFET is limited only by the ability of the drive circuit to charge and discharge the gate capacitance. In practice for a standard 3 terminal MOSFET, the switching transitions represent a large di/dt which reacts with the finite inductance of the source bonding wire and source lead. This gives rise to a potential difference between the source metallisation and the external source terminal. This voltage will add to, or subtract from, the applied gate drive (depending on the sign of the di/dt) so as to oppose the

switching transition. The SensorFET enables gate drive to be referenced direct to the source metallisation so by-passing the inductances of the power source connection. Very fast switching speeds are thus possible.

SensorFET compatible integrated circuits

As a general rule current limit comparators and operational amplifiers require 100 to 200 mV sensitivity for SensorFET compatibility. Two recently developed I.C.s suitable for use with the SensorFET are the AU2903 low power dual voltage comparator, and the AU2904 low power dual operational amplifier. Both these components feature operational capability from a single power supply and an input common-mode voltage range which includes ground. A number of driver/control I.C.s are also available which comply with this sensitivity requirement. They are listed as follows:

Device	Description	Application
AU2903	Comparitor	General
AU2904	Op. AMP	General
MC33152	SensorFET Driver	Micro-processor Interface
MC33034	Motor Controller	Brushless DC Motors
MC34129	Current Mode Controller	Push-Pull SMPS

All of these devices function comfortably with output voltages that SensorFETs provide.

Conclusion

The SensorFET offers an efficient and cost effective method for current sampling in power circuits. The instantaneous device current can be monitored by either a signal level resistor or a virtual earth op-amp arrangement. Choice of resistor is straightforward provided certain guide-lines are adhered to. A relatively simple relationship exists between the sense and load currents, which is dependent on the value of sense resistor used.

1.2.8 Avalanche Ruggedness

Recent advances in power MOS processing technology now enables power MOS transistors to dissipate energy while operating in the avalanche mode. This feature results in transistors able to survive in-circuit momentary overvoltage conditions, presenting circuit designers with increased flexibility when choosing device voltage grade against required safety margins.

This paper considers the avalanche characteristics of 'rugged' power MOSFETs and presents results from investigations into the physical constraints which ultimately limit avalanche energy dissipation in the VDMOS structure. Results suggest that the maximum sustainable energy is a function of the applied power density waveform, independent of device voltage grade and chip size.

The ability of a rugged device to operate reliably in a circuit subject to extreme interference is also demonstrated.

Introduction.

Susceptibility to secondary breakdown is a phenomenon which limits the power handling capability of a bipolar transistor to below its full potential. For a power MOSFET, power handling capability is a simple function of thermal resistance and operating temperature since the device is not vulnerable to a second breakdown mechanism. The previous statement holds true provided the device is operated at or below its breakdown voltage rating (B_{VDSS}) and not subject to overvoltage. Should the transistor be forced into avalanche by a voltage surge the structure of the device permits possible activation of a parasitic bipolar transistor which may then suffer the consequences of second breakdown. In the past this mechanism was typical of failure in circuits where the device became exposed to overvoltage. To reduce the risk of device failure during momentary overloads improvements have been introduced to the Power MOS design which enable it to dissipate energy while operating in the avalanche condition. The term commonly used to describe this ability is 'Ruggedness', however before discussing in further detail the merits of a rugged Power MOSFET it is worth considering the failure mechanism of non-rugged devices.

Failure mechanism of a non-rugged Power MOS.

A power MOS transistor is made up of many thousands of cells, identical in structure. The cross section of a typical cell is shown in Fig.1. When in the off-state or operating in saturation, voltage is supported across the p-n junction as shown by the shaded region. If the device is subjected to over-voltage (greater than the avalanche value of the device), the peak electric field, located at the p-n junction, rises to the critical value (approx. 200 kV / cm) at which avalanche multiplication commences. Computer modelling has shown that the maximum electric field occurs on the corner of the P+ diffusion. The electron-hole plasma generated by the avalanche process in this region gives rise to a source of electrons which are swept across the drain and a source of holes which flow through the P+ and P body regions towards the source metal contact. Clearly the P- region constitutes a resistance which will give rise

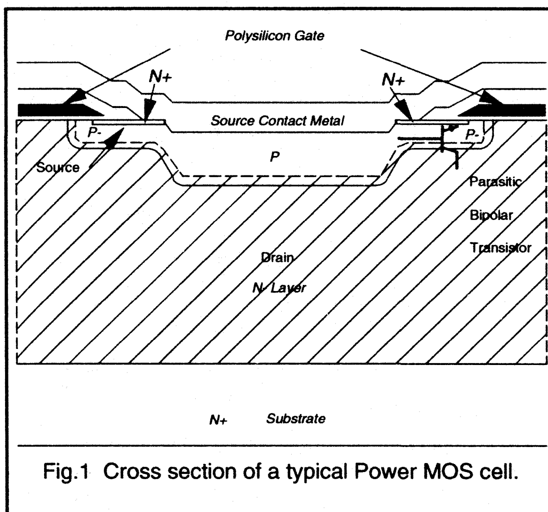


Fig.1 Cross section of a typical Power MOS cell.

to a potential drop beneath the n+. If this resistance is too large the p-n junction may become forward biased for relatively low avalanche currents. Also if the manufacturing process does not yield a uniform cell structure across the device or if defects are present in the silicon then multiplication may be a local event within the crystal. This would give rise to a high avalanche current density flowing beneath the source n+ and cause a relatively large potential drop sufficient to forward bias the p-n junction and hence activate the parasitic npn bipolar transistor inherent in the MOSFET structure. Due to the positive temperature coefficient associated with a forward biased p-n junction, current crowding will rapidly ensue with the likely result of second breakdown and eventual device destruction.

In order that a power MOS transistor may survive transitory excursions into avalanche it is necessary to manufacture a device with uniform cell structure, free from defects throughout the crystal and that within the cell the resistance beneath the n+ should be kept to a minimum. In this way a forward biasing potential across the p-n junction is avoided.

Definition of ruggedness.

The term 'Ruggedness' when applied to a power MOS transistor, describes the ability of that device to dissipate energy while operating in the avalanche condition. To test ruggedness of a device it is usual to use the method of unclamped inductive load turn-off using the circuit drawn in Fig.2.

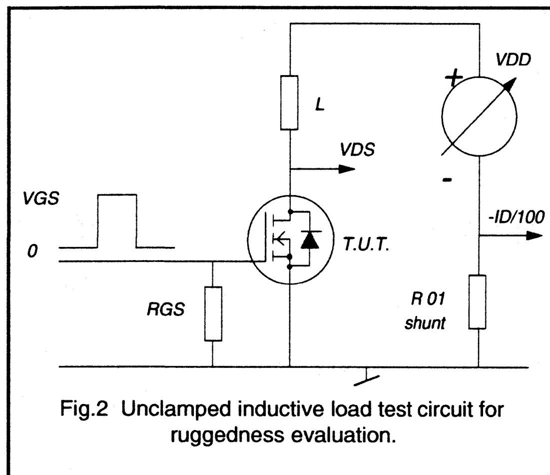


Fig.2 Unclamped inductive load test circuit for ruggedness evaluation.

Circuit operation:-

A pulse is applied to the gate such that the transistor turns on and load current ramps up according to the inductor value, L and drain supply voltage, V_{DD}. At the end of the gate pulse, channel current in the power MOS begins to fall while voltage on the drain terminal rises rapidly in accordance with equation 1.

$$\frac{dv}{dt} = L\frac{d^2I}{dt^2} \tag{1}$$

The voltage on the drain terminal is clamped by the avalanche voltage of the Power MOS for a duration equal to that necessary for dissipation of all energy stored in the inductor. Typical waveforms showing drain voltage and source current for a device undergoing successful test are shown in Fig.3.

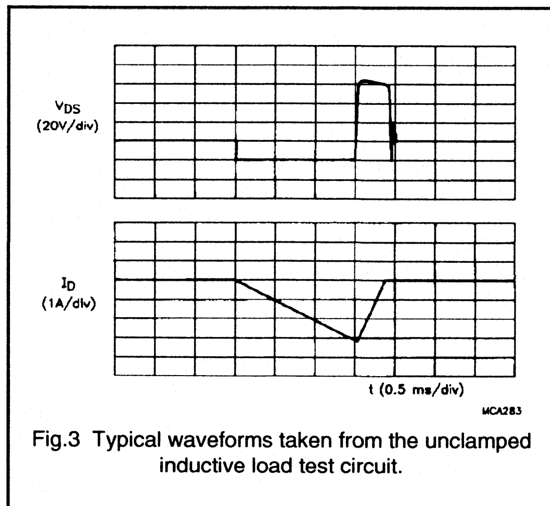


Fig.3 Typical waveforms taken from the unclamped inductive load test circuit.

The energy stored in the inductor is given by equation 2 where I_D is the peak load current at the point of turn-off of the transistor.

$$W_{DSS} = 0.5LI_D^2 \tag{2}$$

All this energy is dissipated by the Power MOS while the device is in avalanche.

Provided the supply rail is kept below 50 % of the avalanche voltage, equation 2 approximates closely to the total energy dissipation by the device during turn-off. However a more exact expression which takes account of additional energy delivered from the power supply is given by equation 3.

$$W_{DSS} = \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} 0.5LI_D^2 \tag{3}$$

Clearly the energy dissipated is a function of both the inductor value and the load current I_D, the latter being set by the duration of the gate pulse. The 50 Ohm resistor between gate and source is necessary to ensure a fast turn-off such that the device is forced into avalanche.

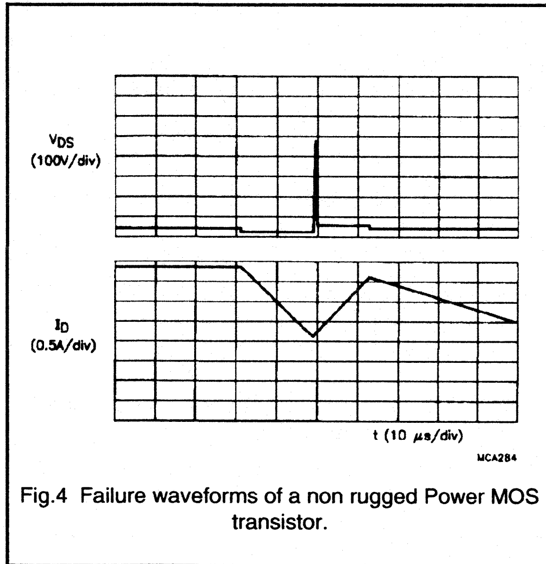


Fig.4 Failure waveforms of a non rugged Power MOS transistor.

The performance of a non-rugged device in response to the avalanche test is shown in Fig.4. The drain voltage rises to the avalanche value followed by an immediate collapse to approximately 30 V. This voltage is typical of the sustaining voltage during Second Breakdown of a bipolar transistor, [1]. The subsequent collapse to zero volts after 12 µS signifies failure of the device. The transistor shown here was only able to dissipate a few micro joules at a very low current if a failure of this type was to be avoided.

Characteristics of a rugged Power MOS.

i) The energy limitation of a rugged device

The power waveform for a BUK627-500B (500 V, 0.8 Ohm) tested at a peak current of 15 A is presented in Fig.5.

The area within the triangle represents the maximum energy that this particular device type may sustain without failure at the above current. Fig.6 shows the junction temperature variation in response to the power pulse, calculated from the convolution integral as shown in equation 4.

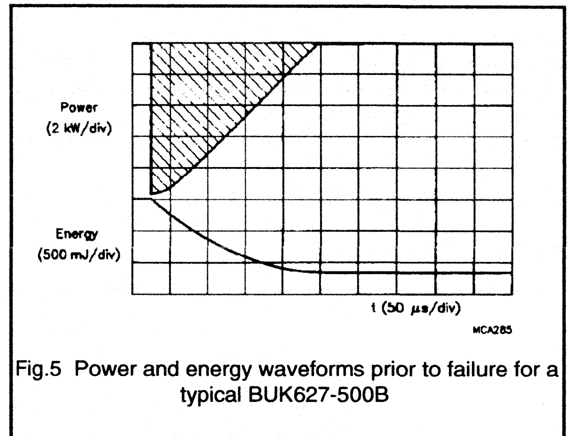


Fig.5 Power and energy waveforms prior to failure for a typical BUK627-500B

$$T_j(t) = \int_{\tau=0}^{\tau=t} P(t-\tau) Z_{th}(\tau) d\tau \qquad (4)$$

where $Z_{th}(\tau)$ = transient thermal impedance.

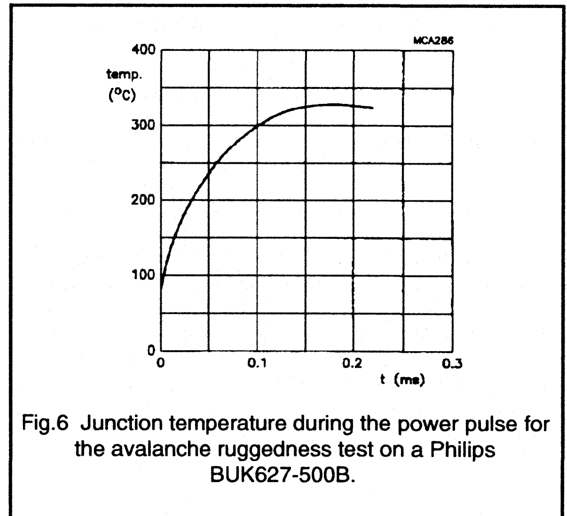


Fig.6 Junction temperature during the power pulse for the avalanche ruggedness test on a Philips BUK627-500B.

Equation 4 predicts that the junction temperature will pass through a maximum of 325 ˚C during the test. The calculation of $Z_{th}(t)$ assumes that the power dissipation is uniform across the active area of the device. When the device operates in the avalanche mode the power will be dissipated more locally in the region of the p-n junction where the multiplication takes place. Consequently a local temperature above that predicted by equation 4 is likely to be present within the device.

Work on bipolar transistors [2] has shown that at a temperature of the order of 400 °C, the voltage supporting p-n region becomes effectively intrinsic as a result of thermal multiplication, resulting in a rapid collapse in the terminal voltage. It is probable that a similar mechanism is responsible for failure of the Power MOS with a local temperature approaching 400 °C resulting in a device short circuit. A subsequent rapid rise in internal temperature will result in eventual device destruction.

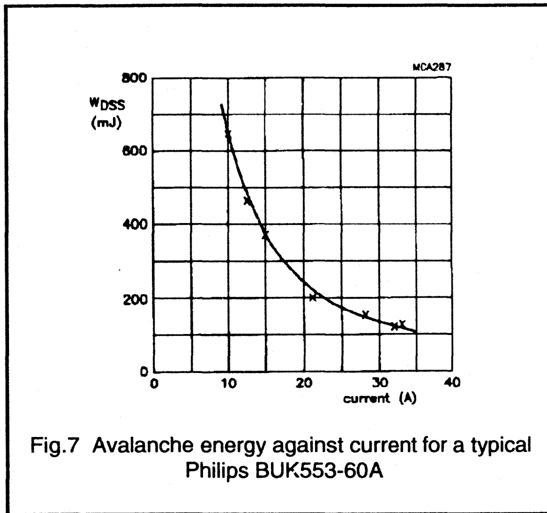


Fig.7 Avalanche energy against current for a typical Philips BUK553-60A

Clearly the rise in T_j is a function of the applied power waveform which is in turn related to circuit current, avalanche voltage of the device and duration of the energy pulse. Thus the energy required to bring about device failure will vary as a function of each of these parameters. The ruggedness of Power MOSFETS of varying crystal size and voltage specification together with dependence on circuit current is considered below.

ii) Sustainable avalanche energy as a function of current.

The typical avalanche energy required to cause device failure is plotted as a function of peak current in Fig.7 for a BUK553-60A (60 V, 0.085 Ohm Logic Level device). This result was obtained through destructive device testing using the circuit of Fig.2 and a variety of inductor values.

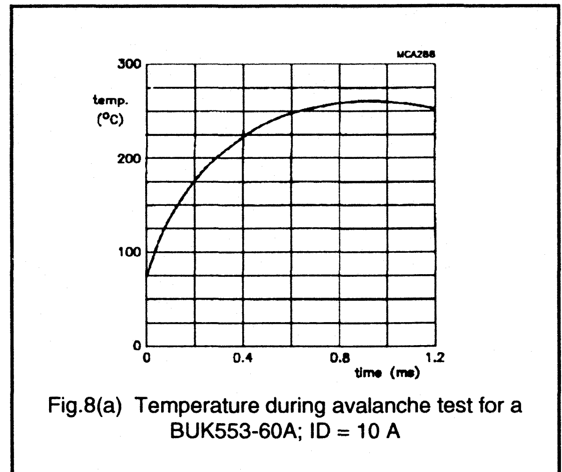


Fig.8(a) Temperature during avalanche test for a BUK553-60A; ID = 10 A

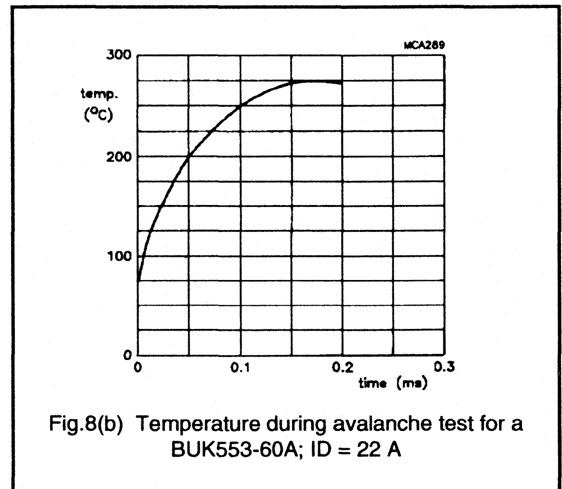
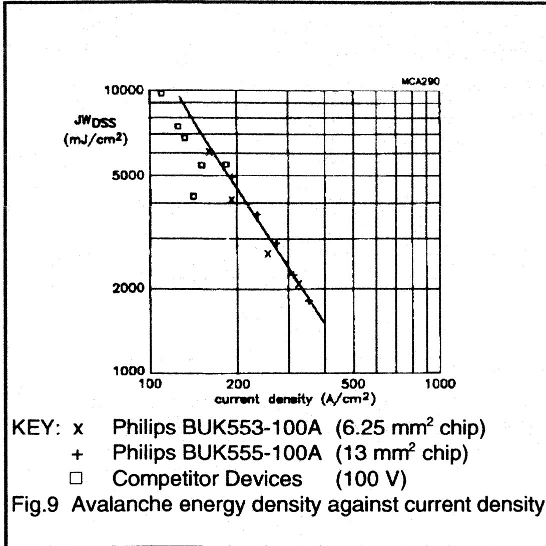


Fig.8(b) Temperature during avalanche test for a BUK553-60A; ID = 22 A

The plot shows that the effect of reducing current is to permit greater energy dissipation during avalanche prior to failure. This is an expected result since lower currents result in reduced power dissipation enabling avalanche to be sustained over a longer period. Temperature plots (Fig.8) calculated for the 10 A and 22 A failure points confirm that the maximum junction temperature reached in each case is the same despite the different energy values. (N.B. The critical temperature is again underestimated as previously stated.)

iii) Effect of crystal size.



KEY: x Philips BUK553-100A (6.25 mm^2 chip)
\+ Philips BUK555-100A (13 mm^2 chip)
□ Competitor Devices (100 V)

Fig.9 Avalanche energy density against current density

To enable a fair comparison of ruggedness between devices of various chip size it is necessary to normalise the results. Therefore instead of plotting avalanche energy against current, avalanche energy density and current density become more appropriate axes. Fig.9 shows the avalanche energy density against current density failure locus for two 100 V Philips Power MOS types which are different only in silicon area. Also shown on this plot are two competitor devices of different chip areas (B_{VDSS} = 100 V). This result demonstrates two points:

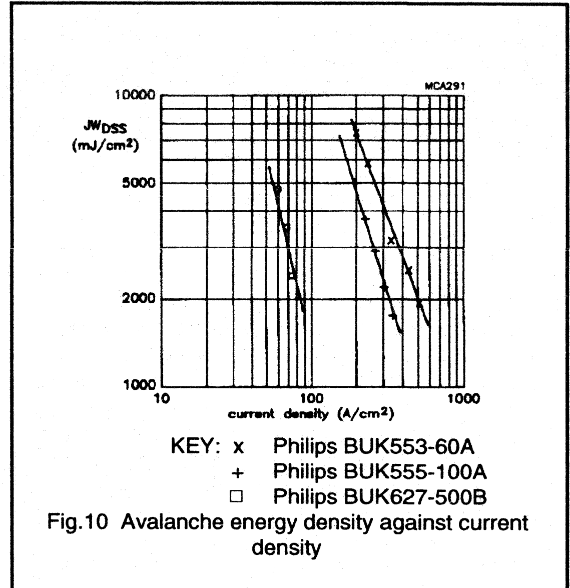
a) the rise in T_j to the critical value for failure is dependent on the power density dissipated within the device as a function of time,

b) the sustainable avalanche energy scales proportional to chip size.

iv) Dependence on the drain source breakdown voltage rating.

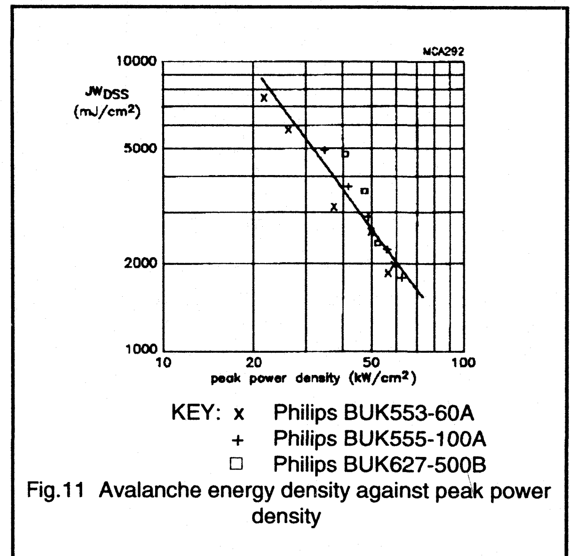
Energy density against current density failure loci are shown for devices of several different breakdown voltages in Fig.10.

Presented in this form it is difficult to assess the relative ruggedness of each device since the current density is reduced for increasing voltage. If instead of peak current density, peak power density is used for the x-axis then comparison is made very simple. The data of Fig.10 has been replotted in Fig.11 in the above manner. Represented in this fashion the ruggedness of each chip appears very similar highlighting that the maximum energy dissipation of a device while in avalanche is dependent only on the power density function.



KEY: x Philips BUK553-60A
\+ Philips BUK555-100A
□ Philips BUK627-500B

Fig.10 Avalanche energy density against current density



KEY: x Philips BUK553-60A
\+ Philips BUK555-100A
□ Philips BUK627-500B

Fig.11 Avalanche energy density against peak power density

Ruggedness ratings.

It should be stressed that the avalanche energies presented in the previous section result in a rise of the junction temperature far in excess of the device rating and in practice energies should be kept within the specification. Ruggedness is specified in data for each device in terms of an unclamped inductive load test maximum condition; recommended energy dissipation at a particular current (usually the rated current of the device).

DEVICE	R_{DSON}	V_{DS}	I_D	W_{DSS}
TYPE	(Ω)	(V)	(A)	(mJ)
BUK552-60A	0.15	60	14	30
BUK552-100A	0.28	100	10	30
BUK553-60A	0.085	60	20	45
BUK553-100A	0.18	100	13	70
BUK627-500B	0.8	500	10	500

The ruggedness rating is chosen to protect against a rise in T_j above the maximum rating. Examples of ruggedness ratings for a small selection of devices are shown above.

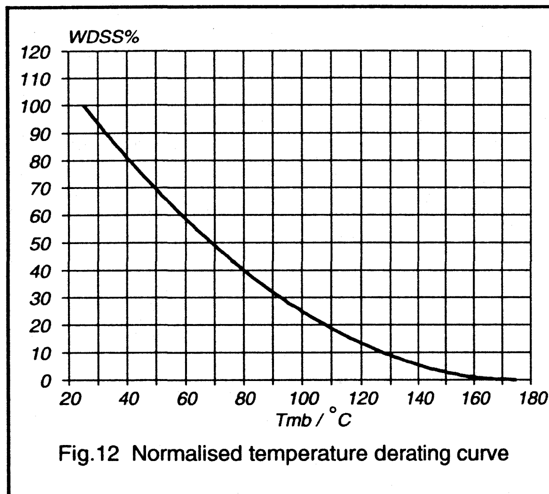


Fig.12 Normalised temperature derating curve

This data is applicable for T_j = 25 C. For higher operating temperatures the permissible rise in junction temperature during the energy test is reduced. Consequently ruggedness needs to be derated with increasing operating temperature. A normalised derating curve for devices with Tj max 175 ˚C is presented in Fig.12.

Performance of a rugged Power MOS device.

The ability of a rugged Power MOS transistor to survive momentary power surges results in excellent device reliability. The response of a BUK553-60A to interference spikes while switching a load is presented below. The test circuit is shown in Fig.13(a) together with the profile of the interference spike in Fig.13(b).

The interference generator produces pulses asynchronous to the switching frequency of the Power MOS. Fig.14 shows the drain voltage and load current response at four instances in the switching cycle. Devices were subjected

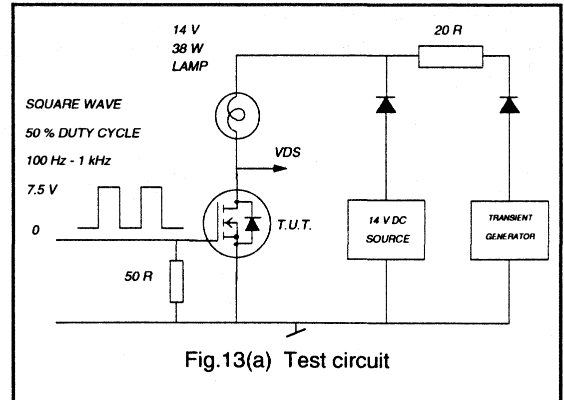


Fig.13(a) Test circuit

to 5000 interference spikes at a frequency of 5 Hz. No degradation in device performance was recorded.

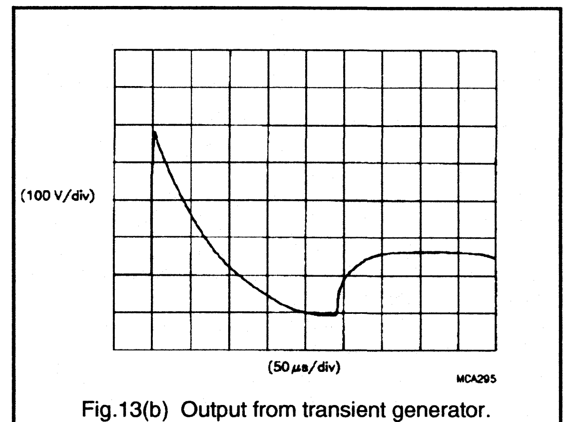
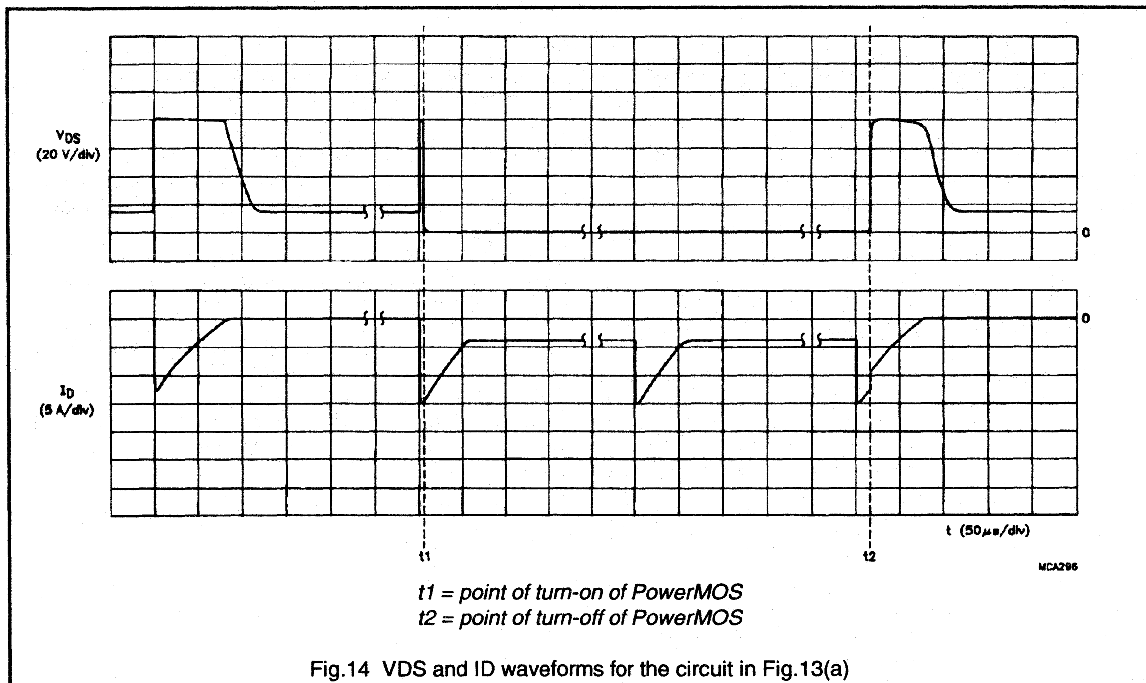


Fig.13(b) Output from transient generator.

Conclusions.

The ability of power MOS devices to dissipate energy in the avalanche mode has been made possible by process optimisation to remove the possibility of turn-on of the parasitic bipolar structure. The failure mechanism of a rugged device is one of excessive junction temperature initiating a collapse in the terminal voltage as the junction area becomes intrinsic. The rise in junction temperature is dictated by the power density dissipation which is a function of crystal size, breakdown voltage and circuit current.

Ruggedness ratings for Philips PowerMOS are chosen to ensure that the specified maximum junction temperature of the device is not exceeded.



t1 = point of turn-on of PowerMOS
t2 = point of turn-off of PowerMOS

Fig.14 VDS and ID waveforms for the circuit in Fig.13(a)

References.

1. DUNN and NUTTALL, An investigation of the voltage sustained by epitaxial bipolar transistors in current mode second breakdown. Int.J.Electronics, 1978, vol.45, no.4, 353-372
2. DOW and NUTTALL, A study of the current distribution established in npn epitaxial transistors during current mode second breakdown. Int.J.Electronics, 1981, vol.50, no.2, 93-108

1.2.9 Electrostatic Discharge (ESD) Considerations

Charge accumulates on insulating bodies and voltages as high as 20,000 V can be developed by, for example, walking across a nylon carpet. Electrically the insulator can be represented by many capacitors and resistors connected as shown in Fig. 1. The value of the resistors is large and as a consequence it is not possible to discharge an insulator by connecting it straight to ground. An ion source is necessary to discharge an insulator.

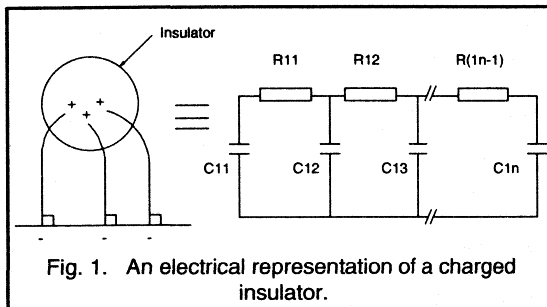


Fig. 1. An electrical representation of a charged insulator.

Since MOSFETs have a very high input impedance, typically > 10^9 Ohms at dc, there is a danger of static electricity building up on the gate source capacitance of the MOSFET. This can lead to damage of the thin gate oxide. There are two ways in which the voltage across the gate source terminals of a MOSFET can be increased to its breakdown voltage by static electricity.

Firstly a charged object can be brought into contact with the MOSFET terminals or with tracks electrically connected to the terminals. This is represented electrically by Fig. 2. Secondly charge can be induced onto the terminals of the MOSFET. Electrically this can be represented by the circuit in Fig. 3.

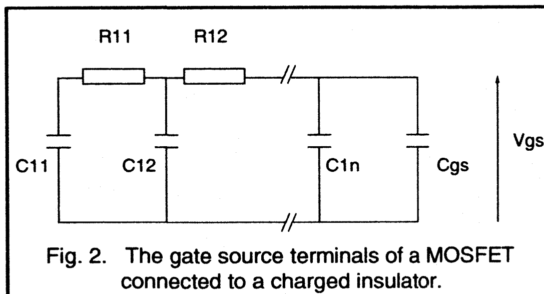


Fig. 2. The gate source terminals of a MOSFET connected to a charged insulator.

From Figs. 2 and 3, it can be seen that, as the total area of the gate source region increases then the sensitivity of the devices to ESD will decrease. Hence power MOSFETs are less prone to ESD than CMOS ICs. Also, for a given voltage rating, MOSFETs with a larger die area (i.e. the devices with lower on-resistance) are less probe to ESD than smaller dice.

To prevent the destruction of MOSFETs through ESD a two pronged approach is necessary. Firstly it is important to minimise the build up of static electricity. Secondly measures need to be taken to prevent the charging up of the input capacitance of MOSFETs by static electric charges.

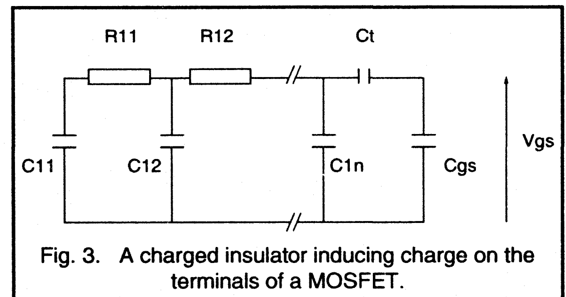


Fig. 3. A charged insulator inducing charge on the terminals of a MOSFET.

In the Philips manufacturing facilities many precautions are taken to prevent ESD damage and these are summarised below.

Precautions taken to prevent the build up of static electricity

1. It is important to ensure that personnel working with MOSFETs are aware of the problems and procedures that have to be followed. This involves the training of staff. Areas in which MOSFETs are handled are designated Special Handling Areas (SHA) and are clearly marked as such. Checks are made every month that anti-static rules are being rigourously implemented.

2. Some materials are more prone to the build up of static electricity than others (e.g. polyester is worse than cotton). Therefore it is important to minimise the use of materials that enhance the likelihood of build up of static electricity. Materials best avoided are acetate, rayon and polyester. The wearing of overclothing made from polycotton with 1% stainless steel fibre is one solution. In clean rooms nylon overalls which have been antistatically treated are worn. The use of insulating materials is avoided.

3. Work benches and floors are covered in a static dissipative material and connected to a common earth. A high conductive material is not used since it would create an electric shock hazard and cause too rapid a discharge of charged material. From the point of view of ESD materials can be classified according to their conductivity as shown below.

insulator (>10^{14} ohm/square)

antistatic (10^{9} - 10^{14} Ohm/square)

static dissipative (10^{5} - 10^{9} Ohm/square)

conductor (<10^{5} Ohm/square).

4. Conducting straps are used to electrically connect personnel to the point of common earthing. This prevents the build up of static charge on staff. The connection is static dissipative to prevent an electric shock hazard.

5. Air plays an important part in the build up of static electricity.

This is particularly troublesome in a dry atmosphere.

Many of the techniques mentioned above are referred to in BS5783.

Precautions taken to prevent damage to MOSFETs by electrostatic build up of charge

1. When MOSFETs are being transported or stored they should be in antistatic containers. These containers should be totally enclosed to prevent charges being induced onto the terminals of devices.

2. If MOSFETs have to be left out on the bench, e.g. during a test sequence, they should be in sockets which have the gate and source pins electrically connected together.

The precautions that should be taken at the customers' premises are the same as above. It should be remembered that whenever a MOSFET is touched by someone there is a danger of damage. The precautions should be taken in every area in which MOSFETs are tested or handled. In addition where devices are soldered into circuits with a soldering iron an earthed bit should always be used.

The probability of device destruction caused by ESD is low even if only the most rudimentary precautions are taken. However without such precautions and with large numbers of PowerMOS devices now being designed into equipment a few failures would be inevitable. The adoption of the precautions outlined will mean that ESD will no longer be a problem.

1.2.10 Understanding the Data Sheet: PowerMOS

All manufacturers of power MOSFETs provide a data sheet for every type produced. The purpose of the data sheet is primarily to give an indication as to the capabilities of a particular product. It is also useful for the purpose of selecting device equivalents between different manufacturers. In some cases however data on a number of parameters may be quoted under subtly different conditions by different manufacturers, particularly on second order parameters such as switching times. In addition the information contained within the data sheet does not always appear relevant for the application. Using data sheets and selecting device equivalents therefore requires caution and an understanding of exactly what the data means and how it can be interpreted. Throughout this chapter the BUK553-100A is used as an example, this device is a 100 V logic level MOSFET.

Information contained in the Philips data sheet

The data sheet is divided into 8 sections as follows:

* Quick reference data
* Limiting values
* Thermal resistances
* Static characteristics
* Dynamic characteristics
* Reverse diode limiting values and characteristics
* Avalanche limiting value
* Graphical data

The information contained within each of these sections is now described.

Quick reference data

This data is presented for the purpose of quick selection. It lists what is considered to be the key parameters of the device such that a designer can decide at a glance whether the device is likely to be the correct one for the application or not. Five parameters are listed, the two most important are the drain-source voltage V_{DS} and drain-source on-state resistance, $R_{DS(ON)}$. V_{DS} is the maximum voltage the device will support between drain and source terminals in the off-state. $R_{DS(ON)}$ is the maximum on-state resistance at the quoted gate voltage, V_{GS}, and a junction temperature of 25 ˚C. (NB $R_{DS(ON)}$ is temperature dependent, see static characteristics). It is these two parameters which provide a first order indication of the devices capability.

A drain current value (I_D) and a figure for total power dissipation are also given in this section. These figures should be treated with caution since they are quoted for conditions that are rarely attainable in real applications. (See limiting values.) For most applications the usable dc current will be less than the quoted figure in the quick reference data. Typical power dissipations that can be tolerated by the majority of designers are less than 20 W (for discrete devices), depending on the heatsinking arrangement used. The junction temperature (T_J) is usually given as either 150 ˚C or 175 ˚C. It is not recommended that the internal device temperature be allowed to exceed this figure.

Limiting values

This table lists the absolute maximum values of six parameters. The device may be operated right up to these maximum levels however they must not be exceeded, to do so may incur damage to the device.

Drain-source voltage and drain-gate voltage have the same value. The figure given is the maximum voltage that may be applied between the respective terminals. Gate-source voltage, $\pm V_{GS}$, gives the maximum value that may be allowed between the gate and source terminals. To exceed this voltage, even for the shortest period can cause permanent damage to the gate oxide. Two values for the dc drain current, I_D, are quoted, one at a mounting base temperature of 25 ˚C and one at a mounting base temperature of 100 ˚C. Again these currents do not represent attainable operating levels. These currents are the values that will cause the junction temperature to reach its maximum value when the mounting base is held at the quoted value. The maximum current rating is therefore a function of the mounting base temperature and the quoted figures are just two points on the derating curve ,see Fig.1.

The third current level quoted is the pulse peak value, I_{DM}. PowerMOS devices generally speaking have a very high peak current handling capability. It is the internal bond wires which connect to the chip that provide the final limitation. The pulse width for which I_{DM} can be applied depends upon the thermal considerations (see section on calculating currents.) The total power dissipation, P_{tot}, and maximum junction temperature are also stated as for the quick reference data. The P_{tot} figure is calculated from the simple quotient given in equation 1 (see section on safe operating area). It is quoted for the condition where the mounting base temperature is maintained at 25 ˚C. As an example, for the BUK553-100A the P_{tot} figure is 75 W, dissipating this amount of power while maintaining the mounting base at

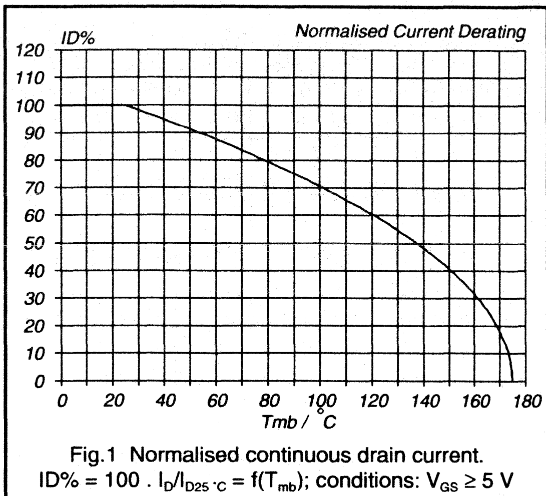


Fig.1 Normalised continuous drain current.
ID% = 100 . $I_D/I_{D25\,^\circ C}$ = f(T_{mb}); conditions: $V_{GS} \geq 5$ V

25 ˚C would be a challenge! For higher mounting base temperatures the total power that can be dissipated is less. Obviously if the mounting base temperature was made equal to the max permitted junction temperature, then no power could be dissipated internally. A derating curve is given as part of the graphical data, an example is shown in Fig.2 for a device with a limiting T_j of 175 ˚C.

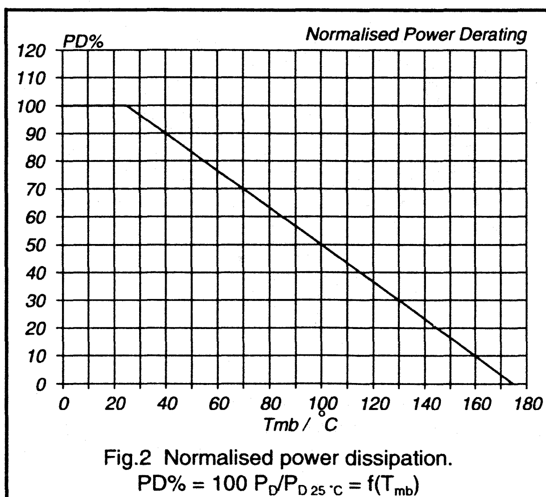


Fig.2 Normalised power dissipation.
PD% = 100 $P_D/P_{D\,25\,^\circ C}$ = f(T_{mb})

Storage temperature limits are also quoted, usually between -40 /-55 ˚C and +150 /+175 ˚C. Both the storage temperature limits and the junction temperature limit are figures at which extensive reliability work is performed by our Quality department. To exceed these figures will cause a reduction in long-term reliability.

Thermal resistance.

For non-isolated packages two thermal resistance values are given. The value from junction to mounting base (R_{thj-mb}) indicates how much the junction temperature will be raised above the temperature of the mounting base when dissipating a given power. Eg a BUK553-100A has a R_{thj-mb} of 2 K/W, dissipating 10 W, the junction temperature will be 20 ˚C above the temperature of its mounting base. The other figure quoted is from junction to ambient. This is a much larger figure and indicates how the junction temperature will rise if the device is NOT mounted on a heatsink but operated in free air. Eg for a BUK553-100A, R_{thj-a} = 60 K/W, dissipating 1 W while mounted in free air will produce a junction temperature 60 ˚C above the ambient air temperature.

For isolated packages, (F-packs) the mounting base (the metal plate upon which the silicon chip is mounted) is fully encapsulated in plastic. Therefore it is not possible to give a thermal resistance figure junction to mounting base. Instead a figure is quoted from junction to heatsink, R_{thj-hs}, which assumes the use of heatsink compound. Care should be taken when comparing thermal resistances of isolated and non-isolated types. Consider the following example:

The non-isolated BUK553-100A has a R_{thj-mb} of 2 K/W. The isolated BUK543-100A has a R_{thj-hs} of 5 K/W. These devices have identical crystals but mounted in different packages. At first glance the non-isolated type might be expected to offer much higher power (and hence current) handling capability. However for the BUK553-100A the thermal resistance junction to heatsink has to be calculated, this involves adding the extra thermal resistance between mounting base and heatsink. For most applications some isolation is used, such as a mica washer. The thermal resistance mounting base to heatsink is then of the order 2 K/W. The total thermal resistance junction to heatsink is therefore

R_{thj-hs} (non isolated type) = R_{thj-mb} + $R_{thmb-hs}$ = 4 K/W

It can be seen that the real performance difference between the isolated and non isolated types will not be significant.

Static Characteristics

The parameters in this section characterise breakdown voltage, threshold voltage, leakage currents and on-resistance.

A drain-source breakdown voltage is specified as greater than the limiting value of drain-source voltage. It can be measured on a curve tracer, with gate terminal shorted to the source terminal, it is the voltage at which a drain current of 250 μA is observed. Gate threshold voltage, $V_{GS(TO)}$, indicates the voltage required on the gate (with respect to the source) to bring the device into its conducting state. For logic level devices this is usually between 1.0 and 2.0 V and for standard devices between 2.1 and 4 V. Useful plots

in the graphical data are the typical transfer characteristics (Fig.3) showing drain current as a function of V_{GS} and the gate threshold voltage variation with junction temperature (Fig.4). An additional plot also provided is the sub-threshold conduction, showing how the drain current varies with gate-source voltage below the threshold level (Fig.5).

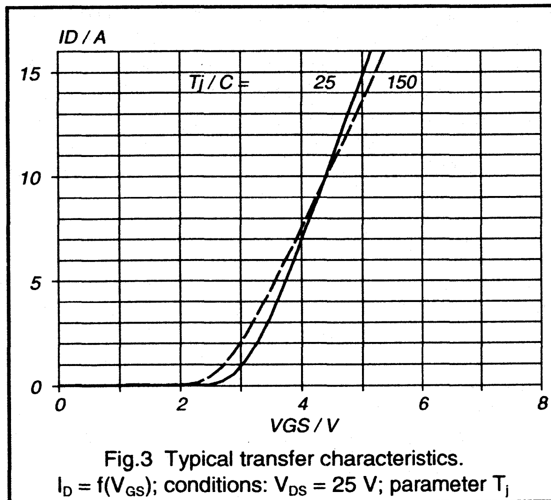


Fig.3 Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

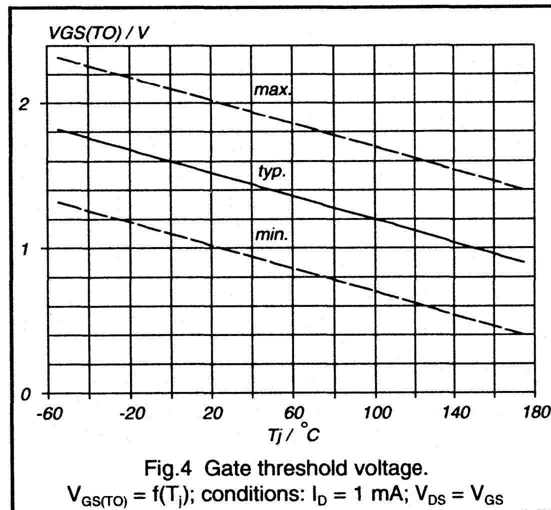


Fig.4 Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

Off-state leakage currents are specified for both the drain-source and gate-source under their respective maximum voltage conditions. Note, although gate-source leakage current is specified in nano-amps, values are typically of the order of a few pico-amps.

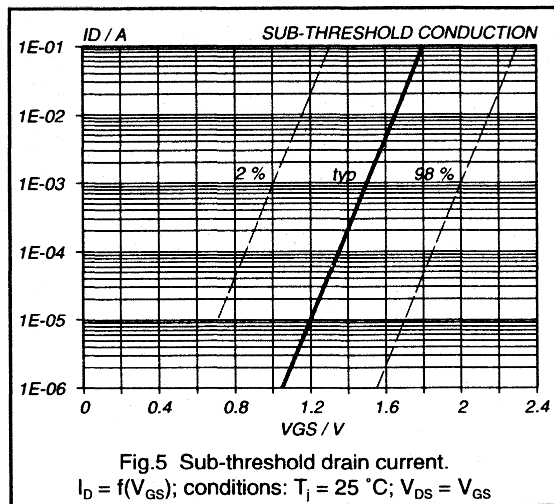


Fig.5 Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

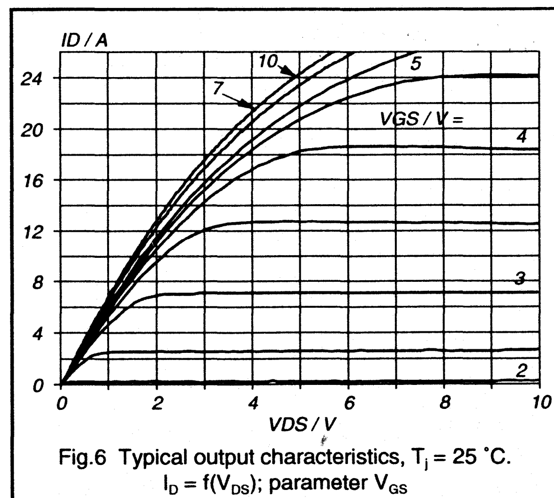


Fig.6 Typical output characteristics, T_j = 25 ˚C.
$I_D = f(V_{DS})$; parameter V_{GS}

The drain-source on-resistance is very important. It is specified at a gate-source voltage of 5 V for logic level FETs and 10 V for a standard device. The on-resistance for a standard MOSFET cannot be reduced significantly by increasing the gate source voltage above 10 V. Reducing the gate voltage will however increase the on-resistance. For the logic level FET, the on-resistance is given for a gate voltage of 5 V, a further reduction is possible however at gate voltages up to 10 V, this is demonstrated by the output characteristics, Fig.6 and on-resistance characteristics, Fig.7 for a BUK553-100A. .

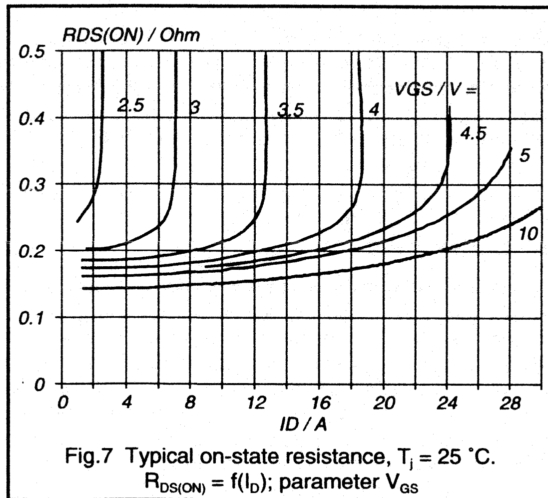


Fig.7 Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

The on-resistance is a temperature sensitive parameter, between 25 ˚C and 150 ˚C it approximately doubles in value. A plot of normalised $R_{DS(ON)}$ versus temperature (Fig.8) is included in each data sheet. Since the MOSFET will normally operate at a T_j higher than 25 ˚C, when making estimates of power dissipation in the MOSFET, it is important to take into account the higher $R_{DS(ON)}$.

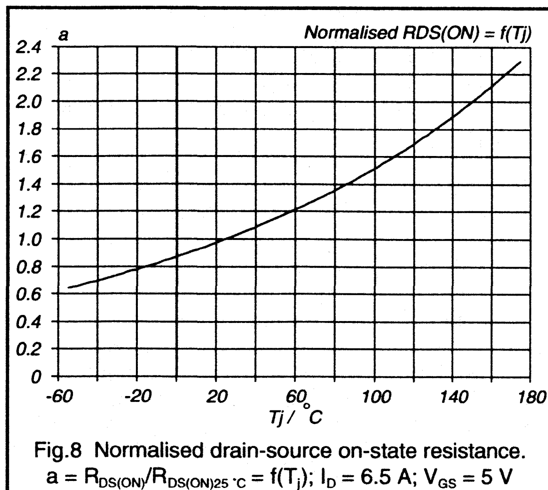


Fig.8 Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 6.5 A; V_{GS} = 5 V

Dynamic Characteristics

These include transconductance, capacitance and switching times.

Forward transconductance, g_{fs}, is essentially the gain parameter which indicates the change in drain current that will result from a fluctuation in gate voltage when the device is saturated. (NB saturation of a MOSFET refers to the flat portion of the output characteristics.) Fig.9 shows how g_{fs} varies as a function of the drain current for a BUK553-100A.

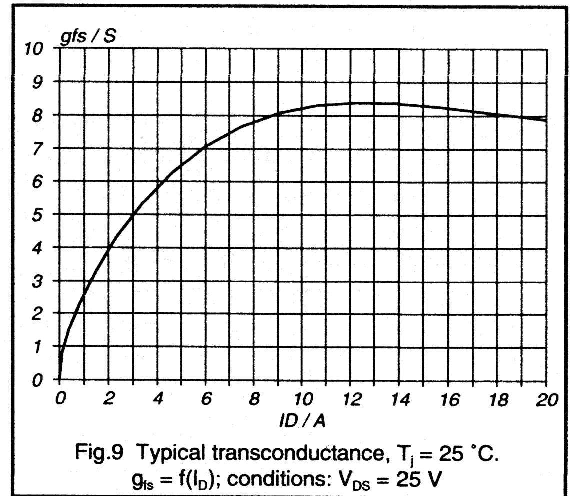


Fig.9 Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

Capacitances are specified by most manufacturers, usually in terms of input, output and feedback capacitance. The values quoted are for a drain-source voltage of 25 V. However this is only part of the story as the MOSFET capacitances are strongly voltage dependent, increasing as drain-source voltage is reduced. Fig.10 shows how these capacitances vary with voltage. The usefulness of the capacitance figures is limited. The input capacitance value gives only a rough indication of the charging required by the drive circuit. Perhaps more useful is the gate charge information an example of which is shown in Fig.11. This plot shows how much charge has to be input to the gate to reach a particular gate-source voltage. Eg. to charge a BUK553-100A to V_{GS} = 5 V, starting from a drain-source voltage of 80 V, requires 12.4 nc. The speed at which this charge is to be applied will give the gate circuit current requirements. More information on MOSFET capacitance is given in chapter 1.2.2.

Resistive load switching times are also quoted by most manufacturers, however extreme care should be taken when making comparisons between different manufacturers data. The speed at which a power MOSFET can be switched is essentially limited only by circuit and package inductances. The actual speed in a circuit is determined by how fast the internal capacitances of the MOSFET are charged and discharged by the drive circuit. The switching times are therefore extremely dependent on the circuit conditions employed; a low gate drive resistance will provide for faster switching and vice-versa. The Philips

data sheet presents the switching times for all PowerMOS with a resistor between gate and source of 50 Ω. The device is switched from a pulse generator with a source impedance also of 50 Ω. The overall impedance of the gate drive circuit is therefore 25 Ω.

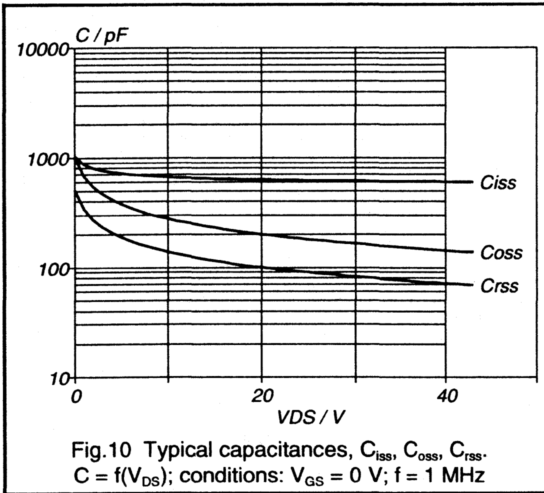


Fig.10 Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
C = f(V_{DS}); conditions: V_{GS} = 0 V; f = 1 MHz

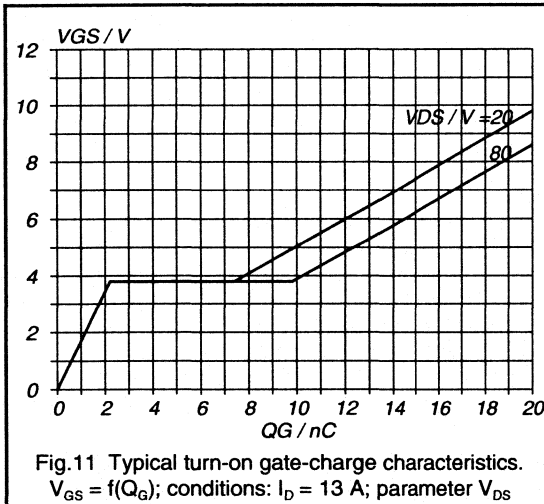


Fig.11 Typical turn-on gate-charge characteristics.
V_{GS} = f(Q_G); conditions: I_D = 13 A; parameter V_{DS}

Also presented under dynamic characteristics are the typical inductances of the package. These inductances become important when very high switching speeds are employed such that large dI/dt values exist in the circuit. Eg. turning-on 30 A within 60 ns gives a dI/dt of 0.5 A/ns. The typical inductance of the source lead is 7.5 nH, from V = -L*dI/dt the potential drop from the source bond pad (point where the source bond wire connects to the chip internally) to the bottom of the source lead would be 3.75 V. Normally a standard device will be driven with a gate-source voltage of 10 V applied across the gate and source terminals, the actual voltage gate to source on the semiconductor however would only be 6.25 V during the turn-on period! The switching speed is therefore ultimately limited by package inductance.

Reverse diode limiting values and characteristics

The reverse diode is inherent in the vertical structure of the power MOSFET. In some circuits this diode is required to perform a useful function. For this reason the characteristics of the diode are specified. The forward currents permissible in the diode are specified as 'continuous reverse drain current' and 'pulsed reverse drain current'. The forward voltage drop of the diode is also provided together with a plot of the diode characteristic, Fig.12. The switching capability of the diode is given in terms of the reverse recovery parameters, t_{rr} and Q_{rr}.

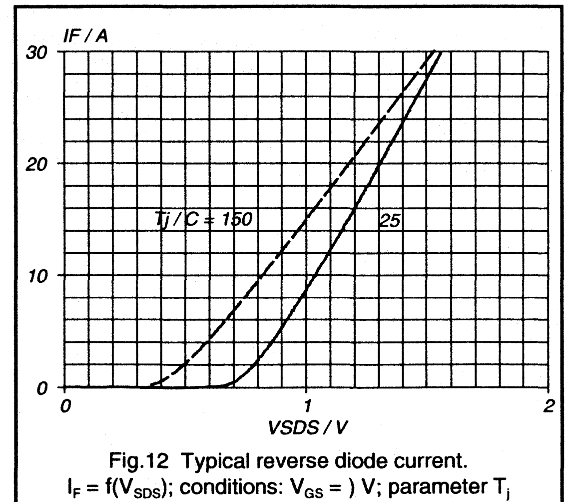


Fig.12 Typical reverse diode current.
I_F = f(V_{SDS}); conditions: V_{GS} =) V; parameter T_j

Because the diode operates as a bipolar device it is subject to charge storage effects. This charge must be removed for the diode to turn-off. The amount of charge stored is given by Q_{rr}, the reverse recovery charge, the time taken to extract the charge is given by t_{rr}, the reverse recovery time. NB. trr depends very much on the -dI_f/dt in the circuit, t_{rr} is specified in data at 100 A/µs.

Avalanche limiting value

This parameter is an indication as to the ruggedness of the product in terms of its ability to handle a transient overvoltage, ie the voltage exceeds the drain-source voltage limiting value and causes the device to operate in an avalanche condition. The ruggedness is specified in

terms of a drain-source non-repetitive unclamped inductive turn-off energy at a mounting base temperature of 25 ˚C. This energy level must be derated at higher mounting base temperatures as shown in Fig.13. NB. this rating is non-repetitive which means the circuit should not be designed to force the PowerMOS repeatedly into avalanche. This rating is only to permit the device to survive if exceptional circuit conditions arise such that a transient overvoltage occurs. (A more detailed explanation of Ruggedness is given in chapter 1.2.8.)

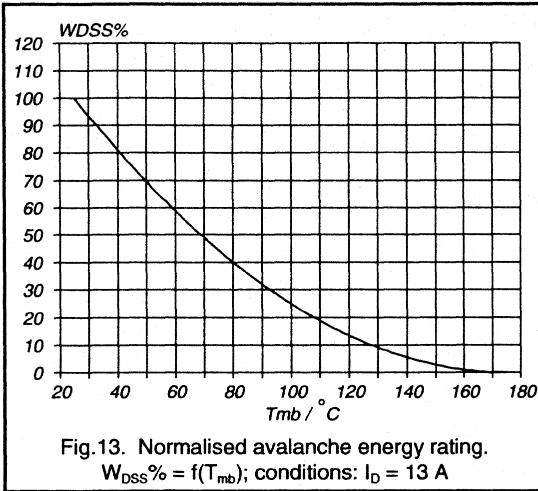


Fig.13. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 13$ A

Safe Operating Area

A plot of the safe operating area is presented for every PowerMOS type. Unlike bipolar transistors a PowerMOS exhibits no second breakdown mechanism. The safe operating area is therefore simply defined from the power dissipation that will cause the junction temperature to reach the maximum permitted value.

Fig.14 shows the SOA for a BUK553-100. The area is bounded by the limiting drain source voltage, limiting current values and a set of constant power curves for various pulse durations. The plots in data are all for a mounting base temperature of 25 ˚C. The constant power curves therefore represent the power that raises the junction temperature by an amount $T_{jmax} - T_{mb}$, ie. 150 ˚C for a device with a limiting T_j of 175 ˚C and 125 ˚C for a device with a limiting T_j of 150 ˚C. . Clearly in most applications the mounting base temperature will be higher than 25 ˚C, the SOA would therefore need to be reduced. The maximum power curves are calculated very simply. The dc curve is based upon the thermal resistance junction to mounting base (junction to heatsink in the case of isolated packages), which is substituted into equation 1. The curves for pulsed operation assume a single shot pulse and instead of thermal resistance, a value for transient thermal impedance is used. Transient thermal impedance is supplied as graphical data for each type, an example is shown in Fig.15. For calculation of the single shot power dissipation capability, a value at the required pulse width is read from the D = 0 curve and substituted in to equation 2. (A more detailed explanation of transient thermal impedance and how to use the curves can be found in chapter 7.)

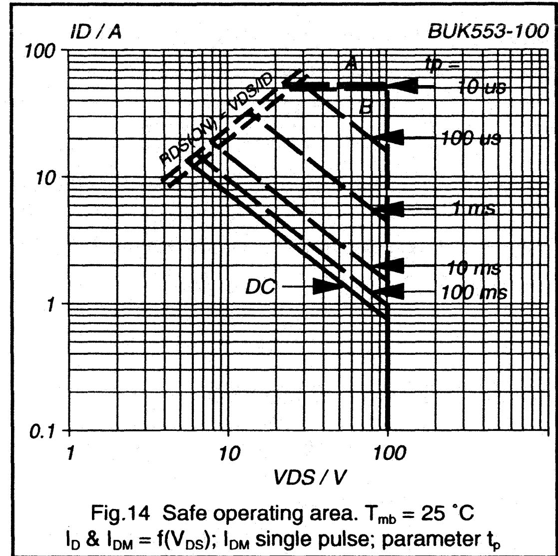


Fig.14 Safe operating area. $T_{mb} = 25$ ˚C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

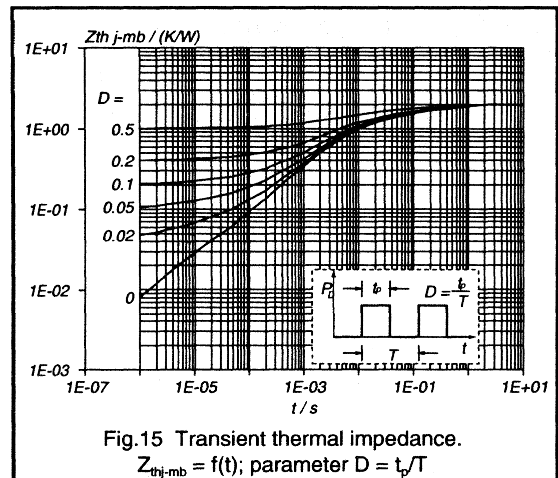


Fig.15 Transient thermal impedance.
$Z_{thj-mb} = f(t)$; parameter $D = t_p/T$

$$P_{tot(dc)} = \frac{T_{jmax} - T_{mb}}{R_{thj-mb}} \quad (1)$$

$$P_{tot\,(pulse)} = \frac{T_{jmax} - T_{mb}}{Z_{thj-mb}} \qquad 2$$

Examples of how to calculate the maximum power dissipation for a 1 ms pulse are shown below. Example 1 calculates the maximum power assuming a T_j of 175 ˚C and T_{mb} of 25 ˚C. This power equates to the 1 ms curve on the SOA plot of Fig.14. Example 2 illustrates how the power capability is reduced if T_{mb} is greater than 25 ˚C.

Example 1: 1 ms pulse at 25 ˚C for a BUK553-100A

Z_{th} = 0.32 K/W, T_{jmax} = 175 ˚C, T_{mb} = 25 ˚C

$$P_{max\,(1\,ms\,pulse)} = \frac{175-25}{0.32} = 469\,W$$

The 469 W line is observed on Fig.13, (4.69 A @ 100 V and 15.6 A @ 30 V etc)

Example 2: 1 ms pulse at 75 ˚C for a BUK553-100A

Z_{th} = 0.32 K/W, T_{jmax} = 175 ˚C, T_{mb} = 75 ˚C

$$P_{max\,(1\,ms\,pulse)} = \frac{175-75}{0.32} = 312\,W$$

Therefore with a mounting base temperature of 75 ˚C the maximum permissible power dissipation is reduced by one third compared with the 25 ˚C value on the SOA plot.

Calculating Currents

The current ratings quoted in the data sheet are derived directly from the maximum power dissipation.

$$I_D(@T_{mb})^2 \cdot R_{DS(ON)}(@T_{jmax}) = P_{tot} \qquad 3$$

substituting for P_{tot} from equation 1

$$I_D(@T_{mb}) = \left\{ \frac{T_{jmax} - T_{mb}}{R_{thj-mb} \cdot R_{DS(ON)}(@T_{jmax})} \right\}^{\frac{1}{2}} \qquad 4$$

To calculate a more realistic current it is necessary to replace T_{jmax} in equation 4 with the desired operating junction temperature and T_{mb} with a realistic working value. It is generally recommended that devices are not operated continuously at T_{jmax}. For reasons of long term reliability, 125 ˚C is a more suitable junction operating temperature. A value of T_{mb} between 75 ˚C and 110 ˚C is also a more typical figure.

As an example a BUK553-100A is quoted as having a dc current rating of 13 A. Assuming a T_{mb} of 100 ˚C and operating T_j of 125 ˚C the device current is calculated as follows:

From Fig.8

$$R_{DS(ON)}(@\,125^oC) = 1.75 \cdot R_{DS(ON)}(@\,25^oC) = 1.75 \cdot 0.18 = 0.315\,\Omega$$

R_{thj-mb} = 2 K/W, using equation 4

$$I_D = \left\{ \frac{25}{2 \cdot 0.315} \right\}^{\frac{1}{2}} = 6.3\,A$$

The device could therefore conduct 6.3 A under these conditions which equates to a 12.5 W power dissipation.

Conclusions

The most important information presented in the data sheet is the on-resistance and the maximum voltage drain-source. Current values and maximum power dissipation values should be viewed carefully since they are only achievable if the mounting base temperature is held to 25 ˚C. Switching times are applicable only for the specific conditions described in the data sheet, when making comparisons between devices from different manufacturers, particular attention should be paid to these conditions.

High Voltage Bipolar Transistor

1.3.1 Introduction To High Voltage Bipolar Transistors

This section introduces the bipolar high voltage transistor and discusses its construction and technology. Specific transistor properties will be analysed in more detail in subsequent sections and in Chapter 2, section 2.1.2.

Basic characteristics

High voltage transistors are almost exclusively used as electronic switches. Therefore, the characteristics of these devices are given for the on-state, the off-state and the transition between the two i.e. turn-on and turn-off.

The relative importance of the ratings V_{CESmax} and V_{CEOmax} usually depends on the converter topology. In a half bridge converter, for instance, the rated V_{CEOmax} is the dominant factor, whilst in a forward converter V_{CESmax} is important. Which rating is most applicable may also depend on whether a slow rise network or snubber is applied (see section 1.3.3).

In the on state both the saturation properties and the switching times are given at a specific collector current called the collector saturation current I_{Csat}. It is this current which is normally considered to be the practical working current of the device. If this device is used at higher currents the total dissipation may be too high, while at low currents the storage time is long. At I_{Csat} the best compromise is present for the total spread of products. The value of the base current used to specify the saturation and switching properties of the device is called I_{Bsat} which is also an important design parameter.

The high voltage transistor chip

A drawing of a high voltage transistor, in this case a fully isolated SOT186 F-pack, is shown in Fig.1 with the plastic encapsulation stripped away. One can see the three leads, two of which are connected with wires to the transistor chip. The third lead makes contact with the mounting base on which the crystal is soldered, enabling good thermal contact with a heatsink. It is the transistor package which basically determines the thermal properties of the device. The electrical properties are mainly determined by the design of the chip inside.

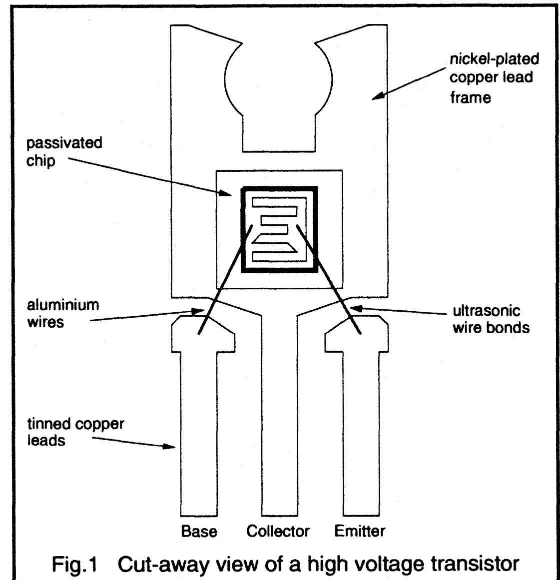


Fig.1 Cut-away view of a high voltage transistor

A cross-section of a transistor chip is given in Fig.2. Here the transistor structure can be recognised with the emitter and the base parts on the surface and the collector connected to the mounting base. The thickest part in the drawing is the collector N⁻-area across which the high voltage will be supported in the off-state. This layer is of prime importance in the determination of the properties of the device. Below the N⁻-layer an extra N⁺-layer is needed for a good electrical contact.

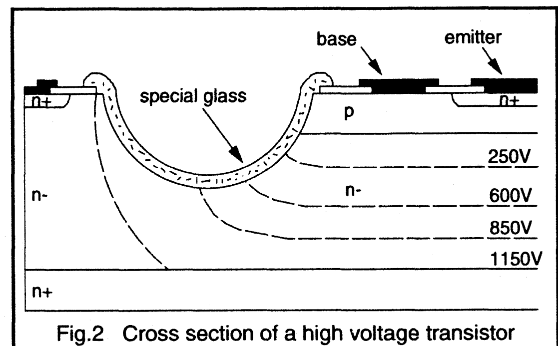


Fig.2 Cross section of a high voltage transistor

Above the collector layer is the base (P) layer, and the emitter (N⁺) layer with their respective metallic contacts on top. It is important to realise that the properties of the device are determined by the active area, this is the area underneath the emitter where the collector current flows and the high voltage can be developed.

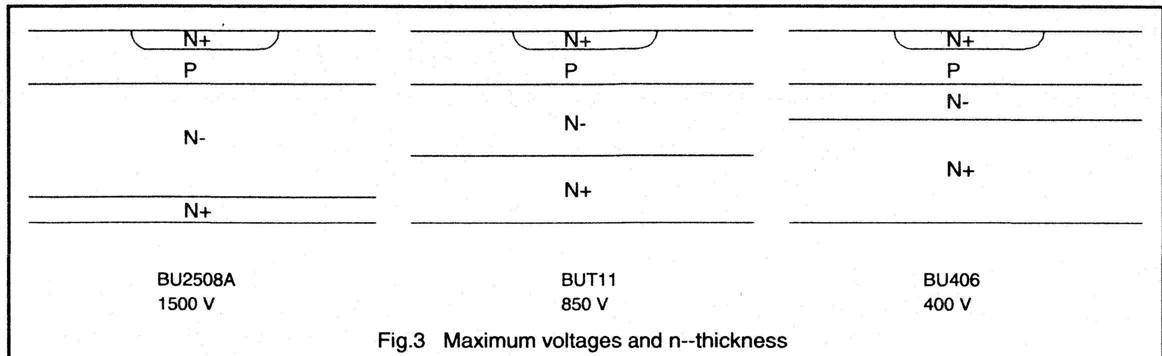


Fig.3 Maximum voltages and n--thickness

In addition to the basic collector-base-emitter structure manufacturers have to add electrical contacts, and special measures are needed at the edges of the crystal to sustain the design voltage. This introduces another very important feature, the high voltage passivation. The function of the passivation, (the example shown here is referred to as glass passivation), is to ensure that the breakdown voltage of the total device is determined by the collector-base structure and not by the construction at the edges. If no special passivation was used the breakdown voltage might be as low as 50% of the maximum value. Manufacturers optimise the high voltage passivation and much work has also been done to ensure that its properties do not change in time.

Technology

There are several ways to make the above structure. The starting material can be an N^--slice where first a diffusion is made in the back, followed by the base and emitter diffusions. This is the well known triple diffused process.

Another way is to start with an N^+-slice on which an N^--layer is grown using epitaxy techniques. If one now does a further two diffusions (P-base and N^+-emitter) one speaks of a double diffused epitaxial process.

The construction where one uses the epi slice to grow a P-layer on top and diffuse an N^+-emitter is referred to as a single diffused epi-base transistor.

All of the above mentioned versions may be called "planar" to distinguish them from the very old fashioned alloy structure which is no longer used. The expression "planar" is also used to indicate the high voltage passivation technique which is being used and some good planar passivation schemes are known. Some manufacturers use the term planar to infer a very fast device but speed is determined by the inner active area of the transistor, not by the passivation.

The question may be asked whether epi-slices are better than triple diffused because since this is the case for diodes. The difference is that the use of epi material for diodes allows a very high degree of "killing" to speed up the devices without the penalty of a higher forward voltage drop.

Transistors are never heavily killed like diodes, because it may ruin the current gain. Basically, there is no difference between the various technologies, provided the doping profile is made the same. The doping profile is important in the deep N^--N^+ junction, for achieving good reverse energy handling capabilities. Epi slices are therefore often made with "buffer layers" for a gradual transition area between the N^--N^+ junction.

Maximum voltage and basic properties

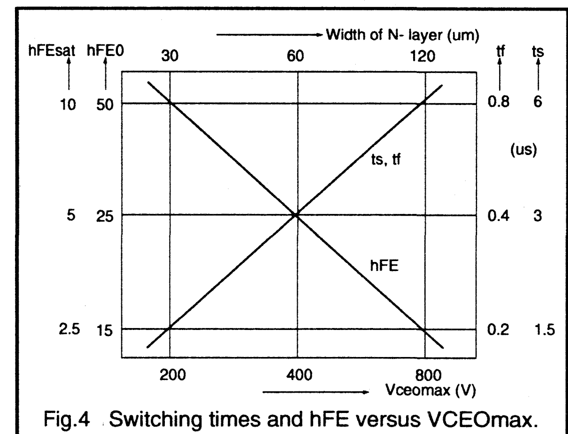


Fig.4 Switching times and hFE versus VCEOmax.

High voltage and low voltage transistors differ primarily in the thickness of the N^--layer. As the thickness and resistivity of this layer is increased, the breakdown voltage goes up as well. The difference between three transistors of different voltages is illustrated in Fig.3.

The BU406 is rated at V_{CESmax} = 400 V, the BUT11 has a V_{CESmax} = 850 V, while the BU2508A can be used up to voltages of 1500 V.

The penalty for increasing the N^--layer however, is a decrease in current gain and an increase in switching times. The graph of Fig.4 points this out by giving both switching times and current gain as a function of the breakdown voltage. These values are to be interpreted as guide-lines to illustrate the effect.

Applications of high voltage transistors

High voltage transistors are mainly used in energy conversion systems. What is common to all these systems, is that a current flows through an inductor, thus storing energy in its' core. When the current is interrupted by turning off the switch, the energy must be transferred one way or the other. Very often the energy is converted into an electrical form e.g. in switch mode power supplies and battery chargers.

A special application is electronic F.L. ballasts where an A.C. voltage is generated to deliver energy to a fluorescent lamp.

Other ways to transfer the energy are A.C. and D.C. motor control where the output is delivered as movement, or induction heating where the output is delivered in the form of heat.

1.3.2 Effects Of Base Drive On Switching Times

The switching processes that take place within a transistor are not always fully understood by designers of power supplies and inverters. This section describes what happens within high-voltage transistors under various base drive conditions.

After a thorough analysis of the charges that are present in a high-voltage transistor it will be described how the switch-off process takes place. Then at various forward and reverse base drive conditions the switching behaviour is discussed in more detail.

The switching process of a transistor

In a high voltage transistor that is in the off-state, there are no charges present. When a high voltage transistor is in the on-state, three charges can be distinguished (see Fig.1).

The first charge Q_B is in the base area and is essential for transistor operation: a collector current will flow only when there is a base charge. The second charge, Q_C, is located in the collector underneath the emitter and causes a low ohmic collector, which makes the collector-emitter voltage low: an increasing Q_C decreases V_{CE}.

The third charge Q_D is located in the collector region underneath the base contact. When the base-collector region becomes forward biased (which happens at very low values of V_{CE}), Q_D rapidly increases when V_{CE} decreases further.

Fig.1 illustrates the charge distribution Q_B, Q_C and Q_D in a forward biased high voltage transistor. The relative influence of the collector-emitter voltage V_{CE} and the collector current I_C is given in Fig.2.

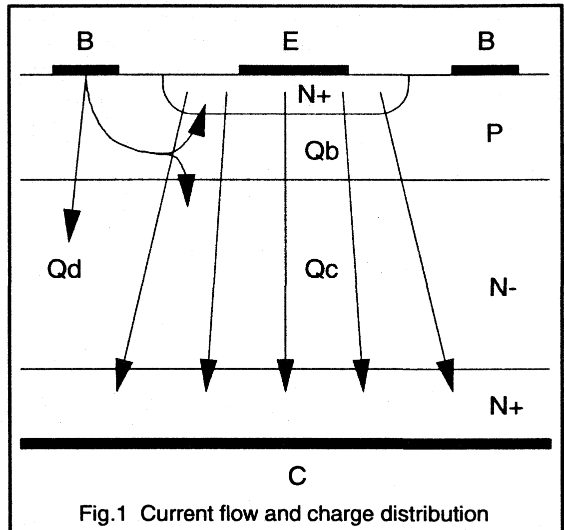


Fig.1 Current flow and charge distribution

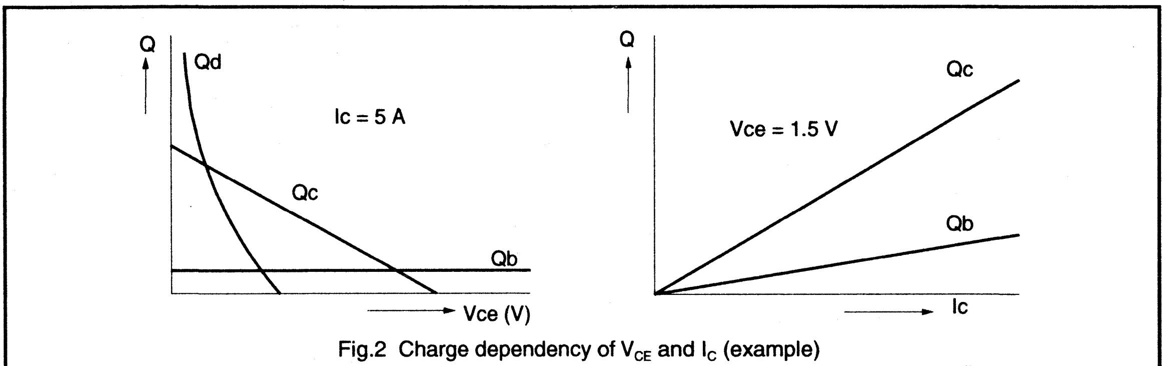


Fig.2 Charge dependency of V_{CE} and I_C (example)

At turn-off the charges must be removed in an active way and it is common practice to apply a negative base current, which pulls the charges out of the transistor. In the process that follows, four phases can be distinguished: the first two during the storage time, the other two during the fall time (see Fig.3).

a. First the negative base current extracts the charge Q_D until it is (about) zero.

b. Then charge is extracted from Q_C, starting from the area underneath the edges of the emitter. Also Q_B will now decrease and the collector current is forced towards the centre of the emitter. As long as Q_B is sufficiently high the collector circuit will force the collector current to flow but V_{CE} must increase because the current density becomes higher. As the emitter current contracts, the negative base current flows through the base resistance underneath the emitter (R_B). The charges Q_C and Q_B now become increasingly located beneath the centre of the emitter and thus have to be extracted through an increasing resistance. Consequently the base-emitter terminal voltage becomes more negative. At the end of the storage time the emitter current is concentrated in the middle of the emitter finger.

c. Fall time begins as soon as Q_B is so low that emitter injection starts to reduce. The emitter current decreases with a speed depending on the rate of change in Q_B: $I_E = 0$ when $Q_B = 0$.

d. A trapped rest-charge Q_R in the collector must still be removed by way of a collector-base current, which appears as a tail in the turn-off wave forms.

The switching waveforms for a BUT11 in a forward converter are given in Fig.4 where the four phases can easily be recognised. (Because of the small base coil used both phases in the fall time appear clearly!).

1 - Removal of Q_D until t = 0.7 us ts (approx)

2 - Q_C and Q_B decrease until t = 1.6 ts us

3 - Removal of Q_B until t = 1.75 us tf

4 - Removal of Q_R until t = 1.85 us tf

Note the course of V_{BE}: first the decrease in voltage due to the base resistance R_B during current contraction and second (because a base coil has been used) the value of V_{BE} which is clamped by the base emitter breakdown voltage of the transistor. It should be remembered that - because breakdown takes place near the surface and not in the active region - this causes no harm to the transistor.

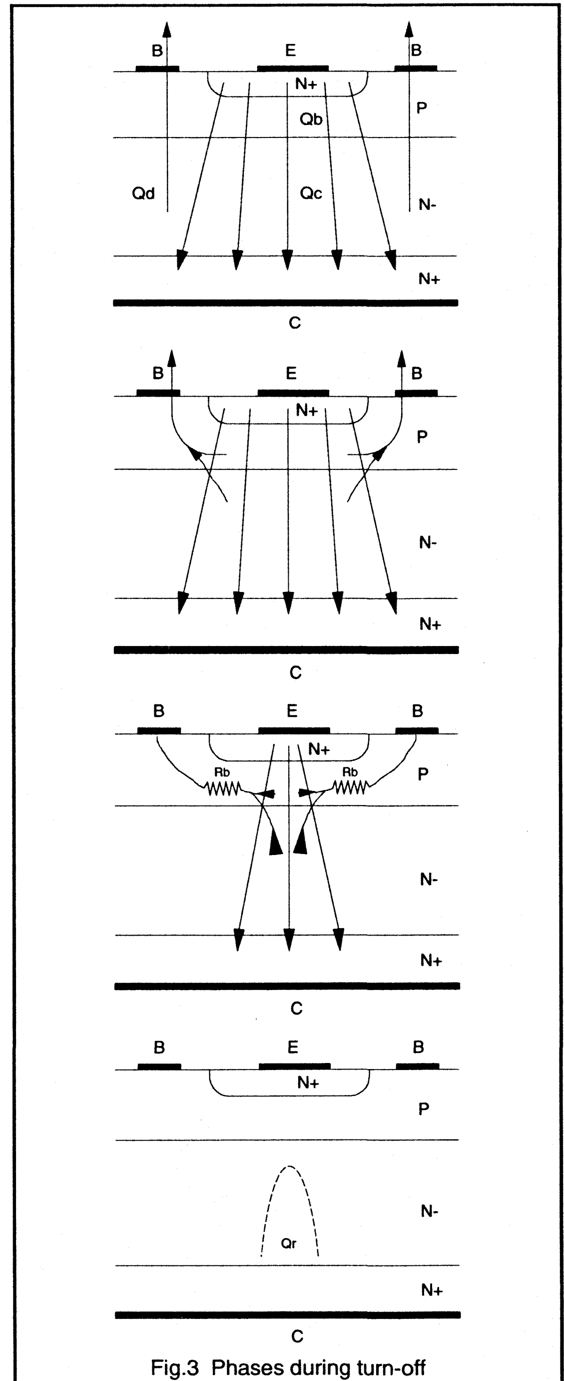


Fig.3 Phases during turn-off

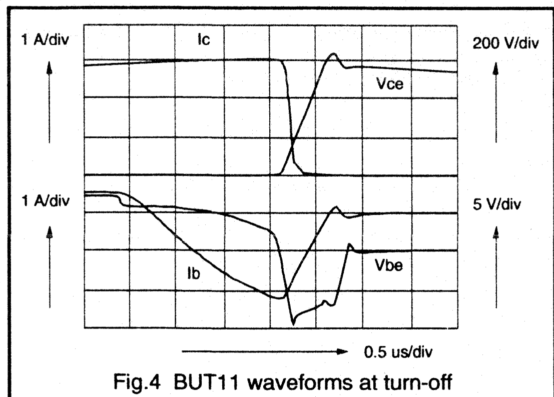


Fig.4 BUT11 waveforms at turn-off

The influence of forward drive on stored charge

Fig.5 shows how, at a fixed value for the collector current I_C, the three charges Q_B, Q_C and Q_D depend upon the collector-emitter voltage. The base charge does not depend upon V_{CE}, it primarily depends upon I_C (see Fig.2). For normal base drive conditions, a satisfactory value for V_{CEsat} is obtained, indicated by N in Fig.5, and moderate values for Q_C and Q_D result.

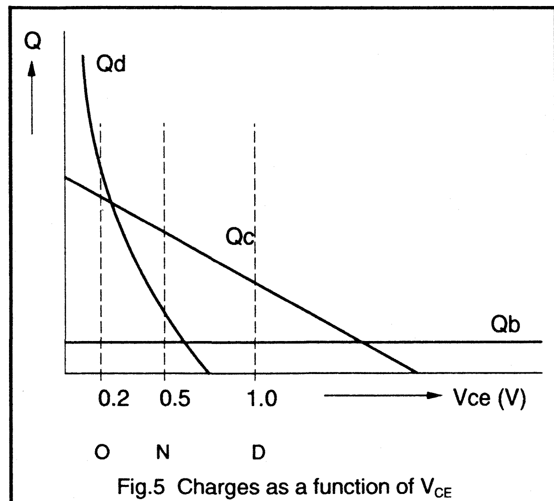


Fig.5 Charges as a function of V_{CE}

When applying a higher base-current than necessary the transistor is said to be overdriven (point O in Fig.5) and both the diode charge Q_B and collector charge Q_C increase. Fig.6 shows results obtained from a computer model which illustrates charge storage as a function of V_{CE}. Here the hole density (p(x)) is given as a function of the depth inside the active area; the doping profile is also indicated. It can be seen that overdrive causes extra holes to be stored near the back of the crystal, known as "deep-hole storage", this is the main reason for the increase in Q_C.

So during overdrive not only Q_D becomes very big but also holes are stored far away from the junction: this thus leads not only to a longer storage time, but also to a large Q_R resulting in tails in the turn-off current!

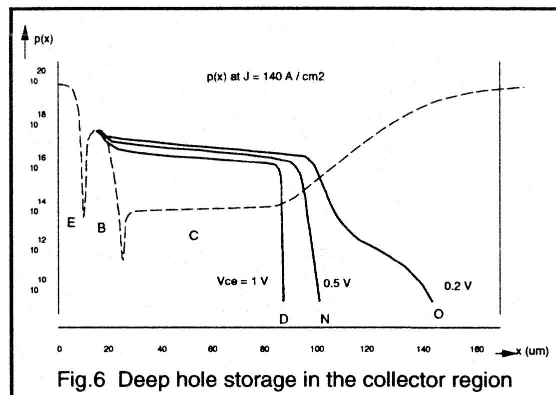


Fig.6 Deep hole storage in the collector region

If a desaturation network is employed (see Fig.7) it appears that not only the collector charge is less, but also that the diode charge equals zero (see D in Figs.5 & 6). When examining the distribution of the charge in the collector region (see Fig.6) one can see that deep hold storage does not appear which means that the charge is located more towards the base-collector junction. This is a nice condition at turn-off because the amount of charge to be removed from the transistor is minimal and furthermore located in a favourable place: desaturation gives short storage and fall times.

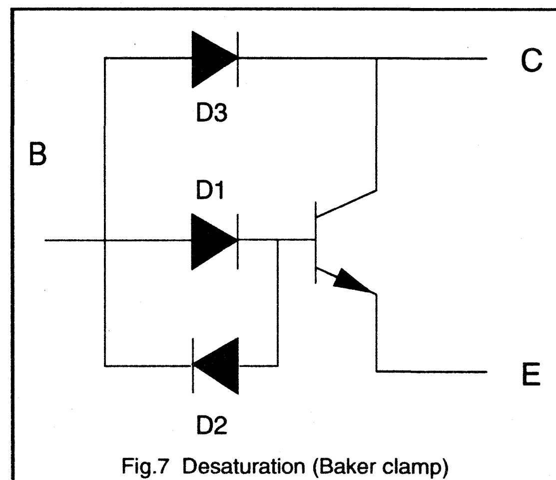


Fig.7 Desaturation (Baker clamp)

It should be clear that the higher the breakdown voltage of the transistor the thicker the n- layer (see Fig.1) and thus the values for Q_D and Q_C will be higher. The experiences obtained with low voltage transistors can therefore not be used for high voltage transistors!

Summarising we can say:

* the higher BVCEO the larger Q_D and Q_C will be.

* during overdrive the diode charge is very high and the collector charge is located deep in the collector region (deep hole storage).

* When desaturated, the diode charge equals zero and there is no deep hole storage: Q_C is located more towards the base-collector region.

Turn-off conditions

Various ways of turning off a high voltage transistor are used but always the base should be switched to a negative supply via an appropriate impedance (3). If this is not done, (ie turn-off is attempted by simply interrupting the base current), very long storage times result and the collector voltage increases, while the collector current falls only slowly. A very high dissipation and thus a short lifetime of the transistor are the result. The charges must be removed using a negative base current!

a) Hard turn-off

The technique widely used, especially for low voltage transistors, is to switch directly to a negative voltage, (see Fig.8). In the absence of a negative supply, this can be achieved with an appropriate R-C network (Fig.8(b)). Also applying an "emitter-drive" (Fig.8(c)) with a large base capacitor in fact is identical to hard-turn-off.

The main drawback is that for high voltage transistors the base charge Q_B is removed rather quickly, so that a high rest charge follows giving a relatively bad fall time and a high dissipation. It depends upon what state the transistor is in (overdriven, desaturated), whether this way of turn-off is sufficient. It also depends upon the kind of transistor that must be switched off. If it is a low voltage transistor (BVCEO~200V) then this will work very well because the charges Q_C and Q_D will be rather low. For transistors with a higher breakdown voltage, hard turn-off will yield the shortest storage time at the cost however of higher turn-off dissipation (longer tf).

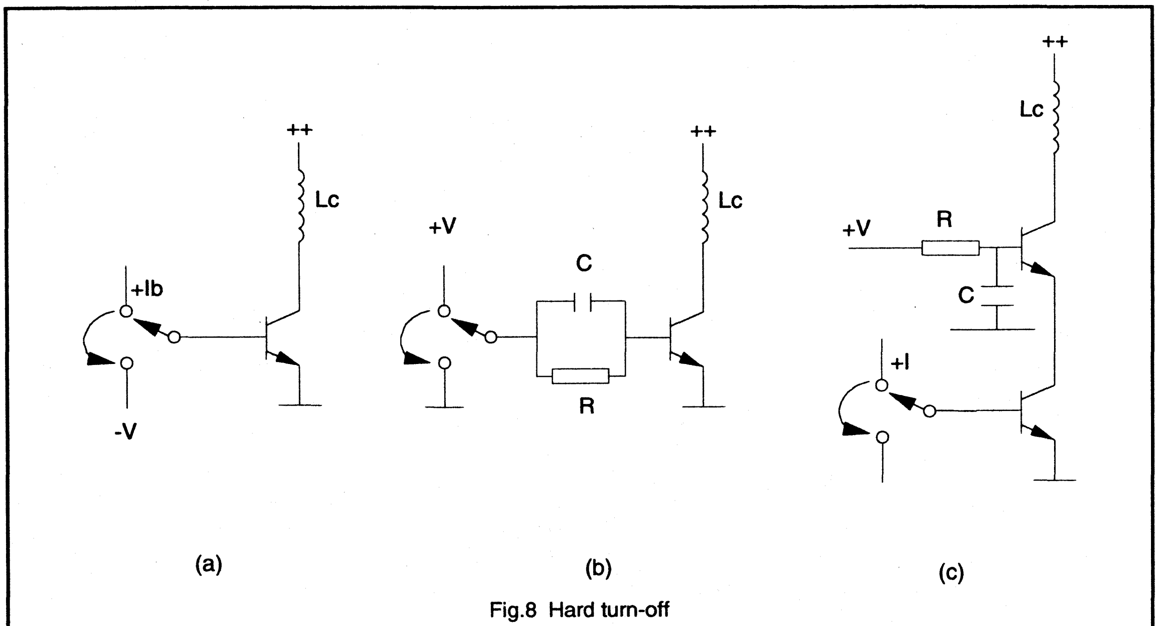


Fig.8 Hard turn-off

b) Smooth turn-off

The trick to properly turn-off a high voltage transistor is to programme a longer storage time, so that Q_D and Q_C can be minimised and then apply a large negative base current yielding a short fall time.

The easiest way to obtain these turn-off requirements is to switch the base to a negative supply via a base coil (see Fig.9).

The base coil gives a constant dI/dt (about) during the storage time. When the fall time begins the negative base current reaches its maximum and the voltage across L_B is such that even the base-emitter junction comes into breakdown (see Fig.4).

An optimum value exists for the base coil: if $L_B = 0$ we have a hard turn-off condition which is not optimal for standard high voltage transistors. If the value of L_B is too high then V_{CE} increases too much during the storage time and so higher losses result (see Fig.10).

For normal converters (fc = 20 to 30 kHz, standard base drive, not overdriven, not desaturated) the following equations give a good indication for the value of L_B.

$$L_B = \frac{(-V_{dr} + V_{BEsat})}{\left(\frac{dI_B}{dt}\right)}$$

with $\frac{dI_B}{dt} \approx 0.5 \cdot I_C \quad (A/\mu s) \quad \text{for} \quad BV_{CEO} = 400V, BV_{CES} = 800V$

and $\frac{dI_B}{dt} \approx 0.15 \cdot I_C \quad (A/\mu s) \quad \text{for} \quad BV_{CEO} = 700V, BV_{CES} = 1500V$

Using $-V_{dr}$ (negative base drive) = 5 Volts, $V_{BE\,sat}$ = 1 Volt and transistors having B_{VCEO} = 400 V it follows:

$$L_B = \frac{12}{I_C} \quad (\mu H) \quad (I_C \quad \text{in Amps})$$

c) Other ways of turn-off

Of course other ways of turn-off are applicable but in general these can be reduced to one of both described methods, or something in between. It must be clear that V_{CEO} has a strong influence: the higher V_{CEO} the longer a storage time must be programmed to achieve proper turn-off. For transistors having a V_{CEO} of, say, 200V or less hard turn-off and the use of a base coil yield comparable losses, so hard turn-off works well. For transistors having V_{CEO} more than 400V hard turn-off is unacceptable because of the resulting tails.

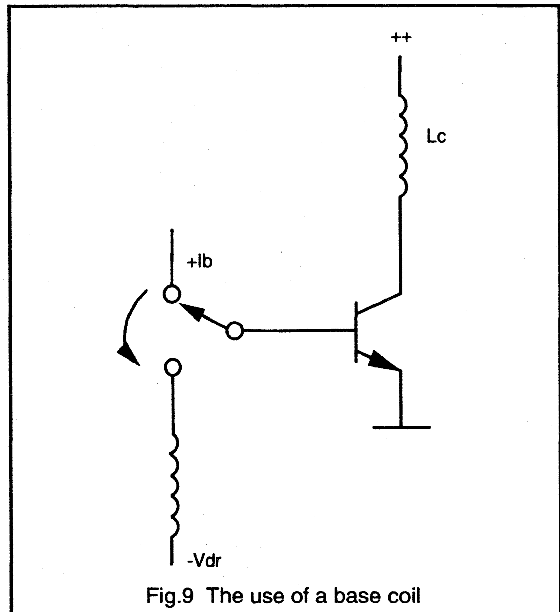


Fig.9 The use of a base coil

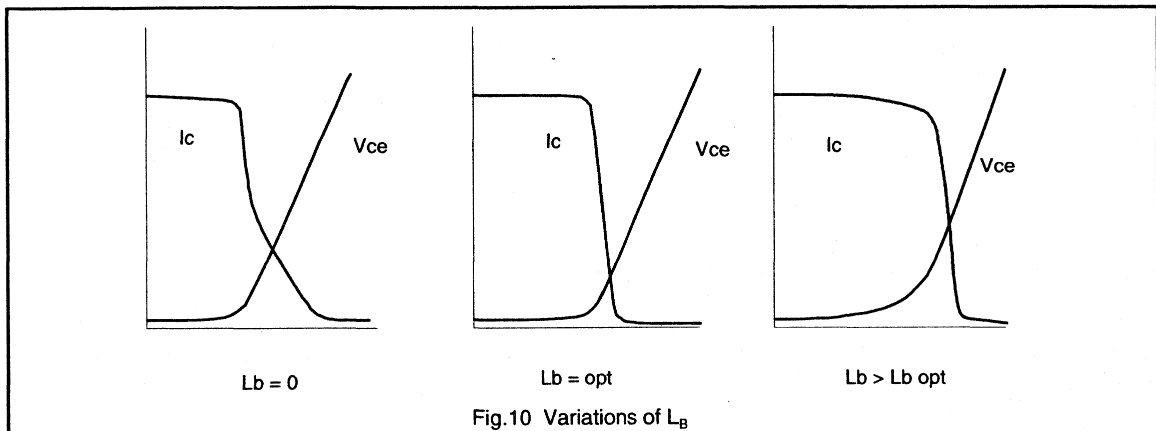


Fig.10 Variations of L_B

Turn-Off for various forward drive conditions

The following paragraphs discuss the influence of hard turn-off and smooth turn-off under standard, desaturated and overdrive conditions.

a) Standard Drive

The optimum I_{BE} at various values of I_C and associated value for L_B is given in Fig.11 for a BUT11.

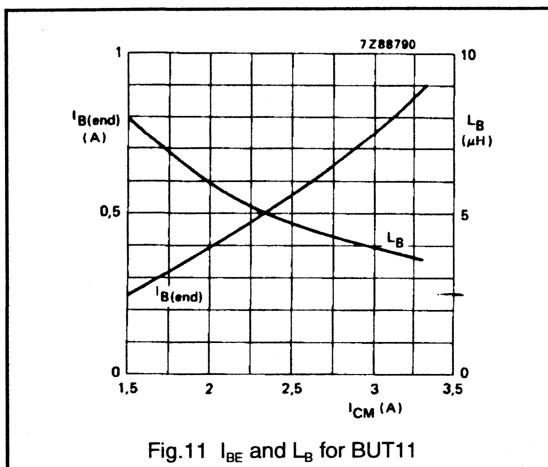


Fig.11 I_{BE} and L_B for BUT11

Deviations from Fig.11 will generally lead to higher power dissipation. If a short storage time is a must in a certain application then L_B can be shorted but this will lead to a long fall time.

Fig.12 compares the use of the advised base coil with hard turn-off.

The reason for the behaviour at hard turn-off is that internal charge is extracted from the base too quickly, while a collector charge is still present (Fig.13). This leads to a large Q_R yielding a considerable tail.

b) Desaturated condition

As has been indicated earlier desaturating a transistor results in less internal charge. Q_D will be zero and Q_C is low and located near the junction. The optimum way of switch-off is to use a base coil having half the value used for standard turn-off yielding a shorter ts and tf. For 400V V_{CEO}-devices (like the Philips BUT range) a harder turn-off can also lead to reasonable results.

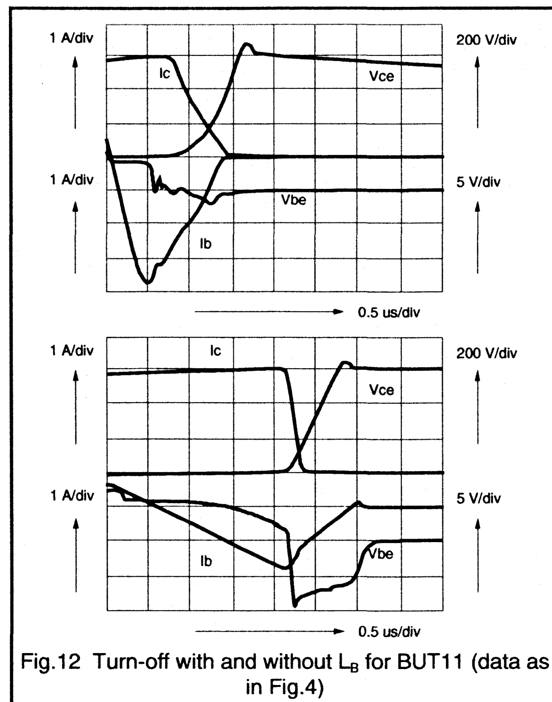


Fig.12 Turn-off with and without L_B for BUT11 (data as in Fig.4)

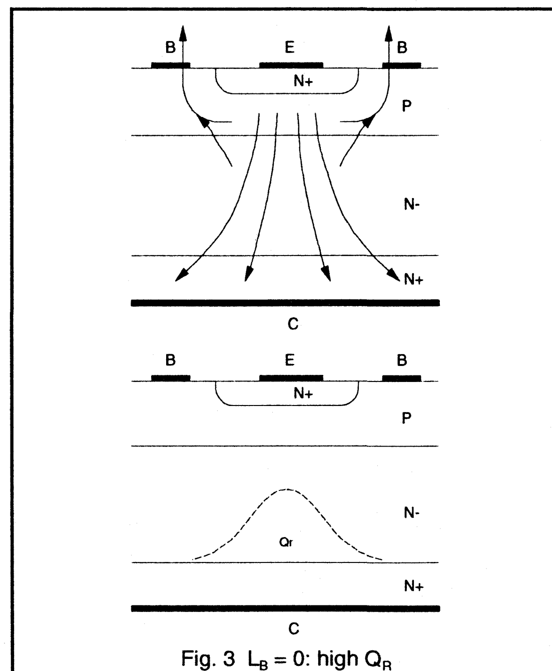


Fig. 3 L_B = 0: high Q_R

Both methods are compared in Fig.13. (NB before turn-off the collector current is slightly higher than the current in the load because of the excess base current flowing through the diode D3 (Fig.7).

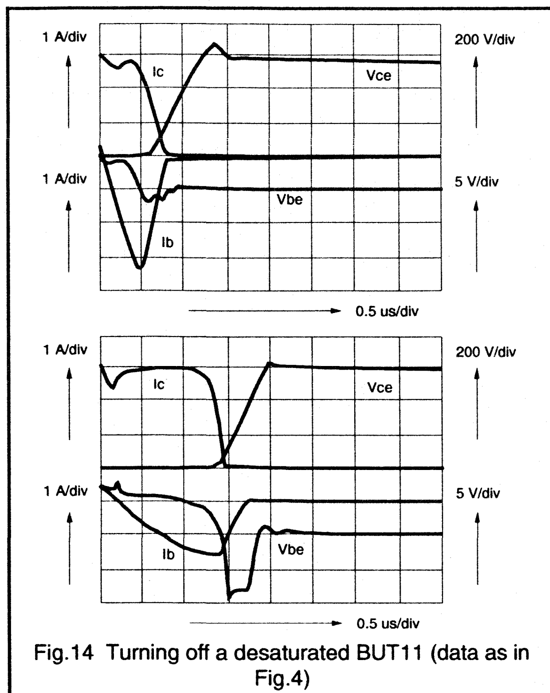


Fig.14 Turning off a desaturated BUT11 (data as in Fig.4)

c) Overdrive situation

When a transistor is severely overdriven the diode charge becomes so large that a considerable tail will result when the advised base coil is used. From the foregoing it should be clear that when hard-turn-off is used with an overdriven transistor the tail even becomes worse and losses higher. Fig.15 speaks for itself, especially when compared with Fig.12. Using larger base coils leads to unacceptably long storage times.

Conclusion

Two ways of turning off a high voltage transistor, hard turn-off and the use of a base coil, were examined in three conditions of the on-state: normal, overdriven and desaturated.

It follows that for transistors having V_{CEO} ~ 400V the use of a base coil yields low losses compared to hard turn-off. As a good approximation the base coil should have the value

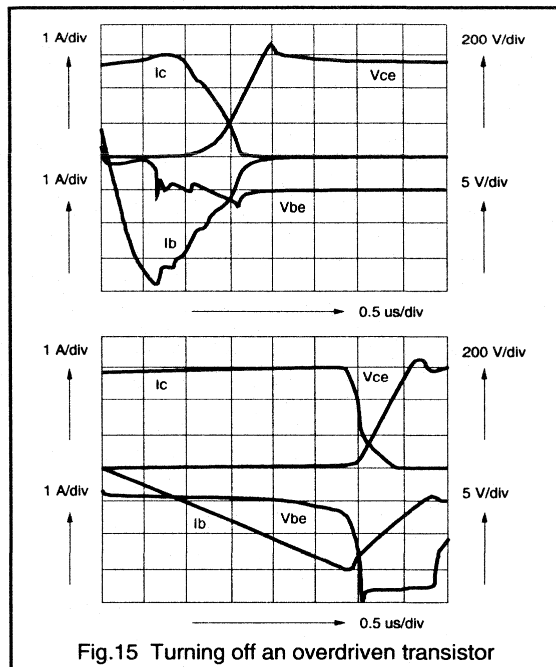


Fig.15 Turning off an overdriven transistor

$$L_B = \frac{12}{I_C} \quad \mu H$$

for normal drive

When using a desaturation circuit the value for L_B should be approximately halved. Hard turn-off may also be used with reasonable results.

Overdrive should be prevented as much as possible because considerable tails in the collector current cause unacceptable losses.

When using transistors having V_{CEO} less than 200V, hard turn-off generally gives good results. Transistors having a V_{CEO} of more than 400V have high losses when hard turn-off is used.

1.3.3 Using High Voltage Bipolar Transistors

This section looks at some aspects of using high voltage bipolar transistors in switching circuits. It highlights points such as switching, both turn-on and turn-off, Safe Operating Areas and the need for snubber circuits. Base drive design curves for the BUT11, BUW12 and BUW13 are discussed under 'Application Information' at the end of the section.

Transistor switching: turn-on

To make optimum use of today's high voltage transistors, one should carefully choose the correct value for both the positive base current when the transistor is 'on' and the negative base current when the device is switched off (see Application Information section).

When a transistor is in the 'off' state, there are no carriers in the thick n^-- layer, consequently there is a resistor with a relatively high value in the collector. To obtain a low 'on'-state voltage, a base current is applied such that the collector area is quickly filled with holes and accordingly the collector resistance will decrease. In the transition time, the so called turn-on time, the voltage and current may both be high, especially in forward converters, and high turn-on losses may result. All the holes in the collector should be delivered via the base contact and it is therefore advised that the base current waveform is such that there is a peak at the beginning. In this way the holes quickly fill the collector area so the voltage is lower and the losses decrease.

In flyback converters the current to be turned on is normally low, but in forward converters this current is normally high. The collector current reaches its on-state value in a short time which is normally determined by the leakage inductance of the transformer.

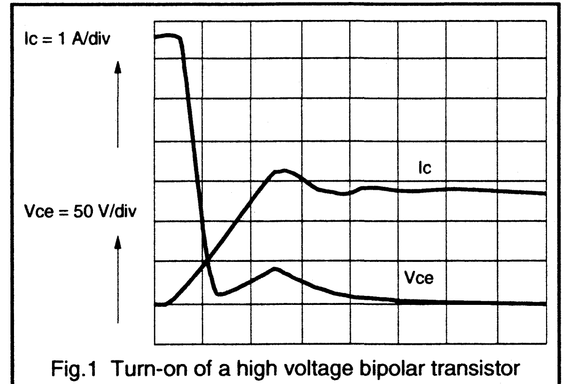


Fig.1 Turn-on of a high voltage bipolar transistor

In Fig.1 the characteristic 'hump' which often occurs at turn-on in forward converters due to the effect of the collector series resistance is observed.

The turn-on losses are strongly dependent on the value of the leakage inductance and the applied base drive. It is generally advised to apply a high initial $+I_B$ for a short time in order to minimise turn on losses.

A deeper analysis can be found in sections 2.1.2 and 2.1.3. Turn on losses are generally low for flyback converters but are the most important factor in forward converter types.

Turn-off of H.V. transistors

All charge stored in the collector when the transistor is on should be removed again at turn-off. To ensure a quick turn-off a negative base current is applied. The time needed to remove the collector hole charge is called the storage time. A short storage time is needed to minimise problems within the control loop in the SMPS.

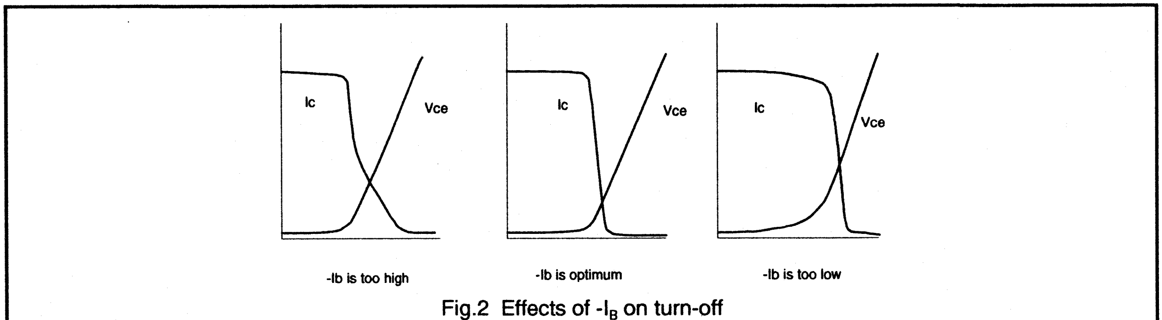


Fig.2 Effects of $-I_B$ on turn-off

Care is needed to ensure the optimum drive. First one should prevent the transistors from being overdriven. It is advantageous to keep $+I_B$ to a minimum because then the danger of tails in the turn-off current is minimal.

Second, the negative base current should be chosen carefully. If the negative base current ($-I_B$) is too low, not only will the storage time be long, but the transistor will also exhibit a high collector-emitter voltage at the end of the storage time, while the current is still high. As a consequence, the turn-off losses will be high (a more detailed explanation is given in section 1.2.2.) If, however, one chooses a very high negative current the danger exists that tails will occur in the collector current, again resulting in high losses. There is an optimum as demonstrated in Fig.2.

A circuit which is worth considering, especially at higher frequencies, is the Baker Clamp or desaturation circuit. This circuit prevents deep saturation of the transistor and one may then benefit from lower losses due to shorter switching times.

The total losses are dependent on the base drive and on the total collector current waveform. In Fig.3 the total losses are shown for a BUW133 as a function of the positive base current, for both the saturated and the desaturated case.

Please note that the loss depends on the conditions used; when different conditions are being used the picture will change. For instance when the dI/dt is less (more leakage inductance) the losses will decrease. Also when the negative drive is less hard, e.g. by applying a base coil, the turn-off losses will be lower. It depends on the specific power supply design which value of storage time is acceptable.

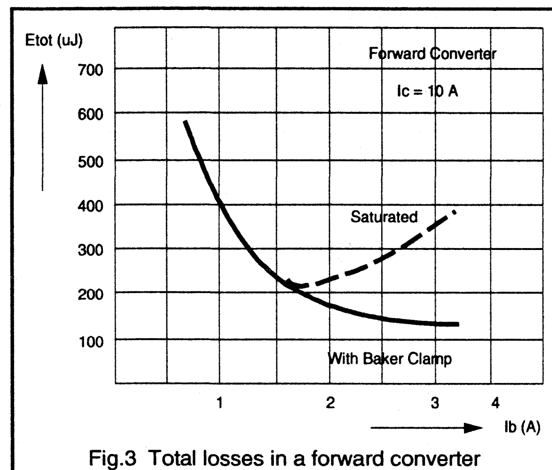


Fig.3 Total losses in a forward converter

The total number of variables is so large that it is virtually impossible to give unique base drive advice for the various applications, but as a rule of thumb one may say that in a forward converter and in bridge converters the best $+I_B$ equals I_{Bsat} which is the value of $+I_B$ which is used in both the V_{CEsat} specification and the switching times specification. By playing around with this value one can optimise it for the specific application.

For a flyback converter the best value to start experimenting with is about 2/3 of the above mentioned I_{Bsat}. The reason for this is that the start current in this case is less (triangular shaped waveform) so the applied base current is "used" better to fill the collector with holes.

The best turn-off base current depends on the voltage rating of the transistor. As a guide-line the following table gives reasonable values for the storage time and may be used to begin the optimising of the base drive:

f (kHz)	tp (µs)	ts (start)
25	20	2
150	10	1.5
100	5	1

The above table holds for transistors with a V_{CEOmax} rating of 400-450V and V_{CESmax} between 850-1000V. Transistors with higher voltages require longer storage times, e.g. transistors with V_{CEOmax}=700V and V_{CESmax}=1500V need a storage time which is approximately double the value in the table.

A recommended way to control the storage time is by switching the base to a negative voltage rail via a base coil. The leakage inductance of a driver transformer may serve as an excellent base coil. When applying a base coil one may also benefit from the fact that at the moment of the fall time the negative base current reaches a maximum, yielding a short fall time. As a guide-line the base coil should be chosen such that the peak value of the negative base current equals half the value of the collector current.

Specific problems and solutions

A high voltage transistor needs protection circuits to ensure that the device will survive all the currents and voltages it will see during its life in a converter.

a) Maximum currents

Exceeding current ratings normally does not lead to transistor failure. In the case of a short circuit, the protection is normally fast enough for problems to be avoided. Most devices are capable of carrying much more current than specified provided the times involved are very short.

b) Maximum voltages

In contrast with current ratings it is NOT allowed to exceed the published voltage ratings. As breakdown currents may flow in very small areas of the device there may be immediate damage to the device in very short times (nanoseconds). So, even for very short times it is not allowed to have higher voltages on the device. If one observes a voltage which is higher than the published value there is basically only one solution: apply transistors with a higher voltage rating.

c) Safe operating areas (SOAR)

Two areas of safe operation can be distinguished. They are Forward Bias SOAR and Reverse Bias SOAR. Forward bias safe operating area is valid when positive values of I_B or V_{BE} are present. It is only important for some overload conditions and not of much practical use in SMPS-circuits.

In contrast, Reverse bias safe operating area, which is valid for negative values of I_B and V_{BE} during turn-off with an inductive load (see Fig.4), is a key element in the specification of high voltage transistors. It gives the allowed combinations of both I_C and V_{CE} during turn-off and if one goes beyond the given boundaries there is the danger of instant failure.

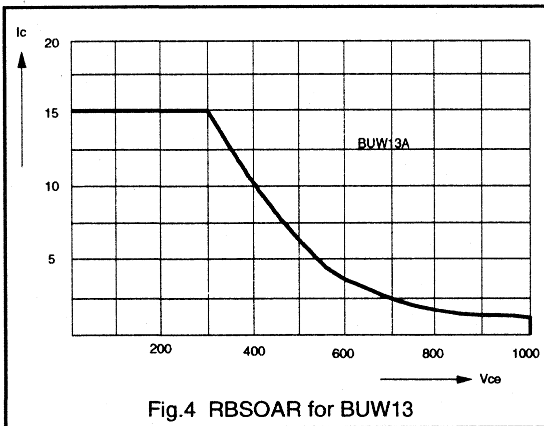


Fig.4 RBSOAR for BUW13

The usual way of ensuring that the devices stay within the published RBSOAR is to apply a snubber network (see Fig.5). When the voltage rises the diode starts conducting charging the capacitor. As the inductive load acts as a current source, one can see that the rate of rise of the voltage is limited and the locus in the I_C-V_{CE} plane is then much safer, the comparison of the locus in the I_C-V_{CE} plane with and without a snubber network is also given in Fig.5.

As a handy guide-line one may say that the snubber capacitor in a 20-40 kHz converter is about 1nF for each 100W of throughput power (this is the power which is being transferred via the transformer). One may then reduce this value empirically when required.

At higher frequencies it may appear that the capacitor should be smaller because the time available to discharge the capacitor is shorter.

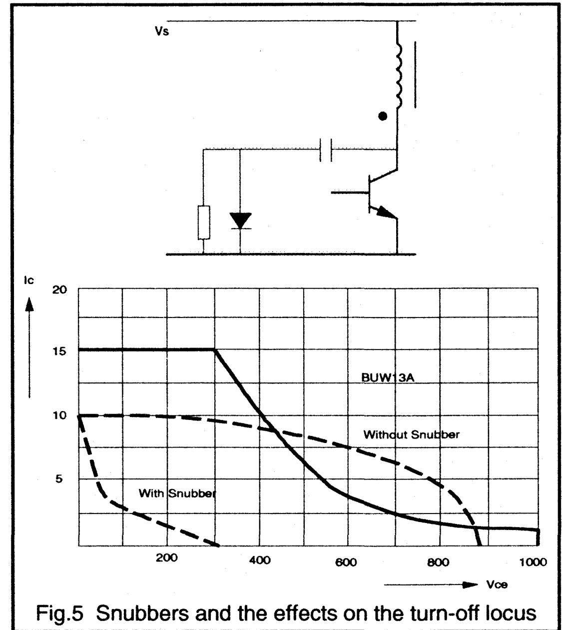


Fig.5 Snubbers and the effects on the turn-off locus

The following table may serve as a guide-line for the value of dV_{CE}/dt for some switching frequencies

f (kHz)	25	50	100
dV_{CE}/dt (kV/µs)	1	2	4

The snubber resistor should be chosen such that the capacitor will be discharged in the shortest occurring on-time of the switch.

In some cases the losses in the snubber may be considerable. Clever designs exist to feed the energy stored in the capacitor back into the supply capacitor, but we will not discuss them here.

d) Other protection networks

In Fig.6 a "maximum protection" diagram is shown with various networks connected. R4, C4, and D4 form the above mentioned snubber. The network with D5, R5 and C5 forms a "peak detector" to limit the maximum occurring collector emitter voltage.

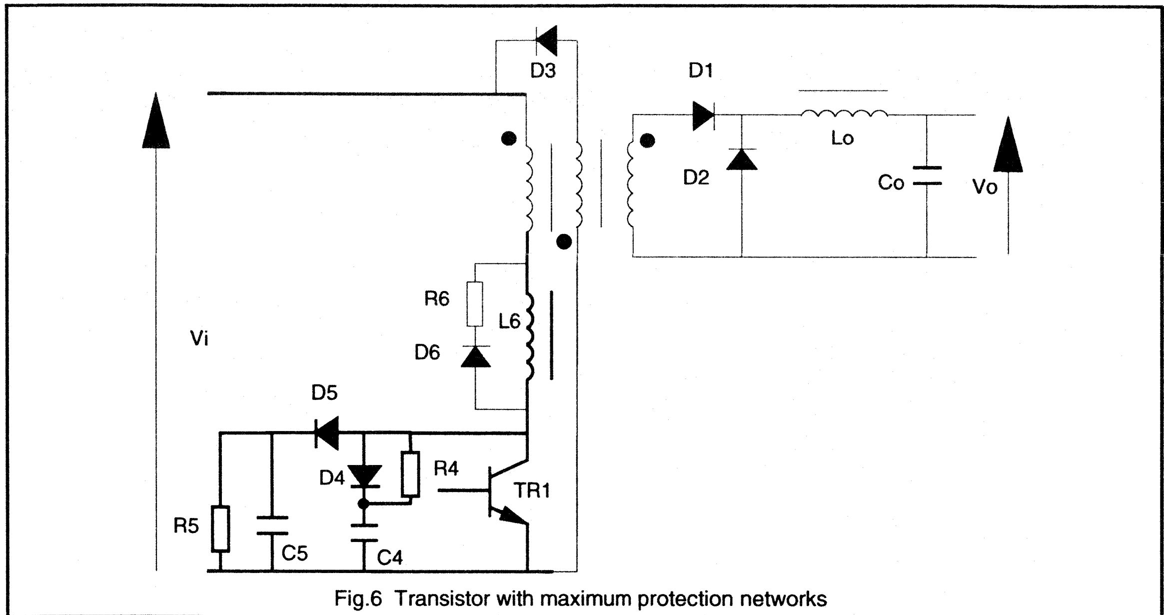


Fig.6 Transistor with maximum protection networks

The inductor L6 serves to limit the rate of rise of I_C which may be very high for some transformer designs. The slower dI_C/dt leads to considerably lower turn-on losses as previously described. Added to L6 is a diode D6 and a resistor R6 which should be dimensioned such that the inductor loses its energy during the off-time of the power switch.

While the snubber is present in almost all SMPS circuits where transistors are used above V_{CEOmax}, the dI_C/dt limiter is only needed when the leakage inductance is extremely low. The peak detector is applied in those circuits which have a bad coupling between primary and secondary windings.

Application Information

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the maximum collector current amplitude and shape.

The operating frequency is mostly set between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Information on nominal base drive, optimum base inductance and maximum transistor dissipation applied in a forward converter is given in appendix I for the BUT11, BUW12 and BUW13. In these figures I_{CM} represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 ˚C under the following conditions (see also Fig.7):

- collector current shape I_{C1} / I_{CM} = 0.9
- duty factor (t_p / T) = 0.45
- rate of rise of I_C during turn-on = 4 A/µs
- rate of rise V_{CE} during turn-off = 1 kV/µs
- reverse drive voltage during turn-off = 5 V
- base current shape I_{B1} / I_{Be} = 1.5

The required thermal resistance of the heatsink can be calculated from

$$R_{th(mb-amb)} < \frac{100 - T_{amb}}{P_{tot}} \quad \text{K/W}$$

To ensure thermal stability the value of the ambient temperature T_{amb} >40 ˚C.

As a base coil is normally advised and a negative drive voltage of -5V is rather common, the value for the base coil, L_B, is given for these conditions. For other values of $-V_{drive}$ (-3 to -7 volt) the base coil follows from:

$$L_B = L_{Bnom} \cdot \frac{(-V_{drive} + 1)}{6}$$

Where L_{Bnom} is the value given in the figures.

Fig.7 Relevant waveforms of the switching transistor in a forward SMPS.

It should be noted, that this advice yields acceptable power losses for the whole spread in the product. It is not just for typical products as is sometimes thought! This is demonstrated in Fig.8, where limit and typical devices are compared (worst-case saturation and worst-case switching).

It appears that the worst-case switching devices have losses P0 at the advised I_{Bend} (I_{Badv}) + 20%, while the saturation worst-case devices have the same losses at I_{Badv} - 20% (that is how I_{Badv} is determined). A typical device now has losses P1 at I_{Badv}, while the optimum I_{Bend} for the typical case might yield losses P2 at an approximately 15% lower I_{Bend} (NB: this is not a rule, it is an example).

Conclusion

To avoid exceeding the RBSOAR of an HVT, snubbers are a requirement for most circuits. To minimise both switching and on-state losses, particular attention should be given to the design of the base drive circuit. It is generally advised that a high initial base current is applied for a short time to minimise turn-on loss. As a guide-line for turn-off, a base coil should be chosen such that the peak value of the negative base current equals half the value of the collector current.

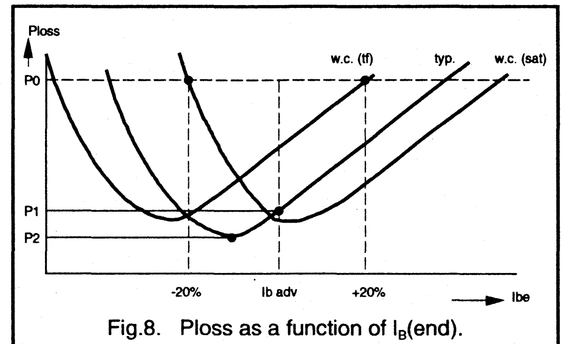
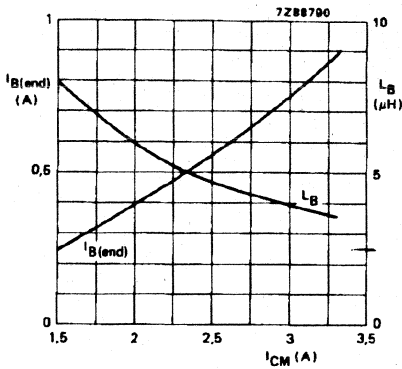
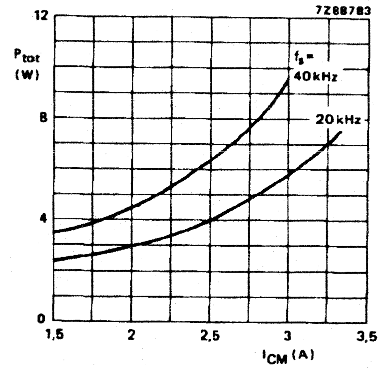


Fig.8. Ploss as a function of I_B(end).

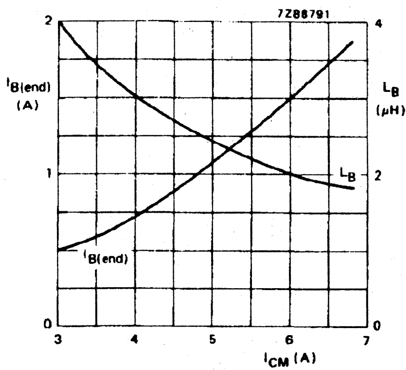
Further guide-lines on optimising HVT circuits for maximum reliability are given in chapter 2.1.2.

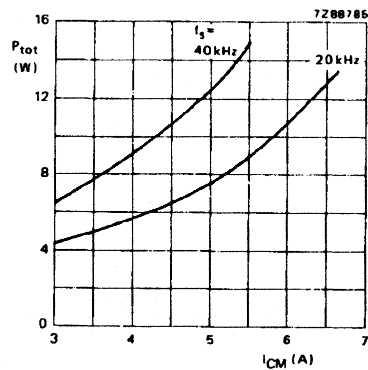
Appendix 1 Base Drive Design Graphs



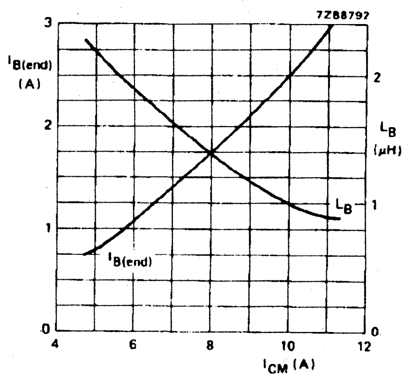


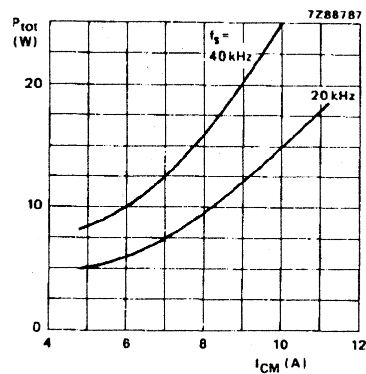
BUT11 Base Drive Design Information





BUW12 Base Drive Design Information





BUW13 Base Drive Design Information

1.3.4 Darlingtons for High Power Systems

The darlington is made with two transistors (see Fig.1.). Obviously, the gain of the darlington is higher than that of a single transistor but darlingtons offer other advantages as well. This section looks at some of the properties of darlingtons with particular emphasis on switching behaviour.

To understand a darlington's switching behaviour it is first necessary to be familiar with the switching processes of a bipolar transistor.

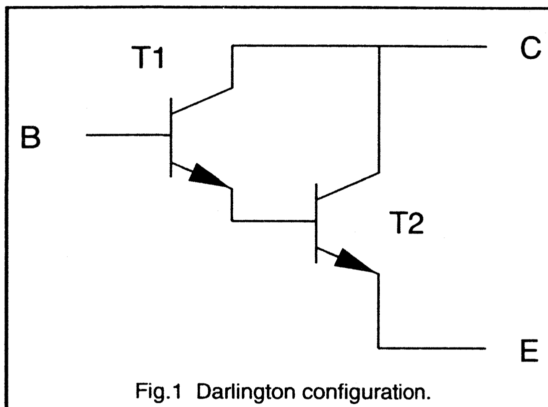


Fig.1 Darlington configuration.

The switching process of a transistor.

A high voltage transistor in the off-state, has no stored charge, however, in the on-state, three regions of charge can be distinguished (see Fig.2(a)). The first charge Q_B, in the base, is essential for transistor operation: if Q_B equals zero, the emitter will not inject electrons (thus $I_E = 0$). The second charge, Q_C, is located in the collector area underneath the emitter and is responsible for the characteristic low resistance, which makes the collector emitter voltage low: increasing Q_C decreases V_{CEsat}. The third charge, Q_D, is located in the collector region underneath the base contact. When the base-collector region becomes forward biased (which happens at very low values of V_{CE}), Q_D rapidly increases as V_{CE} decreases further. The relative influence of the collector emitter voltage V_{CE} is given in Fig.2(b).

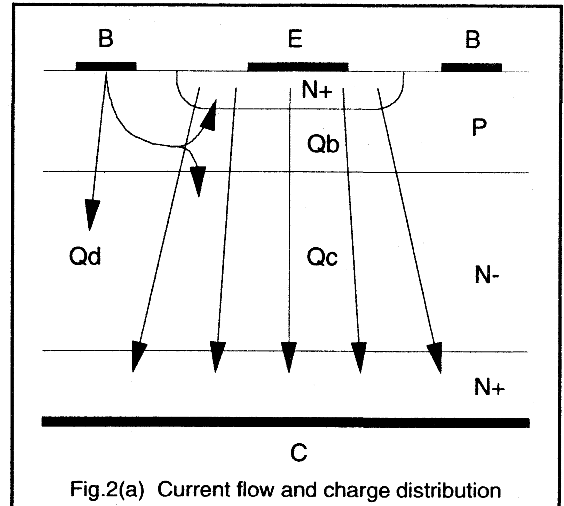


Fig.2(a) Current flow and charge distribution

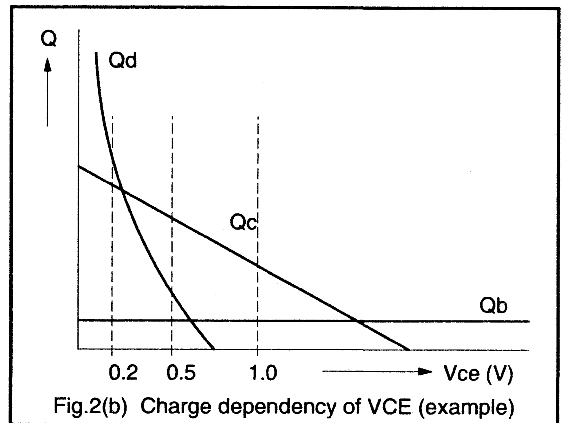


Fig.2(b) Charge dependency of VCE (example)

At turn-off the charges must be removed by applying a negative base current ($-I_B$), pulling the charges out of the transistor. This process can be divided into four phases, as is shown in Fig.3; the first two during the storage time, the other two during the fall time.

First the negative base current extracts charge from Q_D until it is zero.

Then the charge is extracted from Q_C, starting from the area underneath the edges of the emitter. Also Q_B will now decrease and the collector current is forced towards the centre of the emitter. As long as Q_B is sufficiently high a collector current will flow, however, V_{CE} must increase

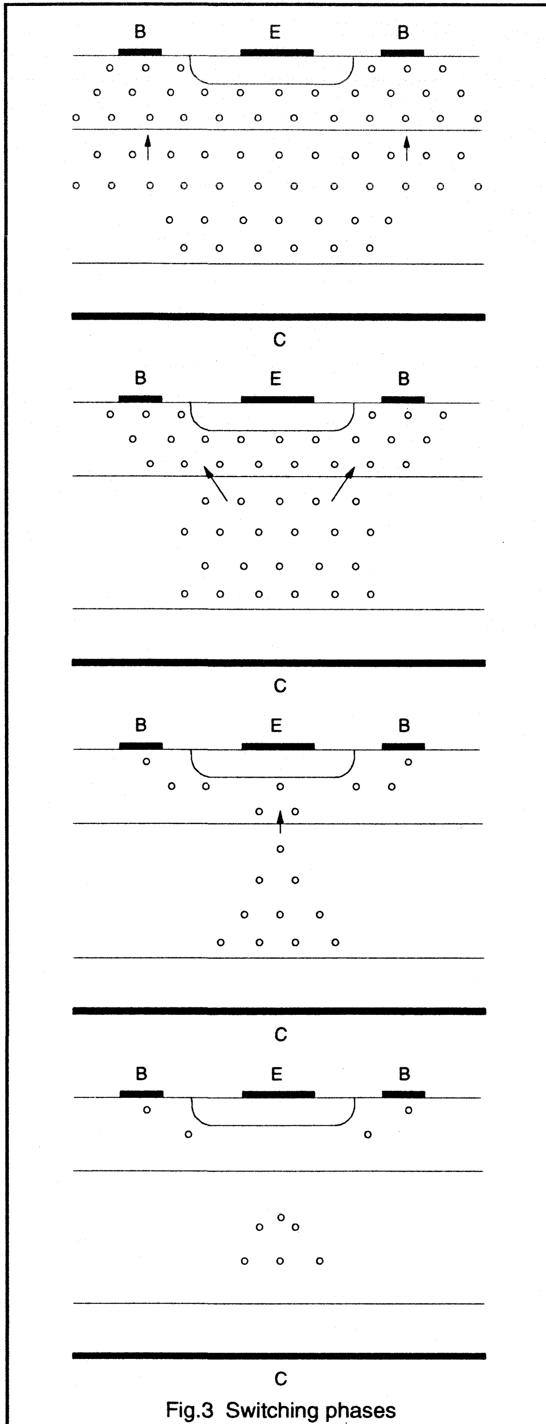


Fig.3 Switching phases

because the current density becomes higher. When the emitter current is contracting, the negative base current flows through the base resistance beneath the emitter. The base emitter voltage now becomes more negative, because the resistance increases during current contraction. At the end of the storage time the emitter current is concentrated in the middle of the emitter finger.

The fall time begins as soon as Q_B is too low to force emitter injection. The emitter current decreases with a speed depending on the rate of change in Q_B: $I_E = 0$ when $Q_B = 0$.

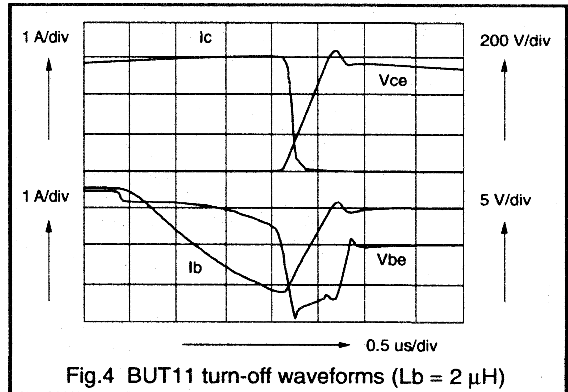


Fig.4 BUT11 turn-off waveforms (Lb = 2 μH)

A trapped rest-charge Q_R in the collector is now removed via a collector base current, which appears as a tail in the collector current turn-off wave forms.

Fig.4 shows the waveforms of a BUT11 in a forward converter. The four phases are easily recognised (the positive base current was chosen such that the two parts in the fall time are clearly distinguished).

1 - Removal of Q_D until t = 0,7 μs (approx.)
2 - Q_C and Q_B decrease until t = 1,6 μs
3 - Removal of Q_B until t = 1,75 μs
4 - Removal of Q_R until t = 1,85 μs.

Note the course of V_{BE}: first the decrease in voltage due to the base resistance during current contraction and second (because a base coil has been used) the value of V_{BE} which is clamped by the base emitter breakdown voltage of the transistor. This causes no harm to the transistor, since breakdown takes place near the crystal surface and not in the active region.

Darlingtons.

As is shown in Fig.5 a darlington is made with two transistors: T1 the input or driver transistor, T2 is the output transistor. Darlingtons intended for fast switching must also include a so called speed-up diode. This speed-up diode provides a current path for the extraction of the collector charges which are present in the output transistor. Without this diode the switching losses may be very high and the

energy handling is worse. Normally a resistor is present between base and emitter of T2 as well, this is discussed later.

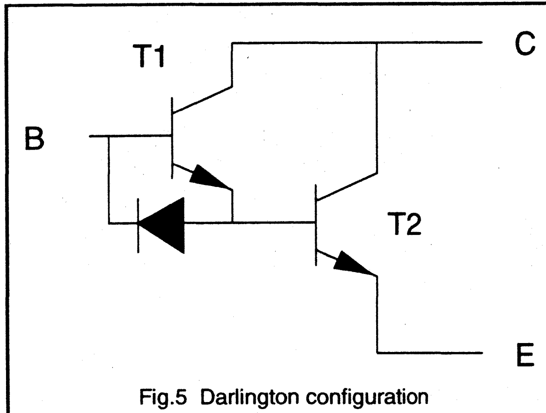


Fig.5 Darlington configuration

The obvious advantage of a darlington is its higher current gain. The positive base drive can therefore be much less than in the case of a single transistor.

When constructing darlingtons with discrete transistors one might use the current gain as a guide-line to determine the size of the driver. To drive a 10 A transistor, having a gain of 5, it seems logical to use a 2 A transistor as a driver, yielding a 12 A darlington. However, this is not correct and dynamic considerations lead to a different conclusion. Before discussing the switching behaviour of a darlington it is important to realise that the driver transistor in fact desaturates the output transistor.

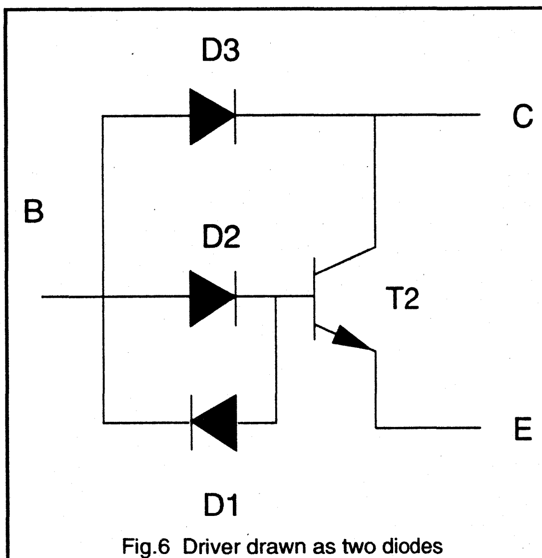


Fig.6 Driver drawn as two diodes

In Fig.6 the driver transistor is drawn as D2 (base emitter diode) and D3 (base collector diode). (D1 is the speed up diode). It is clear that D2 and D3 form a desaturation circuit preventing the output transistor from being severely overdriven and the base current of T2 will be the exact value required for its V_{CE}. This highlights another important result, the driver transistor will always be overdriven because it takes all the excess base current. (Overdrive can be avoided if a desaturation network is used around the darlington.) Thus, a darlington consists of an overdriven driver and a desaturated output transistor.

The effects of overdriving a transistor

When a transistor is overdriven, the base current is higher than needed which will lead to an increase in the charge stored in the device. Because overdrive yields very low values of V_{CE}, Q_D will become very large as is shown in Fig.2. Consequently an increase in storage time will result. Furthermore an effect known as "deep hole storage" causes charge to be stored in the lowest N^+-layer deep in the collector region (see Fig.7.). During the turn off this charge is responsible for a rest charge Q_R which is considerably more than in the normal case (where Q_C just reaches the lowest N^- region). The result of overdrive will be a serious increase in switching times, not only ts but also tf, as there will be a considerable tail.

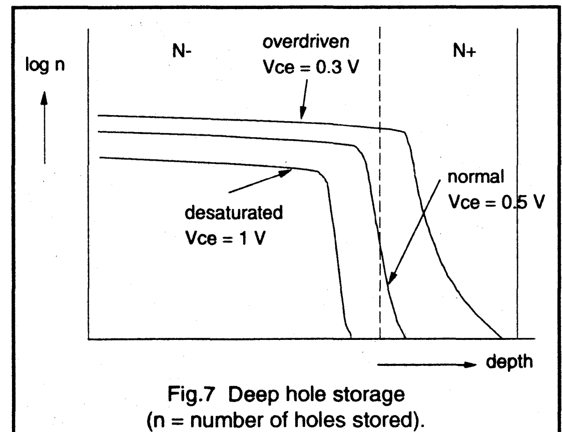


Fig.7 Deep hole storage
(n = number of holes stored).

The effects of desaturation

When a transistor is desaturated (Fig.6) the diodes will force a V_{CEsat} of about 1 V. This has two important consequences. First, there will be no Q_D since the collector base voltage is about zero, so the storage time will be reduced. Second, the charge Q_C will be less than normal and located closer to the base-collector junction, so Q_R will be less and the fall time will be shorter.

Switching behaviour of darlingtons.

When a darlington with a speed-up diode is switched off, first the charge of the input transistor T1 will be removed. The driver will initially draw more collector current which can flow out through the base adding to the negative base current, while at the same time the output transistor will draw less current (see Fig.8). There will be a considerable rest charge in the driver since it is overdriven. Then, as the base voltage decreases due to current contraction, the speed-up diode becomes conductive. Now the collector of the output takes the whole load current and its stored charge is removed prior to the fall time. The storage time of the output transistor allows time for the rest charge Q_R of the input transistor to disappear. However this happens at a low value of V_{BE} (equal to the forward drop of the speed up diode) which means that a tail in the turn off waveforms may appear when the driver transistor is strongly overdriven. In order to prevent this situation and to allow for the ever present overdrive, the driver transistor should be chosen bigger than indicated by current gain considerations.

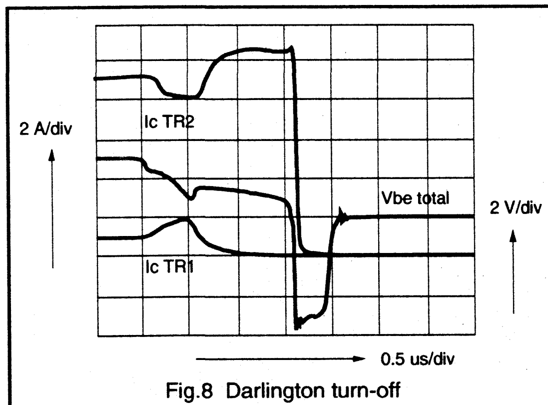


Fig.8 Darlington turn-off

Fig.9 is an example of turn-off of a darlington with a small driver under overdrive conditions. Given here are the collector currents of both the driver, output transistor and total current plus the rising collector emitter voltage at the end of the storage time. Just before the fall time begins, one can see that the driver's I_C is increasing again because the rising voltage activates the trapped charge Q_R leading to a considerable tail in the turn off current. This tail, as shown in Fig.9, shows up in the driver rather than the output transistor! Therefore the current rating of the driver should be big enough.

As a general guide-line one may state that -provided the darlington is designed correctly- the best value for the $-dI_B/dt$ is the same as for a desaturated transistor. So as a guide-line:

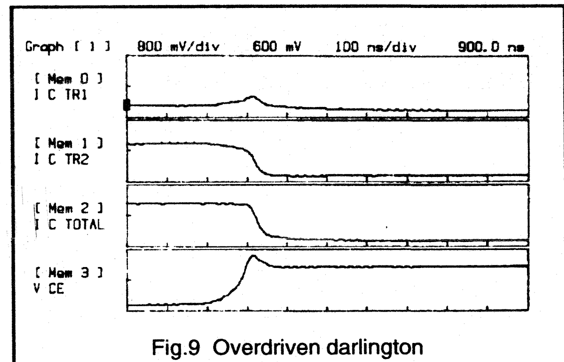


Fig.9 Overdriven darlington

400 V (V_{CEOmax}) darlingtons: $-dI_B/dt = I_C$ (A/µs)
800 V (V_{CEOmax}) darlingtons: $-dI_B/dt = I_C/3$ (A/µs)

As an example: a 25 A darlington with V_{CEOmax} = 400 V has an optimum $-dI_B/dt$ of 25 A/µs. With a negative drive of -5 V this means a base coil of 0.2 µH. So, apart from a higher current gain, a well-designed darlington is much less sensitive to overdrive and can have shorter storage times.

Discrete darlingtons.

An important question when making discrete darlingtons is the ratio between driver and output transistor. Calculating with H_{FEmin} = 5 (for a transistor with a $V_{CEOsust}$ = 400 V), the conclusion may be drawn that a 10 A transistor should be driven with a 2 A transistor. This, however, yields a darlington which is sensitive to overdrive and may show a tail during turn-off. Because the driver operates at a very low V_{CE} the current gain is very low and the stored charge is high. For a fast switching 400 V (V_{CEO}) transistor, as a rule of thumb, the driver should be about twice the size predicted from current gain calculations. So in this case not a 2 A transistor but a 4 A device should be chosen.

The total switching current capability, however, is higher than 10 + 4 = 14 A. When the above mentioned rule is applied, the output transistor can handle 50% more than its normal current because it is desaturated. So in this case the output can handle 15 A and the total current in the darlington can be as high as 4 + 15 = 19 A.

For transistors with voltage ratings other than 400 V, the optimum ratio of driver to output will be higher at lower voltages whilst in the case of higher voltage transistors this value will be lower. The table below gives an indication of how to make a 10 A darlington for a selection of V_{CEOmax} values. So, a 10 A darlington with a V_{CEO} of 200 V may be made with a 6 A output and a 1.5 A driver transistor etc...

V_{CEOmax}	Darlington	Output	Driver
200 V	10 A	6 A	1.5 A
400 V	10 A	5 A	2.5 A
800 V	10 A	4 A	4 A

Table 1: Discrete Darlingtons design guide-lines

For discrete darlingtons composed with BUT-transistors the switchable currents and the drive requirements are given in Table 2. As a guidance: 1 transistor driving 2 identical ones yields a darlington that can handle a current which is twice the total current capability of the output transistor; 1 transistor driving 3 identical ones can handle 1.75x the total current capability of the output transistors. For the Philips types BUT 11 to 14 one may of course also read similar devices with the same I_{Csat} (given in between brackets).

Driver T1	Output T2	Switchable Current (A)	Required base drive (A)
BUT11 (3 A)	BUT12 (6 A)	6 - 12	0.14 - 0.6
BUT12 (6 A)	BUW13 (10 A)	10 - 20	0.22 - 0.9
BUW13 (10 A)	2 x BUW13 (20 A)	20 - 40	0.45 - 2
BUW13 (10 A)	3 x BUW13 (30 A)	30 - 52	0.75 - 2.4
BUV98 (20 A)	BUV298 (40 A)	40 - 80	0.9 - 4
BUV98 (20 A)	3 x BUV98 (60 A)	60 - 104	1.5 - 4.8

Table 2: Discrete darlingtons.

The advice given above is valid for high frequency switching (say, 20 kHz). For lower frequencies (up to say 2 kHz) when the dynamic properties are not essential, the ratio which follows from current gain considerations will suffice. The speed-up diode is not necessary then, but there has to be a current path to remove the collector charges, so a resistor (parallel the base-emitter of both driver and output) must be applied.

Dynamic Considerations.

Strange things may occur when using darlingtons in very fast switching applications. Generally, ringing and or oscillations occur and it is sometimes difficult to find an explanation for certain effects. Some peculiarities which are commonly experienced are described below.

Ringing Tail

When using darlingtons in a chopper an effect which can be described as "a tail with ringing" after the fall time, sometimes leading to destruction of the device, can occur. Measurements revealed, that the cause was a fast rising V_{CE} fed back to the base via the collector base capacitance. Ringing occurs in the base drive circuit and the device can become forward biased again (see Fig.10) especially when there is a high drive impedance. When using a series base coil, always use a resistor between base and emitter of the driver. This may prevent the driver from becoming forward biased. In the case of a snubber the problem hardly exists because the dV_{CE}/dt is too low to forward bias the base via the collector base capacitor.

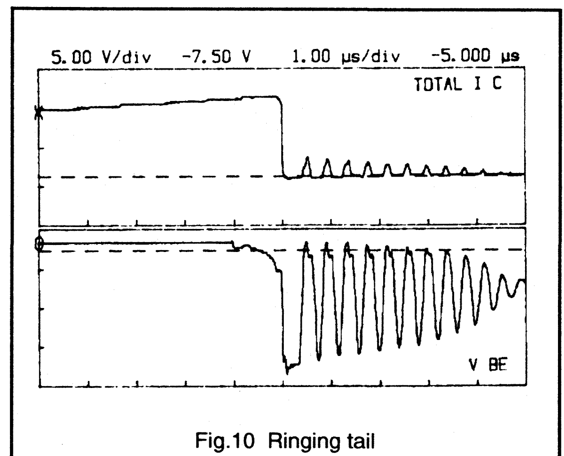


Fig.10 Ringing tail

There is also an advantage to be gained in using more than one speed up diode. The speed up diode enables a reverse bias voltage to be developed across the drive transistor during turn-off. Connecting two or three diodes in series instead of just the one, enables a larger reverse bias voltage to be developed. This will hold off the driver more effectively and help prevent oscillations.

Oscillations in V_{CE}

When using a darlington in a flyback circuit where the voltage after turn off is high, the voltage may show ringing at the end of the transfer period when the voltage decreases again as shown in Fig.11. In some cases a spontaneous oscillation may start which could lead to device destruction. The explanation is as follows: when the voltage decreases, a negative going voltage is also induced on the base of the output transistor via its collector base capacitance. This will of course not forward bias the output transistor, but, as the emitter of the driver is connected to this base contact as well, it may forward bias the driver transistor. As a result, the driver will turn on again, but due to a lack of drive energy,

it will quickly switch back off so the voltage will rise again. The next negative going edge of the collector voltage will then re-start the procedure.

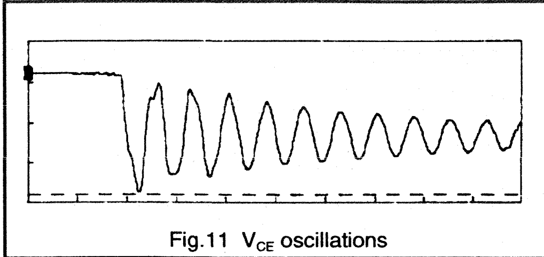


Fig.11 V_{CE} oscillations

The measure to take is to provide a low impedance path between the base and emitter of both the output and driver transistor. Applying a base emitter resistor for the T2 may prove sufficient. Fig.12 show the difference in ringing when a resistor of 10 ohms is placed parallel to the base emitter of the output transistor. It is obvious that a low base emitter resistor dramatically reduces ringing on the base.

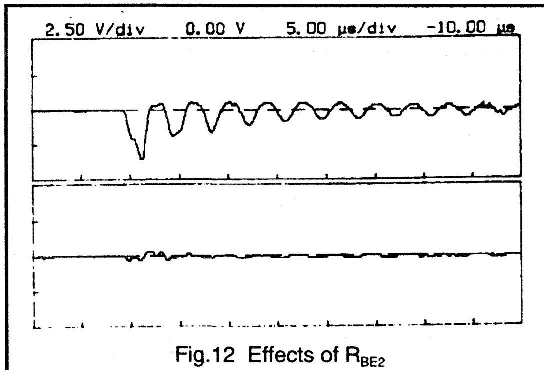


Fig.12 Effects of R_{BE2}

Other Perils

Other effects exist which may seriously affect the behaviour of darlingtons in practical circuits. One to watch carefully is lead inductances: in the case of discrete darlingtons with parallelled output transistors this may lead to serious mismatches in current sharing. The recommended way of parallelling is to make a symmetrical layout ensuring that lead inductances are identical for the parallelled devices especially for the higher current leads.

Another trap to be avoided is the required base current. The higher current gain of a darlington does not turn the darlington into a PowerMOS, not for ease of drive and not for switching times. One may be tempted to apply a low value for the positive base current but as most darlingtons are being used in high power systems with high initial values for the current, it is advised to have a peak current at turn-on for the first few microseconds. Also one should realise that a considerable negative energy is required to turn-off the darlington, although it is roughly half the energy required to turn-off a similar transistor. As in the case of transistors one should allow the darlington time to turn off by "programming" a storage time.

Ready Made Darlingtons.

Ready made darlingtons can be made monolithic, primarily for lower powers, or made with discrete chips. The ISOTOP outline (SOT227), a collaboration project between Philips and STM, mostly contains a few crystals which are internally wired. Of course the design guide-lines, as discussed in the paragraphs above were used to make the designs. The result is a range of darlingtons, which is optimal for high frequency switching. The 4-lead package allows full access to the darlington allowing the correct measures to be taken in case of problems, such as previously described. Other huge advantages of the ISOTOP package are 2.5 kV insulation and creepage distances of 9.5 mm, enough for a UL1577 approval.

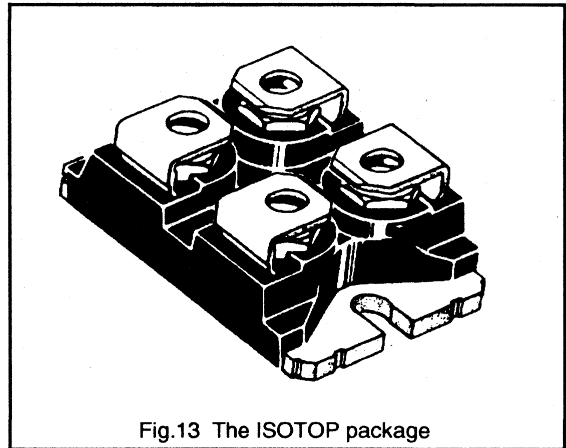


Fig.13 The ISOTOP package

The ISOTOP package also features a very low internal inductance of 5 nH which yields very low internal voltages across the wires. For darlingtons in ISOTOP this means less parasitic effects, so the darlingtons perform optimally. Table 3 gives a list of output powers which can be obtained in ACMC systems with some ISOTOP darlingtons, both from single phase and from three phase mains.

More information on the use of ISOTOP and drive circuits for darlingtons can be found in chapter 3.

Type	V_{CESMAX}	V_{CEOMAX}	I_{CSAT}	I_{BSAT}	Power (kW) 220 / 240 V	Power (kW) 380 / 440 V
	(V)	(V)	(A)	(A)	without snubber	with snubber
ESM3045A	1000	450	18	0.72	-	5
ESM3045D	600	450	15	0.3	3	-
ESM4045A	1000	450	30	1.2	-	10
ESM4045D	600	450	25	0.5	5	-
ESM6045A	1000	450	60	2.4	-	18
ESM6045D	600	450	50	1.0	10	-

Table 3. Output power guide-lines for ISOTOP darlingtons.

Conclusions.

A practical darlington consists of a desaturated output transistor plus an overdriven driver transistor.

Overdrive leads to relatively long storage times and to tails while desaturation leads to shorter storage times and a short fall time.

The tail of a driver is allowed to last as long as the storage time of the output transistor.

A darlington for fast switching should have a driver that is twice as big as calculated to be necessary for current gain. The output transistor can then handle about 50% more than its normal current.

Ringing may occur when there is no low resistive path for the collector base current when the collector voltage changes quickly. For a fast rising V_{CE} there is the danger of parasitic turn-on of driver or output transistor. In the case of a quick decrease of V_{CE} the driver may turn on again due to a negative voltage on its emitter.

ISOTOP devices contain a complete optimised darlington on one insulated high current package with many advantages.

1.3.5 Understanding The Data Sheet: High Voltage Transistors

Being one of the most important switching devices in present day switch-mode power supplies and other fast switching applications, the high voltage transistor is a component with many aspects that designers do not always fully understand. In spite of its "age" and the variety of papers and publications of manufacturers and users of high voltage transistors, data sheets are somewhat limited in the information they give. This section deals with data sheets of high voltage transistors and the background to their properties. A more detailed look at the background to transistor ratings can be found in chapter 2.1.2.

Fig.1 shows the cross section of a high voltage transistor. The active part of the transistor is highlighted (the area underneath the emitter) and it is this part of the silicon that determines the primary properties of the device: breakdown voltages, current gain, switching times. All the added parts can only make these properties worse: a bad passivation scheme can yield a much lower collector-base breakdown voltage, too thin wires may seriously decrease the current capability, a bad die bonding (soldering layer) leads to a high thermal resistance but can also cause a bad thermal fatigue behaviour.

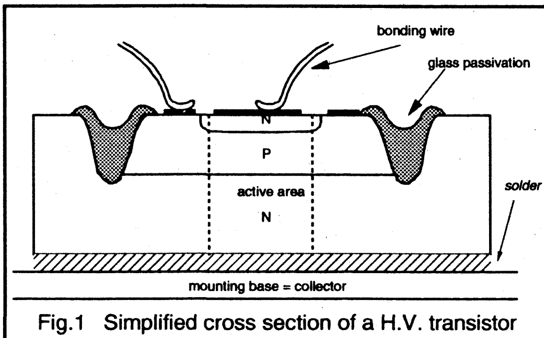


Fig.1 Simplified cross section of a H.V. transistor

The data sheet

The data sheet of a high voltage transistor can specify -

* Ratings: maximum allowable currents through and voltages across terminals as well as temperatures that must not be exceeded.

* Characteristics: describing properties in the on and off state (static) as well as dynamic, both in words and in figures.

* SOAR: safe operating area both in forward and reverse biased conditions.

Data sheets are intended as a means of presenting the essentials of a device and at the same time give an overview of the guaranteed specification points. This data is checked as a final measurement of the device and customers may wish to use it for their incoming inspection. For this reason the data is such that it can be inspected rather easily in relatively simple test circuits. This somewhat application unfriendly way of presenting data is unavoidable if cheap devices are a must, and they are!.

Each of the above mentioned items will now be discussed in more detail, in some instances parts of the data for a BUT11 will be used as an example. The BUT11 is intended for 3 amp applications and has a maximum V_{CES} of 850 volts.

Maximum ratings

There is a significant difference between current and voltage ratings. Exceeding voltage ratings can lead to breakdown phenomena which are possibly destructive within fractions of a second. The avalanche effects normally take place within a very small volume and therefore only little energy can be absorbed. Surge voltages, as are sometimes allowed for other components, are out of the question for high voltage transistors!

There is however, no reason to have a derating on voltages: using the device up to its full voltage ratings - in worst case situations - is allowed. The life tests, done in our quality laboratories, clearly show that no voltage degradation takes place and excellent reliability is maintained.

From the foregoing it should be clear, that the habit of derating is not a good one. If you, as a designer, are convinced that the collector-emitter voltage never exceeds, say, 800 volts, do not ask for a transistor having 1000 volts blocking capability! Higher voltage devices not only have a lower gain, but also higher switching losses.

The rating for the emitter-base voltage is a special case: to allow a base coil to be used, the base-emitter diode may be brought into breakdown; in some cases a $-I_{Bav}$ is given to prevent excessive base-emitter dissipation. The only effect of base-emitter breakdown that has been observed is a slight decrease in current gain at very low values of the collector current (approximately 10% at say a few milliamps); at higher currents the effects can be neglected completely.

The maximum value for V_{CEO} is important if no snubber is applied; it sets a firm boundary in applications with a very fast rising collector voltage and a normal base drive (see also section on SOAR).

Currents above a certain value may be destructive if they last long enough: bonding wires fuse due to excessive heating. Therefore short peak currents are allowed well above the rated I_{Cmax} with values up to five times this value being published for I_{CMmax}. Exceeding the published maximum temperatures is not immediately destructive, but may seriously affect the useful life of the device. It is well known, that the useful life of a semiconductor device doubles for each 10K decrease in working junction temperature. Another factor that should be kept in mind is the thermal fatigue behaviour, which strongly depends on the die-bonding technology used. Philips high voltage devices are capable of 10,000 cycles with a temperature rise of 90K!

This kind of consideration leads to the following advice: under worst case conditions the maximum case-temperature should not exceed 115 ˚C for reliable operation. This advice is valid regardless of the maximum temperature being specified. Of course for storage the published values remain valid!

The maximum total power-dissipation P_{tot} is not a very useful parameter as it is the quotient of T_{jmax} and $R_{th(j-mb)}$, ($R_{th(j-mb)}$ is the thermal resistance from junction to mounting base), implying a rather impractical infinite heatsink, kept at 25 ˚C!

Electrical characteristics

Static parameters characterise leakage currents, current gains, saturation voltages; dynamic parameters are switching times, but also include transition frequency and collector capacitance.

To start: I_{Csat}, the collector saturation current, is that value of the collector current where both saturation and switching properties of the devices are specified. I_{Csat} is not a characteristic that can be measured, but it is used as a specification point.

In the off-state various leakage currents are specified, however these are mostly unimportant. Also a $V_{CEOsust}$ is specified, being equal to V_{CEOmax}: for switching purposes it is the RBSOAR that is important (see next section).

In the on-state the saturation voltages V_{CEsat} and, to a lesser extent, V_{BEsat} are important. V_{CEsat} is a measure for saturation losses and V_{BEsat} normally influences base drive. At some more points, minimum or typical values for the current gain h_{FE} may be given. Sometimes even worst case V_{CEsat} is given as a function of both I_C and I_B. It is not possible to precisely relate these curves to a real circuit; in practice currents and voltages vary over a switching cycle, current gain therefore varies in time (e.g. directly after turn-on) and exact results can never be predicted. A reasonable indication can, however, be obtained using these curves.

Both the transition frequency (f_T) and the collector capacitance (C_c or C_{ob}) are minor parameters: they do not affect the performance in fast switching applications and both are strongly dependent on the measuring conditions.

Switching times may be given in circuits with an inductive or a resistive collector load (see Fig.2 for simplified test circuits and waveforms).

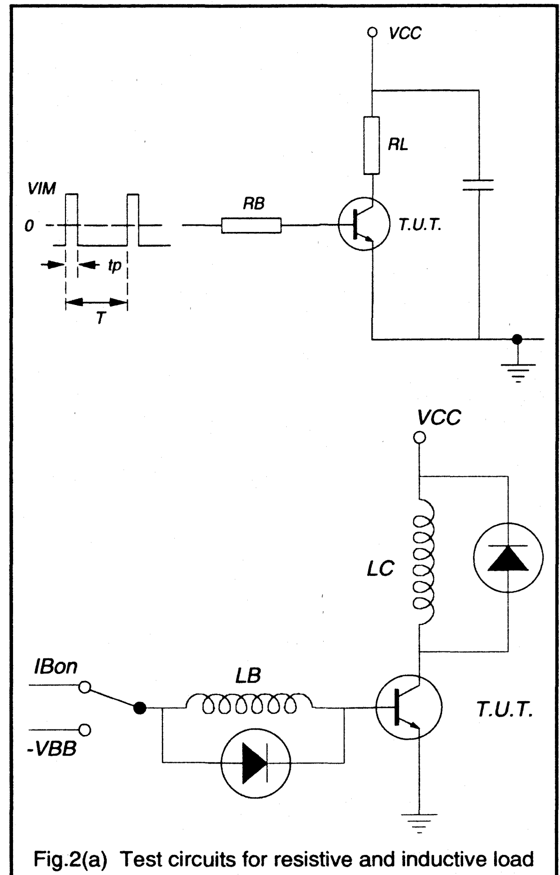


Fig.2(a) Test circuits for resistive and inductive load

When comparing similar devices from different manufacturers one is confronted with a great variety of base drive conditions. The positive base current ($+I_B$) may be the same as the one used in the V_{CEsat} spec. but also lower values (up to 40% lower) or desaturation networks may be used, yielding better ts and tf values. The negative base drive, $-I_B$, may equal $+I_B$ or it may be twice this value, yielding a shorter ts, and sometimes it is determined by switching the base to a negative voltage, possibly via a base coil. Altogether it is quite confusing and when comparing switching times one should be well aware of all the differences!

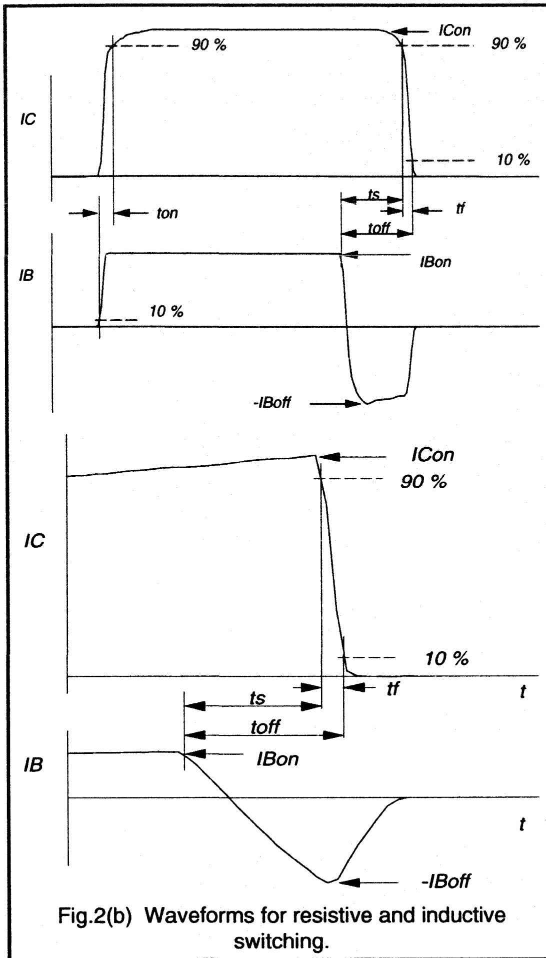


Fig.2(b) Waveforms for resistive and inductive switching.

As an example a BUT11 has been measured at $I_C = 3$ amps in a resistive test circuit varying both $+I_B$ and $-I_B$. The results in table 1 show that it is possible to turn a normal transistor into a super device by simple specmanship!

$I_C = 3$ A	ts (µs)	tf (ns)
$+I_B = 0.6$ A; $-I_B = 0.6$ A (normal case)	2.5	260
$+I_B = 0.36$ A; $-I_B = 0.72$ A (underdriven)	1.6	210
$+I_B = 0.36$ A; $-V_{BE} = -5$ V (underdriven, hard turn-off)	0.8	50

Table 1 Switching times and base drive for the BUT11

The effect of base drive variations on storage and fall times is given in table 2. The reference is the condition that both $+I_B$ as well as $-I_B$ equals the value for I_B given in the V_{CEsat} spec.

	ts	tf	comments
$+I_B$ = ref.	normal	normal	reference
$+I_B$ = 40% less	↓	↓	
Desaturated	↓	↓	
$-I_B$ = ref.	normal	normal	reference
$-I_B = 2 * +I_B$	↓	↓	
Directly to -5 V	↓	↑	with normal base drive!
Directly to -5 V	↓	↓	if under driven
Via L to -5 V	↓	↓	

Table 2 Switching times and base drive variations.

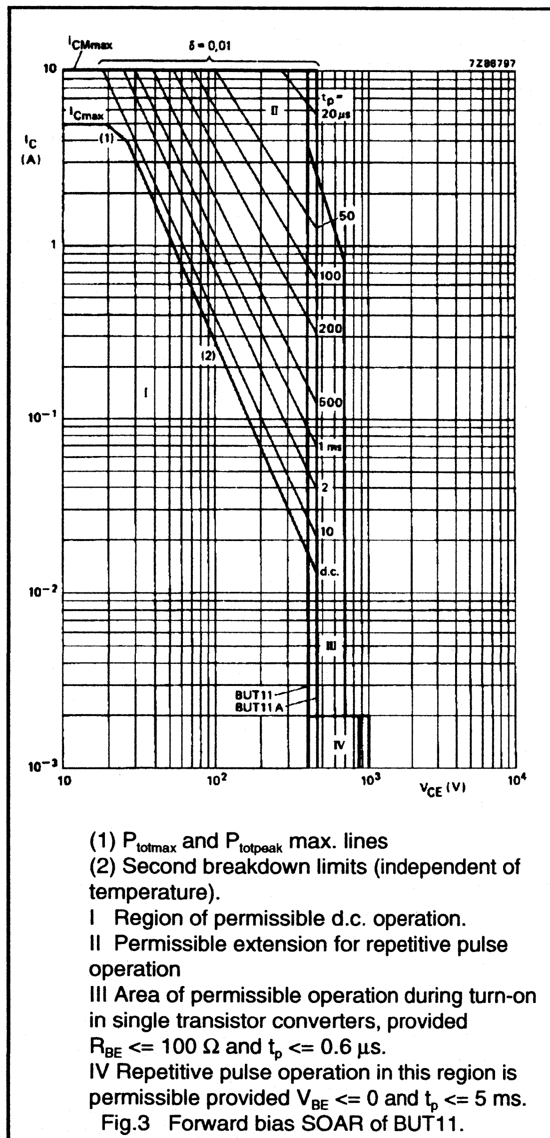
The turn-on time is a parameter which only partially correlates with dissipation as it is usually the behaviour directly after the turn-on time which appears to be most significant. Both inductive and resistive load test circuits are only partially useful, as resistive loads are seldom used and very often some form of slow-rise network is used with inductive loads. Both circuits provide easy lab. measurements and the results can be guaranteed. The alternative of testing the devices in a real switchmode power supply would be too costly!

Safe Operating Area

One can distinguish between forward bias safe operating area (FBSOAR) and reverse bias safe operating area (RBSOAR). Chapter 2.1.3 deals with both subjects in more detail, a few of the main points are covered below.

Forward Bias Soar gives boundaries for d.c. operation or pulsed operation. In switching applications, where the transistor is "on" or "off", normally the excursion in the I_C-V_{CE}-plane is done very fast and in fact the designer may use the whole plane, with the boundaries I_{Cmax} and V_{CEOmax}, both as given in the ratings. This is useful for snubberless applications and for overload e.g. conditions at switch-on of the power supply

Fig.3 gives the Forward Bias SOAR of the BUT11 and one can easily recognise the boundaries I_{Cmax}, I_{CMmax} and V_{CEOmax}, all as given in the ratings. There is a P_{totmax} (1) and I_{SB} boundary (2), that both shift at higher levels of I_C when shorter pulses are used. Note that in the upper right hand corner pulse times of 20 µs are permitted leading to the square switching SOAR.



(1) P_{totmax} and $P_{totpeak}$ max. lines
(2) Second breakdown limits (independent of temperature).
I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation
III Area of permissible operation during turn-on in single transistor converters, provided R_{BE} <= 100 Ω and t_p <= 0.6 µs.
IV Repetitive pulse operation in this region is permissible provided V_{BE} <= 0 and t_p <= 5 ms.

Fig.3 Forward bias SOAR of BUT11.

For turn-on an extra area is added (area III), while area IV is only a formal conformation of the fact that leakage currents are allowed to flow!

Reverse Bias SOAR is valid when a negative voltage or current is applied to the base during turn-off. Due to current contraction in the middle of the emitter fingers, current concentration takes place during the fall time, possibly damaging the device.

A typical example can be found in Fig.4 where for both base drive and emitter drive the RBSOAR of the BUT11 is given.

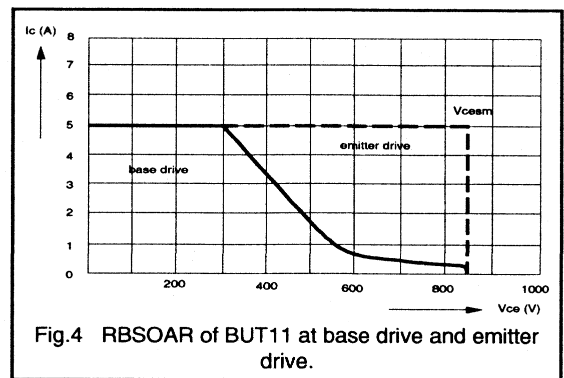


Fig.4 RBSOAR of BUT11 at base drive and emitter drive.

It is striking that for emitter drive the whole I_{Cmax}-V_{CESmax}-plane may be used so no snubber is necessary (a small snubber may prevent overshoot, however). The base drive RBSOAR normally depends on base drive conditions, but unfortunately there is no uniform trend in this behaviour. Therefore the RBSOAR curve in the data gives the worst case behaviour of the worst-case devices.

For snubber design the following rule of thumb gives a good starting value for the snubber capacitor: C = 1 nF for each 100 watts of throughput power. After checking the locus in the I_C-V_{CE}-plane with worst case drive under worst-case conditions this value may be decreased, if necessary. (More information on snubbers is given in section 1.3.3.)

Conclusions

Voltage ratings as given in the data must never be exceeded, as they may lead to immediate device destruction. Surge voltages as sometimes given for other components are not allowed for high voltage transistors. Current ratings are less strict as they are time-dependent: one should obey the Forward bias SOAR, however.

Reverse Bias SOAR is for almost all switching applications of prime importance. Philips give in their data sheets a curve for worst case devices under worst case conditions. For snubber design a value of 1 nF per 100 watts of throughput power is advised as a starter value; afterwards it must be checked whether the I_C-V_{CE} locus stays within the published RBSOAR curve.

For characteristics both saturation and switching properties are given at I_{Csat}. Most figures are of limited use as they give static conditions, where in a practical situation properties are time-dependent. Switching times are given in relatively simple circuits that may be used rather easily e.g. for incoming inspection.

Switching times depend strongly on drive conditions. Both transition frequency f_T and collector capacitance C_c are minor parameters.

CHAPTER 2

Switch Mode Power Supplies

2.1 Using Power Semiconductors in Switch Mode Topologies (including transistor selection guides)

2.2 Output Rectification

2.3 Design Examples

2.4 Magnetics Design

2.5 Resonant Power Supplies

Using Power Semiconductors in Switch Mode Topologies

2.1.1 An Introduction To Switch-Mode Power Supply Topologies.

For many years the world of power supply design has seen a gradual movement away from the use of linear power supplies to the more practical switch mode power supply (S.M.P.S.). The linear power supply contains a mains transformer and a dissipative series regulator. This means the supply has extremely large and heavy 50/60 Hz transformers, and also very poor power conversion efficiencies, both serious drawbacks. Typical efficiencies of 30% are standard for a linear. This compares with efficiencies of between 70 and 80%, currently available using S.M.P.S. designs.

Furthermore, by employing high switching frequencies, the sizes of the power transformer and associated filtering components in the S.M.P.S. are dramatically reduced in comparison to the linear. For example, an S.M.P.S. operating at 20kHz produces a 4 times reduction in component size, and this increases to about 8 times at 100kHz and above. This means an S.M.P.S. design can produce very compact and lightweight supplies. This is now an essential requirement for the majority of electronic systems. The supply must slot into an ever shrinking space left for it by electronic system designers.

Outline

At the heart of the converter is the high frequency inverter section, where the input supply is chopped at very high frequencies (20 to 200kHz using present technologies) then filtered and smoothed to produce dc outputs. The circuit configuration which determines how the power is transferred is called the TOPOLOGY of the S.M.P.S., and is an extremely important part of the design process. The topology consists of an arrangement of transformer, inductors, capacitors and power semiconductors. (Bipolar or MOSFET power transistor and power rectifiers.)

Presently, there is a very wide choice of topologies available, each one having its own particular advantages and disadvantages, making it suitable for specific power supply applications. Basic operation, advantages, drawbacks and most common areas of use for the most common topologies are discussed in the following sections. A selection guide to the Philips range of power semiconductors (including bipolars, MOSFETs and rectifiers) suitable for use in S.M.P.S. applications is given at the end of each section.

(1) Basic switch-mode supply circuit.

An S.M.P.S. can be a fairly complicated circuit, as can be seen from the block diagram shown in Fig.1. (This configuration assumes a 50/60Hz mains input supply is used.) The ac supply is first rectified, and then filtered by the input reservoir capacitor to produce a rough dc input supply. This level can fluctuate widely due to variations in the mains. In addition the capacitance on the input has to be fairly large to hold up the supply in case of a severe droop in the mains. (The S.M.P.S. can also be configured to operate from any suitable dc input, in this case the supply is called a dc to dc converter.)

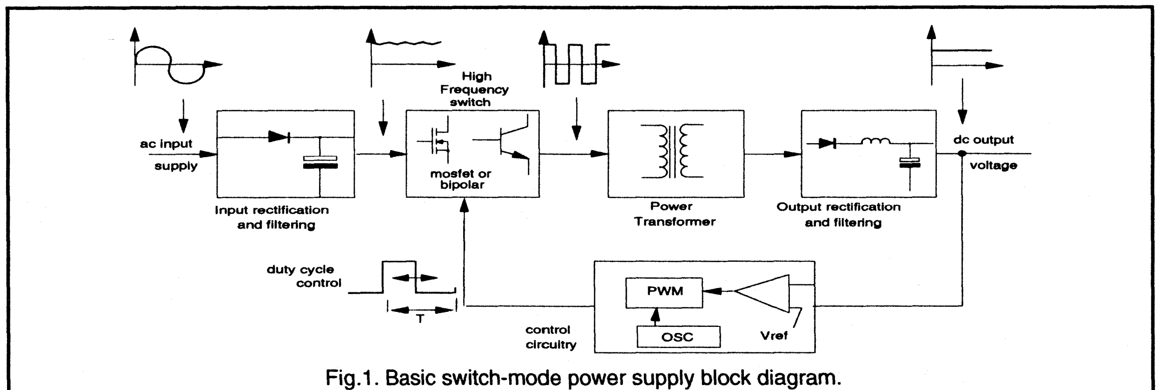


Fig.1. Basic switch-mode power supply block diagram.

The unregulated dc is fed directly to the central block of the supply, the high frequency power switching section. Fast switching power semiconductor devices such as MOSFETs and Bipolars are driven on and off, and switch the input voltage across the primary of the power transformer. The drive pulses are normally fixed frequency (20 to 200kHz) and variable duty cycle. Hence, a voltage pulse train of suitable magnitude and duty ratio appears on the transformer secondaries. This voltage pulse train is appropriately rectified, and then smoothed by the output filter, which is either a capacitor or capacitor / inductor arrangement, depending upon the topology used. This transfer of power has to be carried out with the lowest losses possible, to maintain efficiency. Thus, optimum design of the passive and magnetic components, and selection of the correct power semiconductors is critical

Regulation of the output to provide a stabilised dc supply is carried out by the control / feedback block. Generally, most S.M.P.S. systems operate on a fixed frequency pulse width modulation basis, where the duration of the on time of the drive to the power switch is varied on a cycle by cycle basis. This compensate for changes in the input supply and output load. The output voltage is compared to an accurate reference supply, and the error voltage produced by the comparator is used by dedicated control logic to terminate the drive pulse to the main power switch/switches at the correct instance. Correctly designed, this will provide a very stable dc output supply.

It is essential that delays in the control loop are kept to a minimum, otherwise stability problems would occur. Hence, very high speed components must be selected for the loop. In transformer-coupled supplies, in order to keep the isolation barrier intact some type of electronic isolation is required in the feedback. This is usually achieved by using a small pulse transformer or an opto-isolator, hence adding to the component count.

In most applications, the S.M.P.S. topology contains a power transformer. This provides isolation, voltage scaling through the turns ratio, and the ability to provide multiple outputs. However, there are non-isolated topologies (without transformers) such as the buck and the boost converters, where the power processing is achieved by inductive energy transfer alone. All of the more complex arrangements are based on these non-isolated types.

(2) Non-Isolated converters.

The majority of the topologies used in todays converters are all derived from the following three non-isolated versions called the buck, the boost and the buck-boost. These are the simplest configurations possible, and have the lowest component count, requiring only one inductor, capacitor, transistor and diode to generate their single output. If isolation between the input and output is required, a transformer must be included before the converter.

(a) The Buck converter.

The forward converter family which includes the push-pull and bridge types, are all based on the buck converter, shown in Fig.2. It's operation is straight-forward. When switch, TR1 is turned on, the input voltage is applied to inductor, L1, and power is delivered to the output. Inductor current also builds up according to Faraday's law shown below:-

$$V = L\frac{dI}{dt}$$

When the switch is turned off, the voltage across the inductor reverses and freewheel diode, D1 becomes forward bias. This allows the energy stored in the inductor to be delivered to the output. This continuous current is then smoothed by output capacitor Co. Typical buck waveforms are also shown in Fig.2.

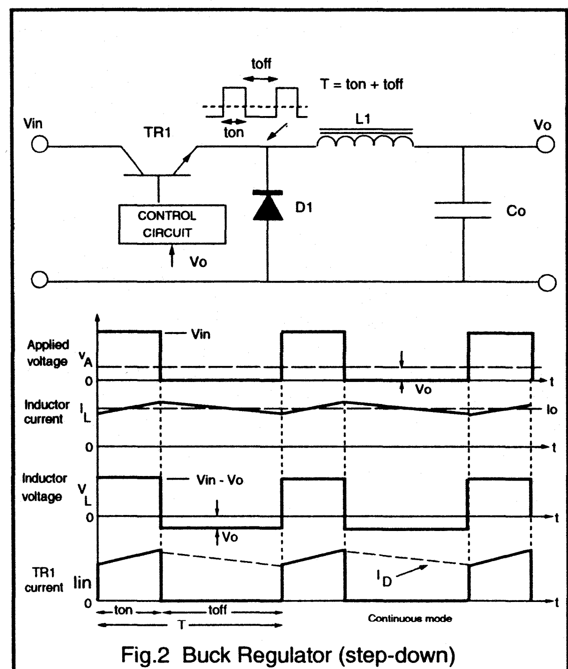


Fig.2 Buck Regulator (step-down)

The LC filter has an averaging effect on the applied pulsating input, producing a smooth dc output voltage and current, with very small ripple components superimposed. The average voltage/sec across the inductor over a complete switching cycle must equal zero in the steady state. (The same applies to all of the regulators that will be discussed.)

Neglecting circuit losses, the average voltage at the input side of the inductor is $V_{in}D$, and V_o, the output side voltage. Thus, in the steady state for the average voltage across the inductor to be zero, the basic dc equation of the buck is simply:-

$$\frac{V_o}{V_i}=D$$

D is the transistor switch duty cycle, defined as the conduction time divided by one switching period, usually expressed in the form shown below:-

$$D=\frac{t_{on}}{T}; \quad where \quad T=t_{on}+t_{off}$$

Thus, the buck is a step down type, where the output voltage is always lower than the input. (Since D never reaches one.) Output voltage regulation is provided by varying the duty cycle of the switch. The LC arrangement provides very effective filtering of the inductor current. Hence, the buck and it's derivatives all have very low output ripple characteristics. The buck is normally always operated in continuous mode (inductor current never falls to zero) where peak currents are lower, and the smoothing capacitor requirements are smaller. There are no major control problems with the continuous mode buck.

(b) The Boost Regulator.

Operation of another fundamental regulator, the boost, shown in Fig.3 is more complex than the buck. When the switch is on, diode D1 is reverse biased, and V_{in} is applied across inductor, L1. Current builds up in the inductor to a peak value, either from zero current in a discontinuous mode, or an initial value in the continuous mode. When the switch turns off, the voltage across L1 reverses, causing the voltage at the diode to rise above the input voltage. The diode then conducts the energy stored in the inductor, plus energy direct from the supply to the smoothing capacitor and load. Hence, V_o is always greater than V_{in}. For continuous mode operation, the boost dc equation is obtained by a similar process as for the buck, and is given below:-

$$\frac{V_o}{V_i}=\frac{1}{1-D}$$

Again, the output only depends upon the input and duty cycle. Thus, by controlling the duty cycle output regulation is achieved.

From the boost waveforms shown in Fig.3, it is clear that the current supplied to the output smoothing capacitor from the converter is the diode current, which will always be discontinuous. This means that the output capacitor must be large, with a low equivalent series resistance (e.s.r) to produce a relatively acceptable output ripple. This is in contrast with the buck output capacitor requirements described earlier. On the other hand, the boost input current is the continuous inductor current, and this provides low input ripple characteristics. The boost is very popular for capacitive load applications such as photo-flashers and battery chargers. Furthermore, the continuous input current makes the boost a popular choice as a pre-regulator, placed before the main converter. The main functions being to regulate the input supply, and to greatly improve the line power factor. This requirement has become very important in recent years, in a concerted effort to improve the power factor of the mains supplies.

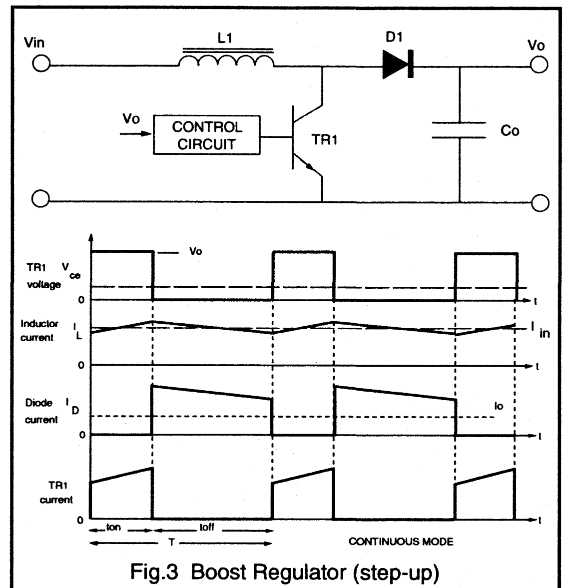


Fig.3 Boost Regulator (step-up)

If the boost is used in discontinuous mode, the peak transistor and diode currents will be higher, and the output capacitor will need to be doubled in size to achieve the same output ripple as in continuous mode. Furthermore, in discontinuous operation, the output voltage also becomes dependent on the load, resulting in poorer load regulation.

Unfortunately, there are major control and regulation problems with the boost when operated in continuous mode. The pseudo LC filter effectively causes a complex second order characteristic in the small signal (control) response. In the discontinuous mode, the energy in the inductor at the start of each cycle is zero, this removes the inductance from the small signal response, leaving only the output capacitance effect. This produces a much simpler response, which is far easier to compensate and control.

(c) The Buck-Boost Regulator (Non-isolated Flyback).

The very popular flyback converter (see section 5(a)) is not actually derived solely from the boost. The flyback only delivers stored inductor energy during the switch off time, the boost however, also delivers energy from the input. The flyback is actually based on a combined topology of the previous two, called the buck-boost or non isolated flyback regulator. This topology is shown in Fig.4.

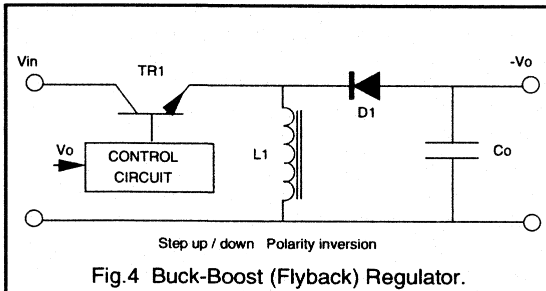


Fig.4 Buck-Boost (Flyback) Regulator.

When the switch is on ,the diode is reverse biased and the input is connected across the inductor, which stores energy as previously explained. At turn off, the inductor voltage reverses, and the stored energy is then passed to the capacitor and load through the forward biased rectifier diode.

The waveforms are similar to the boost, except that the transistor switch now has to support the sum of Vin and Vo across it. Clearly, both the input and output currents must be discontinuous. There is also a polarity inversion, the output voltage generated is negative with respect to the input. Close inspection reveals that the continuous mode dc transfer function is as shown below:-

$$\frac{V_o}{V_i} = \frac{D}{1-D}$$

Observation shows that the value of the switch duty ratio, D can be selected such that the output voltage can either be higher or lower than the input voltage. This gives the converter the flexibility to either step up or down the supply.

This regulator also suffers from the same continuous mode control problems as the boost, and discontinuous mode is usually favoured.

Since, both input and output currents are pulsating, low ripple levels are very difficult to achieve using the buck-boost. Very large output filter capacitors are needed, typically up to 8 times that of a buck regulator.
The transistor switch also needs to be able to conduct the high peak current, as well as supporting the higher summed voltage. The flyback regulator (buck-boost) topology places the most stress on the transistor. The rectifier diode also has to carry high peak currents and so the r.m.s conduction losses will be higher than those of the buck.

(3) Transformers in S.M.P.S. converters.

The non-isolated versions have very limited use, such as dc-dc regulators only capable of producing a single output. The output range is also limited by the input and duty cycle. The addition of a transformer removes most of these constraints and provides a converter with the following advantages:-

1) Input to output isolation is provided. This is normally always necessary for 220 / 110 V mains applications, where a degree of safety is provided for the outputs.

2) The transformer turns ratio can be selected to provide outputs widely different from the input, non-isolated versions are limited to a range of approximately 5 times. By selecting the correct turns ratio, the duty cycle of the converter can also be optimised and the peak currents flowing minimised. The polarity of each output is also selectable, dependent upon the polarity of the secondary w.r.t the primary.

3) Multiple outputs are very easily obtained, simply by adding more secondary windings to the transformer.

There are some disadvantages with transformers such as their additional size, weight and power loss. The generation of voltage spikes due to leakage inductance may also be a problem.

The isolated converters to be covered are split into two main categories, called asymmetrical and symmetrical converters, depending upon how the transformer is operated.

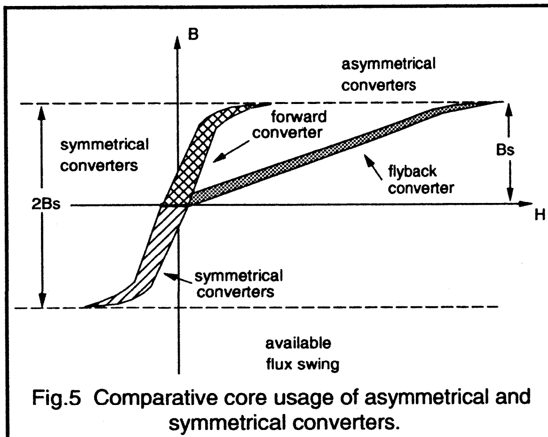


Fig.5 Comparative core usage of asymmetrical and symmetrical converters.

In asymmetrical converters the magnetic operating point of the transformer is always in one quadrant i.e the flux and the magnetic field never changes sign. The core has to be reset each cycle to avoid saturation, meaning that only half of the usable flux is ever exploited. This can be seen in Fig.5, which shows the operating mode of each converter. The flyback and forward converter are both asymmetrical types. The diagram also indicates that the flyback converter is operated at a lower permeability (B/H) and lower inductance than the others. This is because the flyback transformer actually stores all of the energy before dumping into the load, hence an air gap is required to store this energy and avoid core saturation. The air gap has the effect of reducing the overall permeability of the core. All of the other converters have true transformer action and ideally store no energy, hence, no air gap is needed.

In the symmetrical converters which always require an even number of transistor switches, the full available flux swing in both quadrants of the B / H loop is used, thus, utilising the core much more effectively. Symmetrical converters can therefore produce more power than their asymmetrical cousins. The 3 major symmetrical topologies used in practise are the push-pull, the half-bridge and the full bridge types.

Table.1 outlines the typical maximum output power available from each topology using present day technologies:-

Converter Topology	Typical max output power
Flyback	200W
Forward	300W
Two transistor forward / flyback	400W
Push-pull	500W
Half-Bridge	1000W
Full-Bridge	>1000W

Table.1 Converter output power range

Many other topologies exist, but the types outlined in Table.1 are by far the most commonly used in present S.M.P.S. designs. Each is now looked at in more detail, with a selection guide for the most suitable Philips power semiconductors included.

(4) Selection of the power semiconductors.

The Power Transistor.

The two most common power semiconductors used in the S.M.P.S. are the Bipolar transistor and the power MOSFET. The Bipolar transistor is normally limited to use at frequencies up to 30kHz, due to switching loss. However, it has very low on-state losses and is a relatively cheap device, making it the most suitable for lower frequency applications. The MOSFET is selected for higher frequency operation because of its very fast switching speeds, resulting in low (frequency dependent) switching losses. The driving of the MOSFET is also far simpler and less expensive than that required for the Bipolar. However, the on-state losses of the MOSFET are far higher than the Bipolar, and they are also usually more expensive. The selection of which particular device to use is normally a compromise between the cost, and the performance required.

(i) Voltage rating:-

After deciding upon wether to use a Bipolar or MOSFET, the next step in deciding upon a suitable type, is by the correct selection of the transistor voltage rating. For transformer coupled topologies, the maximum voltage developed across the device is normally at turn off. This will be either half, full or double the magnitude of the input supply voltage, dependent upon the topology used. There may also be a significant voltage spike due to transformer leakage inductance that must be included. The transistor must safely withstand these worst case values without breaking down. Hence, for a bipolar device, a suitably high $V_{ces(max)}$ must be selected, and for a MOSFET, a suitably high $V_{BR(DSS)}$. At present 1500V is the maximum blocking voltage available for power Bipolars, and a maximum of 1000V for power MOSFETs.

The selection guides assume that a rectified 220V or 110V mains input is used. The maximum dc link voltages that will be produced for these conditions are 385V and 190V respectively. These values are the input voltage levels used to select the correct device voltage rating.

(ii) Current rating:-

The Bipolar device has a very low voltage drop across it during conduction, which is relatively constant within the rated current range. Hence, for maximum utilisation of a bipolar transistor, it should be run close to its I_{Csat} value. This gives a good compromise between cost, drive requirements and switching. The maximum current for a particular throughput power is calculated for each topology using simple equations. These equation are listed in the appropriate sections, and the levels obtained used to select a suitable Bipolar device.

The MOSFET device operates differently from the bipolar in that the voltage developed across it (hence, transistor dissipation) is dependent upon the current flowing and the device " on-resistance" which is variable with temperature. Hence, the optimum MOSFET for a given converter can only be chosen on the basis that the device must not exceed a certain percentage of throughput (output) power. (In this selection a 5% loss in the MOSFET was assumed). A set of equations used to estimate the correct MOSFET $R_{DS(on)}$ value for a particular power level has been derived for each topology. These equations are included in Appendix.A at the end of the paper. The value of RDS(on) obtained was then used to select a suitable MOSFET device for each requirement.

NOTE! This method assumes negligible switching losses in the MOSFET, however for frequencies above 50kHz switching losses become increasingly significant.

Rectifiers

Two types of output rectifiers are specified from the Philips range. For very low output voltages, below 10V it is necessary to have an extremely low rectifier forward voltage drop, V_F, in order to keep converter efficiency high. Schottky types are specified here, since they have very low V_F values (typically 0.5V). The Schottky also has negligible switching losses and can be used at very high frequencies. Unfortunately, the very low V_F of the Schottky is lost at higher reverse blocking voltages (typically above 50V) and other diode types become more suitable. This means that the Schottky is normally reserved for use on very low outputs.

Note. A suitable guide to selecting the correct rectifier reverse voltage, is to ensure the device will block up to 5 times the output voltage it is used to provide.

For higher voltage outputs the most suitable rectifier is the fast recovery epitaxial diode (FRED). This device has been optimised for the use in high frequency rectification. Its characteristics include low V_F (approx. 1V) with very fast and efficient switching characteristics. The FRED has reverse voltage blocking capabilities up to 1000V. They are therefore, suitable for use in outputs from 10 to 200V.

The rectifier devices specified in each selection guide were chosen as having the correct voltage rating, and high enough current handling capability for the particular output power specified. (A single output is assumed).

(5) Standard isolated topologies.

(a) The Flyback converter.

Operation

Of all the isolated converters, by far the simplest is the single-ended flyback converter shown in Fig.6. The use of a single transistor switch means that the transformer can only be driven unipolar (asymmetrical). This results in a large core size. The flyback, which is an isolated version of the buck-boost does not in truth contain a transformer, but a coupled inductor arrangement. When the transistor is turned on, current builds up in the primary and energy is stored in the core, this energy is then released to the output circuit through the secondary when the switch is turned off. (A normal transformer such as the types used in the buck derived topologies, couples the energy directly during transistor on time, ideally storing no energy).

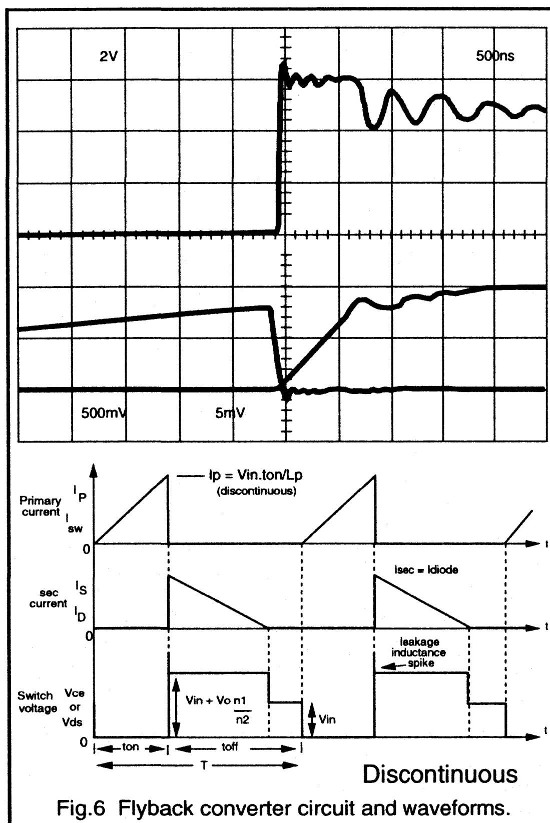


Fig.6 Flyback converter circuit and waveforms.

The polarity of the windings is such that output diode blocks during the transistor on time. When the transistor turns off the secondary voltage reverses maintaining a constant flux in the core, forcing secondary current to flow through the diode to the output load. The magnitude of the peak secondary current, is the peak primary current reached at transistor turn off, reflected through the turns ratio, thus maintaining a constant Ampere-turn balance.

The fact that all of the output power of the flyback has to be stored in the core as $1/2LI^2$ energy, means that the core size and cost will be much greater than in the other topologies, where only the core excitation (magnetisation) energy, which is normally small, is stored. This in addition to the initial poor unipolar core utilisation means that the transformer bulk is one of the major drawbacks of the flyback.

In order to obtain sufficiently high stored energy, the flyback primary inductance has to be significantly lower than required for a true transformer, since high peak currents are needed. This is normally achieved by gapping the core. The gap reduces the inductance, and most of the high peak energy is then stored in the gap, thus, avoiding transformer saturation.

When the transistor turns off, the output voltage is back reflected thro the transformer to the primary and in many cases this can be nearly as high as the supply voltage. There is also a voltage spike at turn off due to the stored energy in the transformer leakage inductance. This means that the transistor must be capable of blocking approximately twice the supply voltage plus the leakage spike. Hence, for a 220V ac application where the dc link can be up to 385V, the transistor voltage rating must lie between 800 and 1000V.

Using a 1000V rated Bipolar transistor such as the BUT11A or BUW13A allows a switching frequency of 30kHz to be used, at output powers up to 200Watts. Furthermore, an emitter switching technique (Reference[1]) permits Bipolar switching at up to 100kHz.

MOSFETs rated at 800 and 1000V can also be used, such as the BUK456-800A which can supply 100W at switching frequencies any where up to 300KHz. Although the MOSFET can be switched much faster and has lower switching losses , it does suffer from significant on state losses, especially in the higher voltage devices compared to the bipolars. An outline of suitable transistors and output rectifiers for different input and power levels using the flyback is given in Table.2.

One way of removing the transformer leakage voltage spike is to add a clamp winding as shown in Fig.6. This allows the leakage energy to be returned to the input instead of stressing the transistor. The diode is always placed at the high voltage end, so that the clamp winding capacitance does not interfere with the transistor turn on current spike which would happen if the diode was connected to ground. This clamp is optional and depends on the designer's particular requirements.

Advantages.

The action of the flyback means that the secondary inductance is in series with the output diode when current is delivered to the load i.e driven from a current source. This means that no filter inductor is needed in the output circuit. Hence, each output requires only one diode and output filter capacitor. This means the flyback is the ideal choice for generating low cost, multiple output supplies. The cross regulation obtained using multiple outputs is also very good (load changes on one output have little effect on the others) because of the absence of the output choke, which degrades this dynamic performance.

The flyback is also ideally suited for generating high voltage outputs. If a buck type LC filter was used to generate a high voltage, a very large inductance value would be needed to reduce the ripple current levels sufficiently to achieve the continuous mode operation required. This restriction does not apply to the flyback, since it does not require an output inductance for successful operation

Disadvantages.

From the flyback waveforms in Fig.6 it is clear that the output capacitor is only supplied during the transistor off time. This means that the capacitor has to smooth a pulsating output current which has higher peak values than the continuous output current that would be produced in a forward converter for example. In order to achieve low output ripple, very large output capacitors are needed, with very low equivalent series resistance (e.s.r). It can be shown that at the same frequency, an LC filter is approximately 8 times more effective at ripple reduction than a capacitor alone, hence, flybacks have inherently much higher output ripples than other topologies. This together with the higher peak currents, large capacitors and transformers limits the flyback to lower output power applications in the 20 to 200Watt range. (It should be noted that at higher voltages, the required output voltage ripple magnitudes are not normally as stringent, and this means that the e.s.r requirement and hence capacitor size will not be as large as expected.)

Two transistor flyback.

One possible solution to the 1000V transistor requirement is the two transistor flyback version shown in Fig.7. Both transistors are switched simultaneously, and all waveforms are exactly the same, except that the voltage across each transistor never exceeds the input voltage . The clamp winding is now redundant, since the two clamp diodes act to return leakage energy to the input. Two 400 or 500V devices can now be selected, which will have faster switching and lower conduction losses. The output power and switching frequencies can thus, be significantly increased. The drawbacks of the two transistor version are the extra cost and more complex isolated gate drive needed for the top floating transistor.

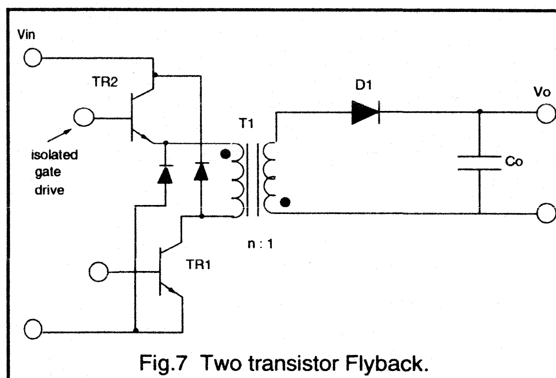


Fig.7 Two transistor Flyback.

Continuous Vs Discontinuous operation.

As with the buck-boost, the flyback can operate in both continuous and discontinuous modes. The waveforms in Fig.6 show discontinuous mode operation. In discontinuous mode, the secondary current falls to zero in each switching period, and all of the energy is removed from the transformer. In continuous mode there is current flowing in the coupled inductor at all times, resulting in trapezoidal current waveforms.

The main plus of continuous mode is that the peak currents flowing are only half that of the discontinuous for the same output power, hence, lower output ripple is possible. However, the core size is about 2 to 4 times larger in continuous mode to achieve the increased inductance needed to reduce the peak currents to achieve continuity.

A further disadvantage of continuous mode is that the closed loop is far more difficult to control than the discontinuous mode flyback. (Continuous mode contains a right hand plane zero in its open loop frequency response, the discontinuous flyback does not. See Ref[3] for further explanation.) This means that much more time and effort is required for continuous mode to design the much more complicated compensation components needed to achieve stability.

There is negligible turn on dissipation in the transistor in discontinuous mode, whereas, this dissipation can be fairly high in continuous mode, especially when the additional effects of the output diode reverse recovery current, which only occurs in the continuous case is included. This normally means that a snubber must be added to protect the transistor against switch-on stresses.

One advantage of the continuous mode is that its open loop gain is independent of the output load i.e V_o only depends upon D and V_{in} as shown in the dc gain equation at the end of the section. Continuous mode has excellent open loop load regulation i.e varying the output load will not effect V_o. Discontinuous mode, on the other-hand does have a dependency on the output, expressed as R_L in the dc gain equation. Hence, discontinuous mode has a much poorer

open loop load regulation i.e changing the output will effect V_o. This problem disappears however, when the control loop is closed and the load regulation problem is usually completely overcome.

The use of current mode control with discontinuous flyback (where both the primary current and output voltage are sensed and combined to control the duty cycle) produces a much improved overall loop regulation, requiring less closed loop gain.

Although the discontinuous mode has the major disadvantage of very high peak currents and a large output capacitor requirement, it is much easier to implement, and is by far the more common of the two methods used in present day designs.

Output power	50W		100W		200W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements Max current Max voltage	2.25A 400V	1.2A 800V	4A 400V	2.5A 800V	8A 400V	4.4A 800V
Bipolar transistors. TO-220 Isolated SOT-186 SOT-93 Isolated SOT-93		BUX85 BUX85F --- ---	BUV28A BUV28AF --- ---	BUT11A BUT11AF --- ---	BUV28A BUV28AF --- ---	--- --- BUT12A BUT12AF
Power MOSFET TO-220 isolated SOT-186 SOT-93 isolated SOT-199	BUK454-400B BUK444-400B --- ---	BUK454-800A BUK444-800A --- ---	BUK455-400B BUK445-400B --- ---	BUK456-800A BUK446-800A --- ---	--- --- BUK437-400B BUK427-400B	--- --- BUK438-800A BUK428-800A
Output Rectifiers O/P voltage 5V 10V 20V 50V 100V	PBYR1635 BYW29-100 BYW29-200 BYV29-300 BYV29-500		PBYR2035 BYV79-100 BYW29-200 BYV29-300 BYV29-500		BYV42-100 BYV42-200 BYV29-300 BYV29-500	

Table.2 Recommended Power Semiconductors for single-ended flyback.

Note! The above values are for discontinuous mode, in continuous mode the peak transistor currents are approximately halved, and the output power available thus increased.

<u>Flyback</u>

Converter efficiency, $\eta = 80\%$; Max duty cycle, $D_{max} = 0.45$

Max transistor voltage, V_{Ce} or $V_{ds} = 2V_{in(max)}$ + leakage spike

$$\text{Max transistor current}, I_C \quad ; \quad I_D = 2\frac{P_{out}}{\eta \quad D_{max} \quad V_{min}}$$

dc voltage gain:- (a) continuous $\frac{Vo}{Vin} = n\frac{D}{1-D}$ (b) Discontinuous $\frac{Vo}{Vin} = D\sqrt{\frac{R_L}{2}\frac{T}{L_p}}$

<u>Applications:-</u> Lowest cost, multiple output supplies in the 20 to 200W range e.g mains input T.V supplies, small computer supplies, E.H.T supplies.

(b) The Forward converter.

Operation.

The forward converter is also a single switch isolated topology, and is shown in Fig.8. This is based on the buck converter described earlier, with the addition of a transformer and another diode in the output circuit. The characteristic LC output filter is clearly present.

In contrast to the flyback, the forward converter has a true transformer action, where energy is transferred directly to the output through the inductor during the transistor on time. It can be seen that the polarity of the secondary winding is opposite that of the flyback, hence, allowing direct current flow through blocking diode D1. During the on time the current flowing causes energy to be built up in the output inductor, L1. When the transistor turns off, the secondary voltage reverses, D1 then goes from conduction to blocking mode and the freewheel diode, D2 then becomes forward biased and provides a path for the inductor current to continue to flow. This allows the energy stored in L1 to be released into the load during the transistor off time.

The forward converter is always operated in continuous mode (in this case the output inductor current), since this produces very low peak input and output currents and small ripple components. Going into discontinuous mode would greatly increase these values, as well as increasing the amount of switching noise generated. No destabilising right hand plane zero occurs in the frequency response of the forward in continuous mode (as with the buck). See Ref[3]. This means that the control problems that existed with the continuous flyback are not present here. So there are no real advantages to be gained by using discontinuous mode operation for the forward converter.

Advantages.

As can be seen from the waveforms in Fig.8, the inductor current, I_L which is also the output current, is always continuous. The magnitude of the ripple component, and hence, the peak secondary current, depends upon the size of the output inductor. Therefore, the ripple can be made relatively small compared to the output current, with the peak current minimised. This low ripple, continuous output current is very easy to smooth, and so the requirements for the output capacitor size, e.s.r and peak current handling are far smaller than they are for the flyback.

Since the transformer in this topology transfers energy directly there is negligible stored energy in the core compared to the flyback. However, there is a small magnetisation energy required to excite the core, allowing it to become an energy transfer medium. This energy is very small and only a very small primary magnetisation current is needed. This means that a high primary inductance is usually suitable, with no need for the core air gap required in the flyback. Standard un-gapped ferrite cores with high permeabilities (2000-3000) are ideal for providing the high inductance required. Negligible energy storage means that the forward converter transformer is considerably smaller than the flyback, and core loss is also much smaller for the same throughput power. However, the transformer is still operated asymmetrically, which means that power is only transferred during the switch on time, and this poor utilisation means the transformer is still far bigger than in the symmetrical types.

The transistors have the same voltage rating as the discontinuous flyback (see disadvantages) , but the peak current required for the same output power is halved, and this can be seen in the equations given for the forward converter. This, coupled with the smaller transformer and output filter capacitor requirements means that the forward converter is suitable for use at higher output powers than the flyback can attain, and is normally designed to operate in the 100 to 400W range. Suitable bipolars and MOSFETs for the forward converter are listed in Table.3.

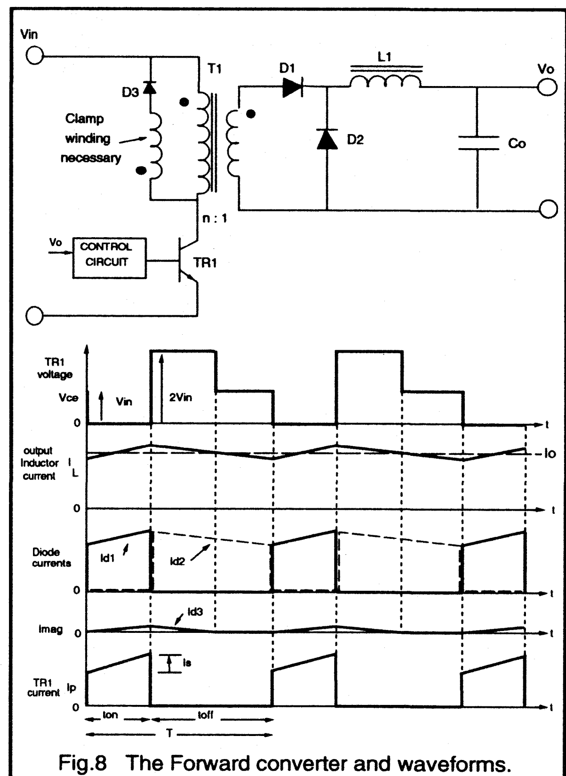


Fig.8 The Forward converter and waveforms.

Disadvantages.

Because of the unipolar switching action of the forward converter, there is a major problem in how to remove the core magnetisation energy by the end of each switching cycle. If this did not happen, there would be a net dc flux build-up, leading to core saturation, and possible transistor destruction. This magnetisation energy is removed automatically by the push-pull action of the symmetrical types. In the flyback this energy is dumped into the load at transistor turn off. However, there is no such path in the forward circuit.

This path is provided by adding an additional reset winding of opposite polarity to the primary. A clamp diode is added, such that the magnetisation energy is returned to the input supply during the transistor off time. The reset winding is wound bifilar with the primary to ensure good coupling, and is normally made to have the same number of turns as the primary. (The reset winding wire gauge can be very small, since it only has to conduct the small magnetisation current.) The time for the magnetisation energy to fall to zero is thus, the same duration as the transistor on time. This means that the maximum theoretical duty ratio of the forward converter is 0.5 and after taking into account switching delays, this falls to 0.45. This limited control range is one of the drawbacks of using the forward converter. The waveform of the magnetisation current is also shown in Fig.8. The clamp winding in the flyback is optional, but is always needed in the forward for correct operation.

Due to the presence of the reset winding, in order to maintain volt-sec balance within the transformer, the input voltage is back reflected to the primary from the clamp winding at transistor turn off for the duration of the flow of the magnetisation reset current through D3. (There is also a voltage reversal across the secondary winding, and this is why diode D1 is added to block this voltage from the output circuit) This means that the transistor must block two times Vin during switch off. The voltage returns to Vin after reset has finished, which means transistor turn on losses will be smaller. The transistors must have the same added burden of the voltage rating of the flyback i.e 400V for 110V mains and 800V for 220V mains applications.

Output diode selection.

The diodes in the output circuit both have to conduct the full magnitude of the output current. They are also subject to abrupt changes in current causing a reverse recovery spike, particularly in the freewheel diode, D2. This spike can cause additional turn on switching loss in the transistor, possibly causing device failure in the absence of snubbing. Thus, very high efficiency, fast trr diodes are required, to minimise conduction losses and to reduce the reverse recovery spike. These requirements are met with Schottky diodes for very low outputs below 10V, and fast recovery epitaxial diodes for higher voltage outputs. It is not normal for forward converter outputs to exceed 100V because of the need for a very large output choke, and flybacks are normally used. Usually, both rectifiers are included in a single package i.e a dual centre-tap arrangement. The Philips range of Schottkies and FREDs which meet these requirements are also included in Table.3.

Two transistor forward.

In order to avoid the use of higher voltage transistors, the two transistor version of the forward can be used. This circuit shown in Fig.9 is very similar to the two transistor flyback and has the same advantages. The voltage across the transistor is again clamped to V_{in}, allowing the use of faster more efficient 400 or 500V devices for 220V mains applications. The magnetisation reset is achieved through the two clamp diode, permitting the removal of the clamp winding.

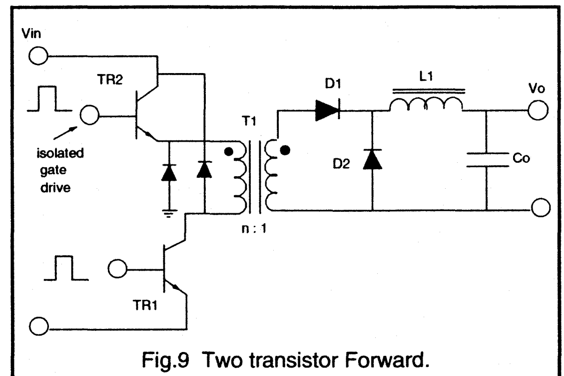


Fig.9 Two transistor Forward.

The two transistor version is popular for off-line applications. It provides higher output powers and faster switching frequencies. The disadvantages are again the extra cost of the higher component count, and the need for an isolated drive for the top transistor.

Although this converter has some drawbacks, and utilises the transformer poorly, it is a very popular selection for the power range mentioned above, and offers simple drive for the single switch and cheap component costs. Multiple output types are very common. The output inductors are normally wound on a single core, which has the effect of improving dynamic cross regulation, and if designed correctly also reduces the output ripple magnitudes even further. The major advantage of the forward converter is the very low output ripple that can be achieved for relatively small sized LC components. This means that forward converters are normally used to generate lower voltage, high current multiple outputs such as 5, 12, 15, 28V from mains off-line applications, where lower ripple specifications are normally specified for the outputs. The high peak currents that would occur if a flyback was used would place an impossible burden on the smoothing capacitor.

Output power	100W		200W		300W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements Max current Max voltage	 2.25A 400V	 1.2A 800V	 4A 400V	 2.5A 800V	 6A 400V	 3.3A 800V
Bipolar transistors. TO-220 Isolated SOT-186 SOT-93 Isolated SOT-93		 BUX85 BUX85F --- ---	 BUV28A BUV28AF --- ---	 BUT11A BUT11AF --- ---	 BUV28A BUV28AF --- ---	 --- --- BUT12A BUT12AF
Power MOSFET TO-220 isolated SOT-186 SOT-93 isolated SOT-199	 BUK454-400B BUK444-400B --- ---	 BUK454-800A BUK444-800A --- ---	 BUK455-400B BUK445-400B --- ---	 BUK456-800A BUK446-800A --- ---	 --- --- BUK437-400B BUK427-400B	 --- --- BUK438-800A BUK428-800A
Output Rectifiers (dual) O/P voltage 5V 10V 20V 50V	 PBYR2035 BYV32-100 BYV32- 200 BYT28-300		 PBYR2535 BYV32-100 BYV32-200 BYT28-300		 PBYR12035T BYV42-100 BYV32-200 BYT28-300	

Table.3 Recommended Power Semiconductors for single-ended forward.

Forward

Converter efficiency, η = 80%; Max duty cycle, D_{max} = 0.45

Max transistor voltage, V_{Ce} or $V_{ds} = 2V_{in(max)}$

$$\text{Max transistor current}, I_C \; ; \; I_D = \frac{P_{out}}{\eta \; D_{max} \; V_{min}}$$

dc voltage gain:- $\frac{Vo}{Vin} = n \; D$

Applications:- Low cost, low output ripple, multiple output supplies in the 50 to 400W range e.g. Small computer supplies, DC/DC converters.

(c) The Push-pull converter.

Operation.

To utilise the transformer flux swing fully, it is necessary to operate the core symmetrically as described earlier. This permits much smaller transformer sizes and provides higher output powers than possible with the single ended types. The symmetrical types always require an even number of transistor switches. One of the best known of the symmetrical types is the push-pull converter shown in Fig.9.

The primary is a centre-tapped arrangement and each transistor switch is driven alternately, driving the transformer in both directions. The push-pull transformer is typically half the size of that for the single ended types, resulting in a more compact design. This push-pull action produces natural core resetting during each half cycle, hence no clamp winding is required. Power is transferred to the buck type output circuit during each transistor conduction period. The duty ratio of each switch is usually less than 0.45. This provides enough dead time to avoid transistor cross conduction. The power can now be transferred to the output for up to 90% of the switching period, hence allowing greater throughput power than with the single-ended types. The push-pull configuration is normally used for output powers in the 100 to 500W range.

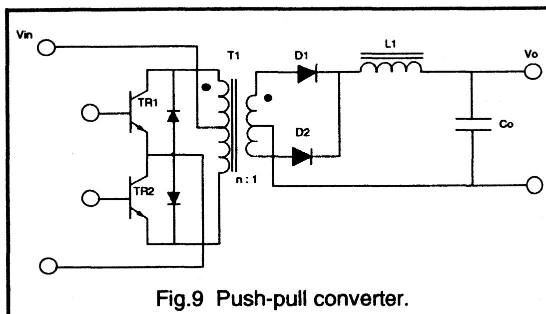


Fig.9 Push-pull converter.

The bipolar switching action also means that the output circuit is actually operated at twice the switching frequency of the power transistors, as can be seen from the waveforms in Fig.10. Therefore, the output inductor and capacitor can be even smaller for similar output ripple levels. Push-pull converters are thus excellent for high power density, low ripple outputs.

Advantages.

As stated, the push-pull offers very compact design of the transformer and output filter, while producing very low output ripple. So if space is a premium issue, the push-pull could be suitable. The control of the push-pull is similar to the forward, in that it is based on the continuous mode buck again. When closing the feedback control loop, compensation is relatively easy. For multiple outputs, the same recommendations given for the forward converter apply.

Clamp diodes are fitted across the transistors, as shown. This allows leakage and magnetisation energy to be simply channelled back to the supply, reducing stress on the switches, and slightly improving efficiency.

The emitter or source of the power transistors are both at the same potential in the push-pull configuration, and are normally referenced to ground. This means that simple base drive can be used for both, and no costly isolating drive transformer is required. (This is not so for the bridge types which are discussed latter.)

Disadvantages.

One of the main drawbacks of the push-pull converter is the fact that each transistor must block twice the input voltage due to the doubling effect of the centre-tapped primary, even though two transistors are used. This occurs when one transistor is off and the other is conducting. When both are off, each then blocks the supply voltage, this is shown in the waveforms in Fig.10 This means that TWO expensive, less efficient 800 to 1000V transistors would be required for a 220V off-line application. A selection of transistors and rectifiers suitable for the push-pull used in off-line applications is given in Table.4.

A further major problem with the push-pull is that it is prone to flux symmetry imbalance. If the flux swing each half cycle is not exactly symmetrical, the volt-sec will not balance and this will result in transformer saturation, particularly for high input voltages. Symmetry imbalance can be caused by different characteristics in the two transistors such as storage time in a bipolar and different on state losses.

The centre-tap arrangement also means that extra copper is needed for the primary, and very good coupling between the two halves is necessary to minimise possible leakage spikes. It should also be noted that if snubbers are used to protect the transistors, the design must be very precise since each tends to interact with the other. This is true for all symmetrically driven converters.

These disadvantages usually dictate that the push-pull is normally operated at lower voltage inputs such as 12, 28 or 48V. dc/dc converters found in the automotive and telecommunication industries are often push-pull designs. At these voltage levels, transformer saturation is easier to avoid.

Since, the push-pull is commonly operated with low dc voltages, a selection guide for suitable power MOSFETs is also included for 48 and 96V applications, seen in Table.5

Current mode control.

The introduction of current mode control circuits has also benefited the push-pull type. In this type of control, the primary current is monitored, and any imbalance which occurs is corrected on a cycle by cycle basis by varying the duty cycle immediately. Current mode control completely removes the symmetry imbalance problem, and the possibilities of saturation are minimised. This has meant that push-pull designs have become more popular in recent years, with some designers even using them in off-line applications.

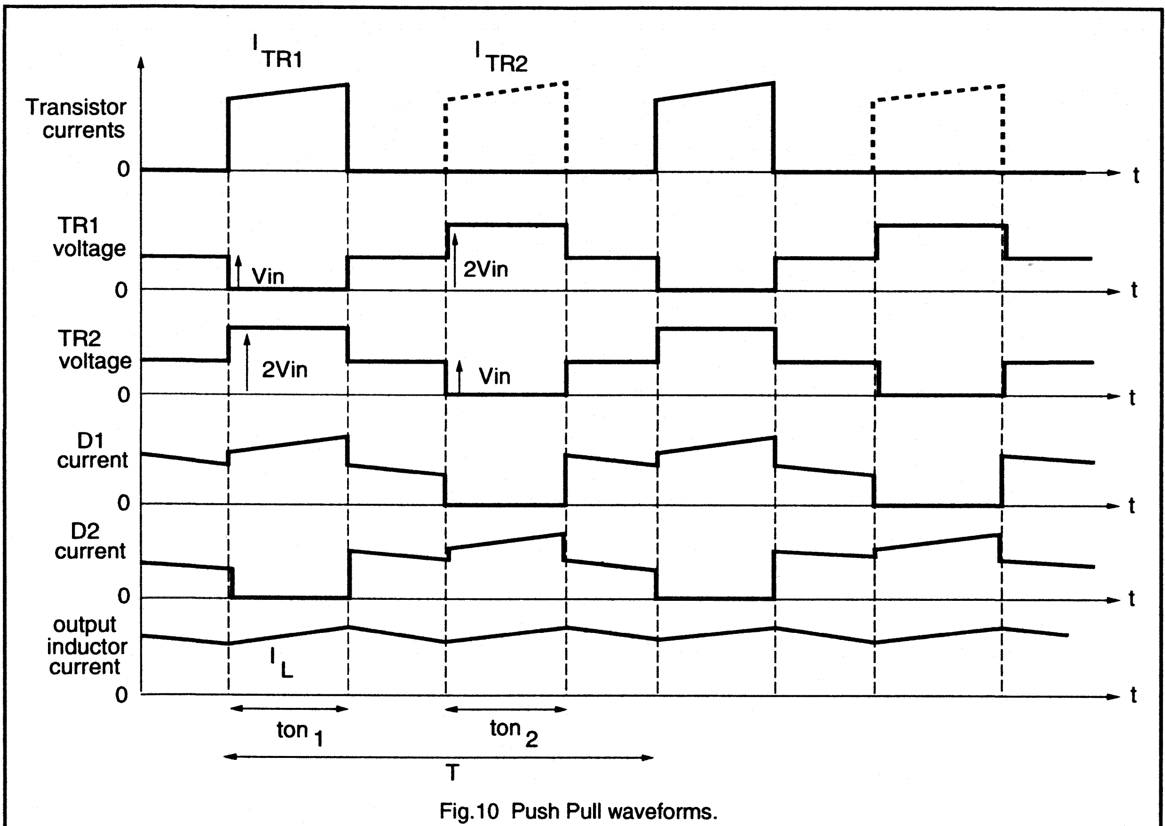


Fig.10 Push Pull waveforms.

Output power	100W		300W		500W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements Max current Max voltage	1.2A 400V	0.6A 800V	4.8A 400V	3.0A 800V	5.8A 400V	3.1A 800V
Bipolar transistors. TO-220 Isolated SOT-186 SOT-93 Isolated SOT-93		BUX85 BUX85F --- ---	BUV28A BUV28AF --- ---	BUT11A BUT11AF --- ---	BUV28A BUV28AF --- ---	--- --- BUT12A BUT12AF
Power MOSFET TO-220 isolated SOT-186 SOT-93 isolated SOT-199	BUK454-400B BUK444-400B --- ---	BUK454-800A BUK444-800A --- ---	BUK455-400B BUK445-400B --- ---	BUK456-800A BUK446-800A --- ---	--- --- BUK437-400B BUK427-400B	--- --- BUK438-800A BUK428-800A
Output Rectifiers (dual) O/P voltage 5V 10V 20V 50V	PBYR2035 BYV32-100 BYV32- 200 BYT28-300		PBYR12035T BYV42-100 BYV32-200 BYT28-300		PBYR12035T BYT230PI-200 BYV42-200 BYT28-300	

Table.4 Recommended Power Semiconductors for off-line Push-pull converter.

Output power	100W		200W		300W	
Line voltage, Vin	96V dc	48V dc	96V dc	48V dc	96V dc	48V dc
Power MOSFET TO-220 isolated SOT-186 SOT-93 isolated SOT-199	BUK454-400A BUK444-400A --- ---	BUK454-200A BUK444-200A --- ---	BUK455-400A BUK445-400A --- ---	BUK456-200B BUK446-200A --- ---	--- --- BUK437-400B BUK427-400B	--- --- --- ---

Table.5 Recommended power MOSFETs for lower input voltage push-pull.

Push-Pull converter.

Converter efficiency, η = 80%; Max duty cycle, $D_{max} = 0.9$

Max transistor voltage, V_{Ce} or $V_{ds} = 2V_{in(max)}$ + leakage spike.

$$\text{Max transistor current}, I_C \; ; \; I_D = \frac{P_{out}}{\eta \; D_{max} \; V_{min}}$$

dc voltage gain:- $$\frac{Vo}{Vin} = 2 \; n \; D$$

Applications:- Compact design, very low output ripple supplies in the 100 to 500W range. More suited to low input applications. e.g battery, 28, 40V inputs, high current outputs. Telecommunication supplies.

(d) The Half-Bridge.

Of all the symmetrical high power converters, the half-bridge converter shown in Fig.11 is the most popular. It is also referred to as the single ended push-pull, and in principle is a balanced version of the forward converter. Again it is a derivative of the buck. The Half-Bridge has some key advantages over the push-pull, which usually makes it first choice for higher power applications in the 500 to 1000W range.

Operation.

The two mains bulk capacitors C1 and C2, are connected in series, and an artificial input voltage mid-point is provided, shown as point A in the diagram. The two transistor switches are driven alternately, and this connects each capacitor across the single primary winding each half cycle, $V_{in}/2$ is superimposed symmetrically across the primary in a push-pull manner. Power is transferred directly to the output on each transistor conduction time and a maximum duty cycle of 90% is available (Some dead time is required to prevent transistor cross-conduction). Since the primary is driven in both directions, (natural reset) a full wave buck output filter (operating at twice the switching frequency) rather than a half wave filter is implemented. This again results in very efficient core utilisation. As can be seen in Fig.12, the waveforms are identical to the push-pull, except that the voltage across the transistors is halved. (The device current would be higher for the same output power.)

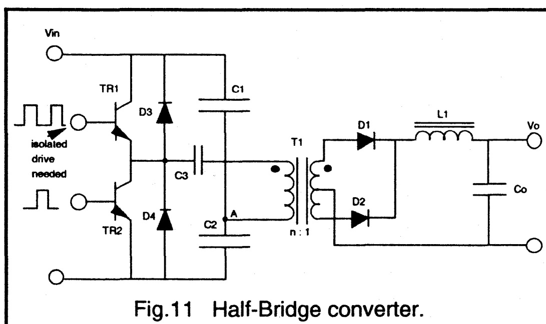


Fig.11 Half-Bridge converter.

Advantages.

Since both transistors are effectively in series, they never see greater than the supply voltage, V_{in}. When both are off, their voltages reach an equilibrium point of $V_{in}/2$. This is half the voltage rating of the push-pull (although double the current). This means that the half-bridge is particularly suited to high voltage inputs, such as off-line applications. For example, a 220V mains application can use two higher speed, higher efficiency 450V transistors instead of the 800V types needed for a push-pull. This allows higher frequency operation.

Another major advantage over the push-pull is that the transformer saturation problems due to flux symmetry imbalance are not a problem. By using a small capacitor (less than 10µF) any dc build up of flux in the transformer is blocked, and only symmetrical ac is drawn from the input.

The configuration of the half-bridge allows clamp diodes to be added across the transistors, shown as D3 and D4 in Fig.11. The leakage inductance and magnetisation energies are dumped straight back into the two input capacitors, protecting the transistors from dangerous transients and improving overall efficiency.

A less obvious exclusive advantage of the half-bridge, is that the two series reservoir capacitors already exists, and this makes it ideal for implementing a voltage doubling circuit. This permits the use of either 110V /220V mains to as selectable inputs to the supply.

The bridge circuits also have the same advantages over the single-ended types as the push-pull, including excellent transformer utilisation, very low output ripple, and high output power capabilities. The limiting factor in the maximum output power available from the half-bridge is the peak current handling capabilities of present day transistors. 1000W is typically the upper power limit. For higher output powers the four switch Full- bridge is normally used.

Disadvantages.

The need for two 50/60 Hz input capacitors is a drawback because of their large size. The top transistor must also have isolated drive, since the gate / base is at a floating potential. Furthermore, if snubbers are used across the power transistor, great care must be taken in their design, since the symmetrical action means that they will interact with one another. The circuit cost and complexity have clearly increased, and this must be weighed up against the advantages gained. In many cases, this normally excludes the use of the half-bridge at lower output power levels below 500W.

Suitable transistors and rectifiers for the half-bridge are given in Table.6

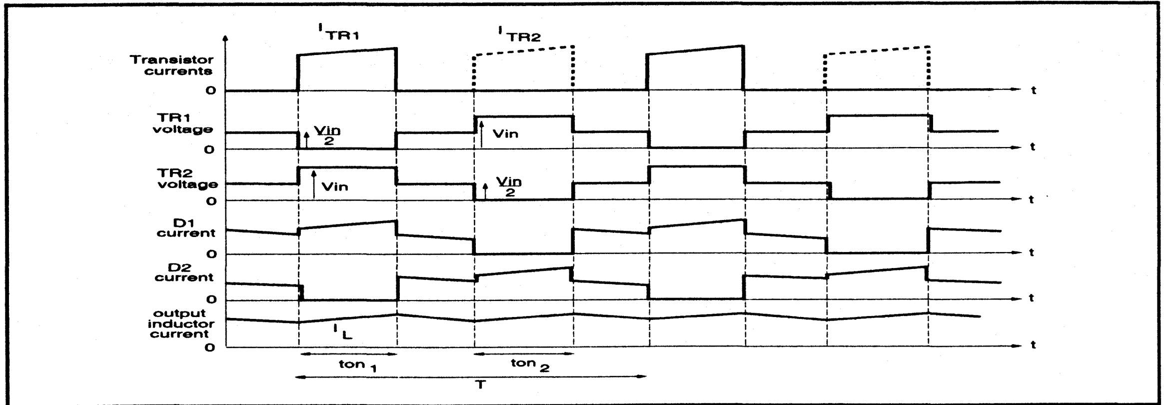


Fig.12 Half-Bridge waveforms.

Output power	300W		500W		750W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements Max current Max voltage	4.9A 250V	2.66A 450V	11.7A 250V	6.25A 450V	17.5A 250V	9.4A 450V
Bipolar transistors. TO-220 Isolated SOT-186	BUV27A BUV27AF	MJE13004 PH13002	BUV27A BUV27AF	MJE13006 BU306F	BUV28A BUV28AF	MJE13008 ---
Power MOSFET SOT-93 isolated SOT-199 SOT-227 (ISOTOP)	--- --- ---	BUK437-500B BUK427-500B ---	--- --- BUK417-500A	BUK438-500A BUK428-500A ---	--- --- ---	BUK438-500A BUK428-500A ---
Output Rectifiers (dual) O/P voltage 5V 10V 20V 50V	PBYR12035T BYV42-100 BYV32-200 BYT28-300		PBYR12035T BYT230PI-200 BYV42-200 BYT28-300		PBYR16035T-45T BYV54 BYT230PI BYV34-300	

Table.6 Recommended Power Semiconductors for off-line Half-Bridge converter.

Half-Bridge converter.

Converter efficiency, η = 80%; Max duty cycle, $D_{max} = 0.9$

Max transistor voltage, V_{Ce} or $V_{ds} = V_{in(max)}$ + leakage spike.

$$\text{Max transistor current}, I_C \;;\; I_D = 2\frac{P_{out}}{\eta \; D_{max} \; V_{min}}$$

dc voltage gain:- $\frac{Vo}{Vin} = n \; D$

Applications:- High power, up to 1000W. High current, very low output ripple outputs. Well suited for high input voltage applications, e.g 110, 220, 440V mains. e.g Large computer supplies, Lab equipment supplies.

(e) The Full-Bridge.

Outline.

The Full-Bridge converter shown in Fig.13 is a higher power version of the Half-Bridge, and provides the highest output power level of any of the converters discussed. The maximum current ratings of the power transistor will eventually determine the upper limit of the output power of the half-bridge. These levels can be doubled by using the Full-Bridge, which is obtained by adding another two transistors and clamp diodes to the Half-Bridge arrangement. The transistors are driven alternately in pairs, T1 and T3, then T2 and T4. The transformer primary is now subjected to the full input voltage. The current levels flowing are halved compared to the half-bridge for a given power level. Hence, the Full-Bridge will double the output power of the Half-Bridge using the same transistor types.

The secondary circuit operates in exactly the same manner as the push-pull and half-bridge, also producing very low ripple outputs at very high current levels. Therefore, the waveforms for the Full-Bridge are identical to the Half-Bridge waveforms shown in Fig.12, except for the voltage across the primary, which is effectively doubled (and switch currents halved). This is expressed in the dc gain and peak current equations, where the factor of two comes in, compared with the Half-Bridge.

Advantages.

As stated, the Full-Bridge is ideal for the generation of very high output power levels. The increased circuit, complexity normally means that the Full-Bridge is reserved for applications with power output levels of 1kW and above. For such high power requirements, designers often select power Darlingtons, since their superior current ratings and switching characteristics provide additional performance and in many cases a more cost effective design.

The Full-Bridge also has the advantage of only requiring one mains smoothing capacitor compared to two for the Half-Bridge, hence, saving space. It's other major advantages are the same as for the Half-Bridge.

Disadvantages.

Four transistors and clamp diodes are needed, instead of two for the other symmetrical types. Isolated drive for two floating potential transistors is now required. The Full-Bridge has the most complex and costly design of any of the converters discussed, and should only be used where other types do not meet the requirements. Again, the four transistor snubbers (if required) must be implemented carefully to prevent interactions occurring between them.

Table.7 gives an outline of the Philips power semiconductors suitable for use with the Full-Bridge. For these very high power applications, devices are available in the SOT-227 (ISOTOP) package. Both Bipolar and MOSFET types are available in this outline, which has extremely high current handling capabilities, fast switching characteristics (provided by very low internal inductance) and a very low thermal resistance.

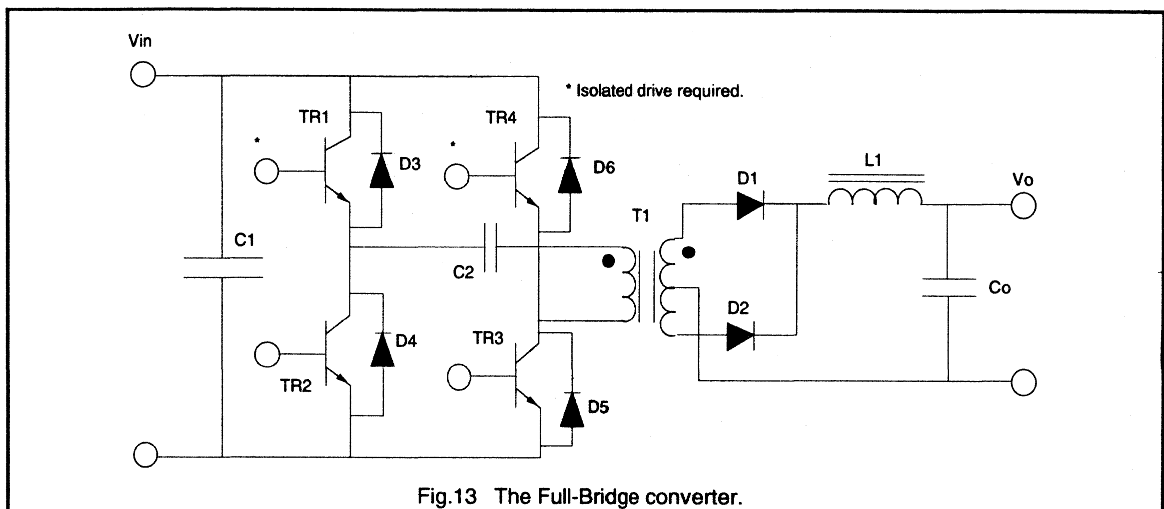


Fig.13 The Full-Bridge converter.

Output power	500W		1000W		2000W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements Max current Max voltage	 5.7A 250V	 3.1A 450V	 11.5A 250V	 6.25A 450V	 23.0A 250V	 12.5A 450V
Bipolar transistors. TO-220 Isolated SOT-186 SOT-93 Isolated SOT-93 SOT-227 (ISOTOP)	 BUV27A BUV27AF --- --- ---	 BUV28A BUV28AF --- --- ---	 BUV27A BUV27AF --- --- ---	 BUV28A BUV28AF --- --- ---	 --- --- --- --- ESM3045D	 BUV28 BUV28AF --- ---
Power MOSFET TO-220 isolated SOT-186 SOT-93 isolated SOT-199 SOT-227 (ISOTOP)	 --- --- --- --- ---	 BUK457-500A BUK447-500A BUK437-500A BUK427-500A ---	 --- --- --- --- BUK417-500A	 --- --- BUK438-500A BUK-428-500A ---	 --- --- --- --- ---	 --- --- --- --- BUK417-500A
Output Rectifiers (dual) O/P voltage 5V 10V 20V 50V	 PBYR12035T BYT230PI BYV42-200 BYT28-300		 PBYR30035CT BYV54 BYT230PI-200 BYV34-300		 PBYR40035CT --- BYV54-200 BYT230PI-300	

Table.7 Recommended Power Semiconductors for the Full-Bridge converter.

Full-Bridge converter.

Converter efficiency, $\eta = 80\%$; Max duty cycle, $D_{max} = 0.9$

Max transistor voltage, V_{ce} or $V_{ds} = V_{in(max)}$ + leakage spike.

$$\text{Max transistor current}, I_C \;;\; I_D = \frac{P_{out}}{\eta \quad D_{max} \quad V_{min}}$$

dc voltage gain:- $\frac{Vo}{Vin} = 2 \quad n \quad D$

Applications:- Very high power, normally above 1000W. Very high current, very low output ripple outputs. Well suited for high input voltage applications, e.g 110, 220, 440V mains. e.g Computer Mainframe supplies, Large lab equipment supplies, Telecomm systems.

Conclusion.

The 5 most common S.M.P.S. converter topologies, the flyback, forward, push-pull, half-bridge and full-bridge types have been outlined. Each has its own particular operating characteristics and advantages, which makes it suited to particular applications.

The converter topology also defines the voltage and current ratings of the power transistors required (Either MOSFET or Bipolar). Simple equations and calculations used to outline the requirements of the transistors for each topology have been presented.

The selection guide for transistors and rectifiers at the end of each topology section, reveals the wide range of devices and package outlines available from Philips, which are ideal for use in S.M.P.S. applications.

References.

(1) See S.M.P.S. section 2.3.3

(2) Philips MOSFET Selection Guide For S.M.P.S. by M.J.Humphreys. Philips power semiconductor Applications group, Hazel Grove.

(3) Switch Mode Power Conversion - Basic theory and design by K.Kit.Sum. (Published by Marcel Dekker inc.1984)

Appendix A.

MOSFET throughput power calculations.

Assumptions made:-

The power loss (Watts) in the transistor due to on state losses is 5% of the total throughput (output) power.

Switching losses in the transistor are negligible. N.B At frequencies significantly higher than 50kHz the switching losses may become important.

The device junction temperature, T_j is taken to be 125˚C. The ratio $R_{ds(125C^\circ)}/R_{ds(25^\circ C)}$ is dependent on the voltage rating of the MOSFET device. Table A1 gives the ratio for the relevant voltage ratings.

The value of $V_{s(min)}$ for each input value is given in Table A2.

Device voltage rating.	$R_{ds(125C)}$ / $R_{ds(25C)}$
100	1.74
200	1.91
400	1.98
500	2.01
800	2.11
1000	2.15

Table. A1 On resistance ratio.

Main input voltage	Maximum dc link voltage	Minimum dc link voltage
220 / 240V ac	385V	200V
110 / 120V ac	190V	110V

Table. A2 Max and Min dc link voltages for mains inputs.

Using the following equations, for a given device with a known $R_{ds(125^\circ C)}$, the maximum throughput power in each topology can be calculated.

Where:-

$P_{th(max)}$ = Maximum throughput power.
D_{max} = maximum duty cycle.
τ = required transistor efficiency (0.05 ± 0.005)
$Rds_{(125^\circ C)} = R_{ds(25^\circ C)}$ x ratio.
$V_{s(min)}$ = minimum dc link voltage.

Forward converter.

$$P_{th(max)} = \frac{\tau \times V_{s(min)}^2 \times D_{max}}{R_{ds(125c)}}$$

$D_{max} = 0.45$

Flyback Converter.

$$P_{th(max)} = \frac{3 \times \tau \times V_{s(min)}^2 \times D_{max}}{4 \times R_{ds(125c)}}$$

$D_{max} = 0.45$

Push Pull Converter.

$$P_{th(max)} = \frac{\tau \times V_{s(min)}^2 \times D_{max}}{R_{ds(125c)}}$$

$D_{max} = 0.9$

Half Bridge Converter.

$$P_{th(max)} = \frac{\tau \times V_{s(min)}^2 \times D_{max}}{4 \times R_{ds(125c)}}$$

$D_{max} = 0.9$

Full Bridge Converter.

$$P_{th(max)} = \frac{\tau \times V_{s(min)}^2 \times D_{max}}{2 \times R_{ds(125c)}}$$

$D_{max} = 0.9$

2.1.2 The power supply designers guide to high voltage transistors

One of the most critical components in power switching converters is the high voltage transistor. Despite its wide usage, feedback from power supply designers suggests that there are several features of high voltage transistors which are generally not well understood.

This section begins with a straightforward explanation of the key properties of high voltage transistors. This is done by showing how the basic technology of the transistor leads to its voltage, current, power and second breakdown limits. It is also made clear how deviations from conditions specified in the data book will affect the performance of the transistor. The final section of the paper gives practical advice for designers, as to how circuits might be optimised and transistor failures avoided.

Introduction

A large amount of useful information about the characteristics of a given component is provided in the relevant data book. By using this information, a designer can usually be sure of choosing the optimum component for a particular application.

However, if a problem arises with the completed circuit, and a more detailed analysis of the most critical components becomes necessary, the data book can become a source of frustration rather than practical assistance. In the data book, a component is often measured under a very specific set of conditions. Very little is said about how the component performance is affected if these conditions are not reproduced exactly when the component is used in a circuit.

There are as many different sets of requirements for high voltage transistors as there are circuits which make use of them. Covering every possible drive and load condition in the device specification is an impossible task. There is therefore a real need for any designer using high voltage transistors to have an understanding of how deviations from the conditions specified in the transistor data book will affect the electrical performance of the device, in particular its maximum ratings.

Feedback from designers implies that this information is not readily available. The intention of this report is therefore to provide designers with the information they need in order to optimise the reliability of their circuits. The characteristics of high voltage transistors stem from their basic technology and so it is important to begin with an overview of this.

HVT technology

Stripping away the encapsulation of the transistor reveals how the electrical connections are made (see Fig.1). The collector is contacted through the back surface of the transistor chip, which is soldered to the nickel-plated copper lead frame. For Philips power transistors the lead frame and the centre leg are formed from a single piece of copper, and so the collector can be accessed through either the centre leg or any exposed part of the lead frame (eg the mounting base for TO220 and SOT93).

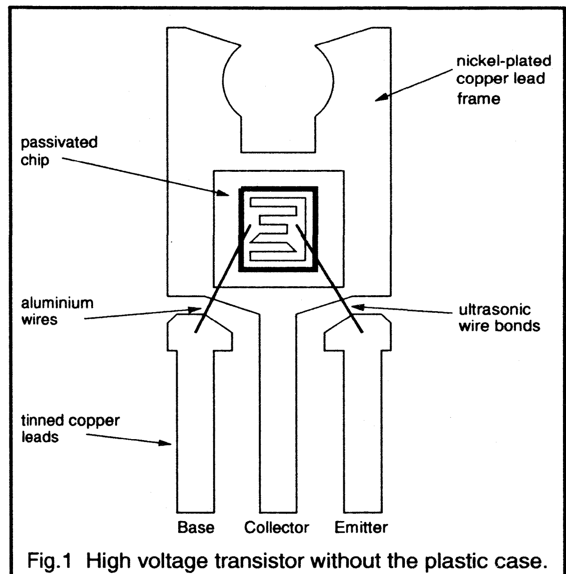


Fig.1 High voltage transistor without the plastic case.

The emitter area of the transistor is contacted from the top surface of the chip. A thin layer of aluminium joins all of the emitter area to a large bond pad. This bond pad is aluminium wire bonded to the emitter leg of the transistor when the transistor is assembled. The same method is used to contact the base area of the chip. Fig.2 shows the top view of a high voltage transistor chip in more detail.

Viewing the top surface of the transistor chip, the base and emitter fingers are clearly visible. Around the periphery of the chip is the high voltage glass passivation. The purpose of this is explained later.

Taking a cross section through the transistor chip reveals its npn structure. A cross section which cuts one of the emitter fingers and two of the base fingers is shown in Fig.3.

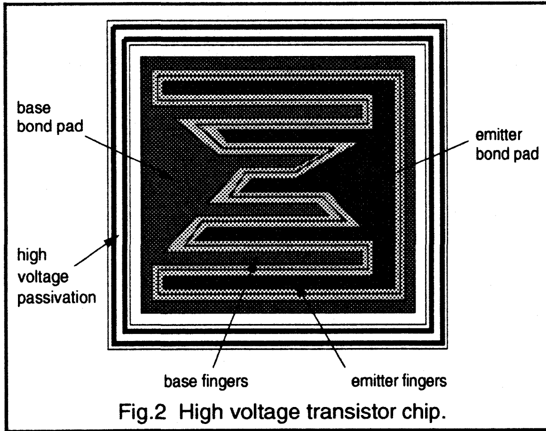


Fig.2 High voltage transistor chip.

On the top surface of the transistor are the aluminium tracks which contact the base and emitter areas. The emitter finger is shown connected to an n+ region. This is the emitter area. The n+ denotes that this is very highly doped n type silicon. Surrounding the n+ emitter is the base, and as shown in Fig.3 this is contacted by the base fingers, one on either side of the emitter. The p denotes that this is highly doped p type silicon.

On the other side of the base is the thick collector n- region. The n- denotes that this is lightly doped n type silicon. The collector region supports the transistor blocking voltage, and its thickness and resistivity must increase with the voltage rating of the device.

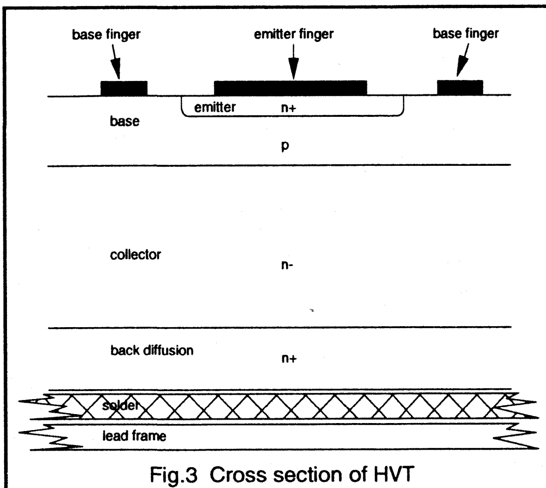


Fig.3 Cross section of HVT

Following the collector region is the n+ back diffusion. The n+ back diffusion ensures a good electrical contact is made between the collector region and the lead frame/collector leg, whilst also allowing the crystal to be thick enough to prevent it from cracking during processing and assembly. The bottom surface of the chip is soldered to the lead frame.

Voltage ratings

Part 1: Base shorted to emitter.

When the transistor is in its off state with a high voltage applied to the collector, the base collector junction is reverse biased by a very high voltage. The voltage supporting *depletion region* extends deep into the collector, right up to the back diffusion, as shown in Fig.4.

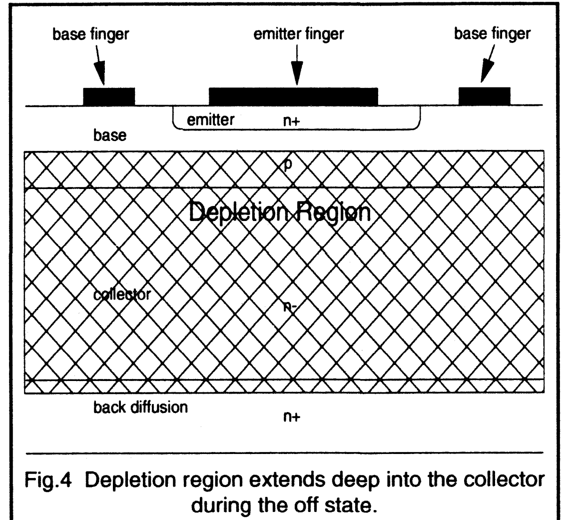


Fig.4 Depletion region extends deep into the collector during the off state.

With the base of the transistor short circuited to the emitter, or at a lower potential than the emitter, the voltage rating is governed by the voltage supporting capability of the reverse biased base collector junction. This is the transistor $V_{CESMmax}$. The breakdown voltage of the reverse biased base collector junction is determined mainly by the collector width and resistivity as follows:

Fig.5 shows the doping profile of the transistor. Note the very high doping of the emitter and the back diffusion, the high doping of the base and the low doping of the collector. Also shown in Fig.5 is the electric field concentration throughout the depletion region for the case where the transistor is supporting its off state voltage. The electric field, E, is given by the equation, E = -dV/dx, where -dV is the voltage drop in a distance dx. Rewriting this equation gives the voltage supported by the depletion region;

$$V = -\int E dx$$

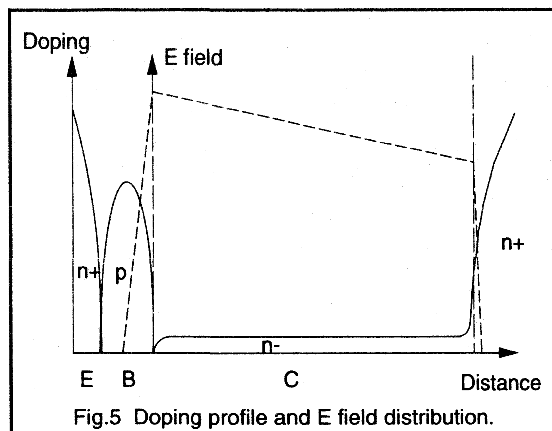


Fig.5 Doping profile and E field distribution.

This is the area under the dotted line in Fig.5.

During the off state, the peak electric field occurs at the base collector junction as shown in Fig.5. If the electric field anywhere in the transistor exceeds 200 kVolts per cm then avalanche breakdown occurs and the current which flows in the transistor is limited only by the surrounding circuitry. If the avalanche current is not limited to a very low value then the power rating of the transistor can easily be exceeded and the transistor destroyed as a result of thermal breakdown. Thus the maximum allowable value of electric field is 200 kV/cm.

The gradient of the electric field, dE/dx, is proportional to charge density which is in turn proportional to the level of doping. In the base, the gradient of the electric field is high because of the high level of doping, and positive because the base is p type silicon. In the collector, the gradient of the electric field is low because of the low level of doping, and negative because the collector is n type silicon. In the back diffused region, the gradient of the electric field is very highly negative because this is very highly doped n type silicon.

Increasing the voltage capability of the transistor can therefore be done by either increasing the resistivity (lowering the level of doping) of the collector region, in order to maintain a high electric field for the entire collector width, or increasing the collector width itself. Both of these measures can be seen to work in principle because they increase the area under the dotted line in Fig.5.

The maximum breakdown voltage of the transistor, $V_{CESMmax}$, is limited by the need to keep the peak electric field, E, below 200 kV/cm. Without special measures, the electric field would crowd at the edges of the transistor chip because of the surface irregularities. This would limit breakdown voltages to considerably less than the full capability of the silicon. Crowding of the equipotential lines at the chip edges is avoided by the use of a glass passivation (see Fig.6). The glass passivation therefore allows the full voltage capability of the transistor to be realised.

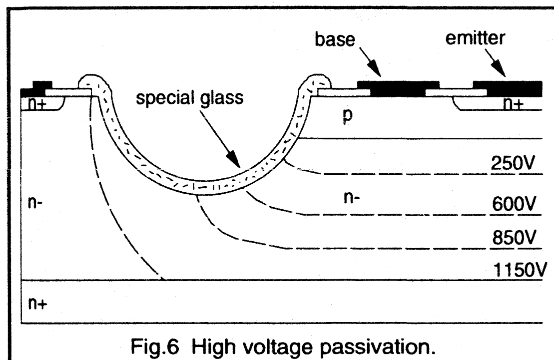


Fig.6 High voltage passivation.

The glass used is negatively charged so as to induce a p-channel underneath it. This ensures that the applied voltage is supported evenly over the width of the glass and does not crowd at any one point. High voltage breakdown therefore occurs in the bulk of the transistor, at the base collector junction, and not at the edges of the crystal.

Exceeding the voltage rating of the transistor, even for a fraction of a second, must be avoided. High voltage breakdown effects can be concentrated in a very small area of the transistor, and only a small amount of energy may damage the device. However, there is no danger in using the full voltage capability of the transistor as the limit under worst case conditions because the high voltage passivation is extremely stable.

Part 2: Open circuit base.

With the base of the transistor open circuit the voltage capability is much lower. This is the V_{CEOmax} of the device and it is typically just less than half of the $V_{CESMmax}$ rating. The reason for the lower voltage capability under open circuit base conditions is as follows:

As the collector emitter voltage of the transistor rises, the peak electric field located at the base collector junction rises too. Above a peak E field value of 100 kV/cm there is an appreciable leakage current being generated.

In the previous case, with the base contact short circuited to the emitter, or held at a lower potential than the emitter, any holes which are generated drift from the edge of the depletion region towards the base contact where they are extracted. However, with the base contact open circuit, the holes generated diffuse from the edge of the depletion region towards the emitter where they effectively act as base current. This causes the emitter to inject electrons into the base, which diffuse towards the collector. Thus there is a flow of electrons from the emitter to the collector.

The high electric field in the collector accelerates the electrons to the level where some have sufficient energy to produce more hole electron pairs through their collisions with the lattice. The current generated in this way adds to the leakage current. Thus with the base contact open circuit the emitter becomes active and provides the system with *gain*, multiplying the leakage current and consequently reducing the breakdown voltage.

For a given transistor the gain of the system is dependant on two things. Firstly it is dependant on the probability that a hole leaving the depletion region will reach the emitter. If the base is open circuit and no recombination occurs then this probability is 1. If the base is not open circuit, and instead a potential below V_{BEon} is applied, then there is a chance that a hole leaving the depletion region will be extracted at the base contact. As the voltage on the base contact is made less positive the probability of holes reaching the emitter is reduced.

Secondly, the gain is dependant on the probability of electrons leaving the emitter, diffusing across the base and being accelerated by the high field in the collector to the level where they are able to produce a hole electron pair in one of their collisions with the lattice. This depends on the electric field strength which is in turn dependant on the collector voltage.

Thus for a given voltage at the base there is a corresponding maximum collector voltage before breakdown will occur. With the base contact shorted to the emitter, or at a lower potential than the emitter, the full breakdown voltage of the transistor is achieved ($V_{CESMmax}$). With the base contact open circuit, or at a *higher* potential than the emitter, the breakdown voltage is lower (V_{CEOmax}) because in this case the emitter is active and it provides the breakdown mechanism with gain.

With the base connected to the emitter by a non zero impedance, the breakdown voltage will be somewhere between the $V_{CESMmax}$ and the V_{CEOmax}. A low impedance approximates to the shorted base, 'zero gain', case and a high impedance approximates to the open base, 'high gain', case. With a base emitter impedance of 47 Ω and no externally applied base voltage, the breakdown voltage is typically 10% higher than the V_{CEOmax}.

Current rating

The maximum allowed DC current is limited by the size of the bond wires to the base and emitter. Exceeding the DC ratings I_{Cmax} and I_{Bmax}, for any significant length of time, may blow these bond wires. If the current pulses are short and of a low duty cycle then values greatly in excess of the DC ratings are allowed. The I_{CMmax} and I_{BMmax} ratings are recommendations for peak current values. For a duty cycle of 0.01 and a pulse width of 10ms these values will typically be double the DC ratings.

If the pulses are shorter than 10ms then even the recommended peak values can be exceeded under worst case conditions. However, it should be noted that combinations of high collector current and high collector voltage can lead to failure by second breakdown (discussed later). As the collector current is increased, the collector voltage required to trigger second breakdown drops, and so allowing large collector current spikes increases the risk of failure by second breakdown. It is therefore advised that the peak values given in the data book are used as design limits in order to maximise the component reliability.

In emitter drive circuits, the peak reverse base current is equal to the peak collector current. The pulse widths and duty cycles involved are small, and this mode of operation is within the capability of all Philips high voltage transistors.

Power rating

The P_{totmax} given in device data is not generally an achievable parameter because in practice it is obtainable only if the mounting base temperature can be held to 25 °C. In practice, the maximum power dissipation capability of a given device is limited by the heatsink size and the ambient temperature. The maximum power dissipation capability for a particular circuit can be calculated as follows;

T_{jmax} is the maximum junction temperature given in the data sheet. The value normally quoted is 150 °C. T_{amb} is the ambient temperature around the device heatsink. A typical value in practice could be 65 °C. R_{thj-mb} is the device thermal resistance given in the data sheet, but to obtain a value of junction to *ambient* thermal resistance, R_{thj-a}, the thermal resistance of the mica spacer (if used), heatsink and heatsink compound should be added to this.

The maximum power which can be dissipated under a given set of circuit conditions is calculated using;

$$P_{max} = (T_{jmax} - T_{amb})/R_{thj-a}$$

For a BUT11AF, in an ambient temperature of 65 °C, mounted on a 10 K/W heatsink with heatsink compound, this gives;

$$R_{thj-a} = 3.95\ K/W + 10\ K/W = 13.95\ K/W$$

and hence the maximum power capable of being dissipated under these conditions is;

$$P_{max} = (150-65)/13.95 = 6\ W$$

Exceeding the maximum junction temperature, T_{jmax}, is not recommended. All of the quality and reliability work carried out on the device is based on the maximum junction temperature quoted in data. If T_{jmax} is exceeded in the circuit then the reliability of the device is no longer guaranteed.

Second breakdown

Pure silicon, also known as *'intrinsic'* silicon, contains few mobile charge carriers at room temperature and so its conductivity is low. By doping the silicon (ie introducing atoms of elements other than silicon) the number of mobile charge carriers, and hence the conductivity, can be increased. Silicon doped in such a way as to increase the number of mobile electrons (negative charge) is called n type silicon. Silicon doped in such a way as to increase the number of mobile holes (positive charge) is called p type silicon. Thus the base region of an npn transistor contains an excess of mobile holes and the collector and emitter regions contain an excess of mobile electrons.

When a high voltage is applied to the transistor, and the collector base junction is reverse biased, a depletion region is developed. This was shown in Fig.4. The depletion region supports the applied voltage. The electric field distribution within the depletion region was shown in Fig.5.

The term *depletion region* refers to a region depleted of mobile charge carriers. Therefore within the depletion region, the base will have lost some holes and hence it is left with a net negative charge. Similarly the collector will have lost some electrons and hence it is left with a net positive charge. The collector is said to have a 'positive space charge' (and the base a 'negative space charge'.)

Consider the case where a transistor is in its off state supporting a high voltage which is within its voltage capability. The resulting electric field distribution is shown in Fig.7.

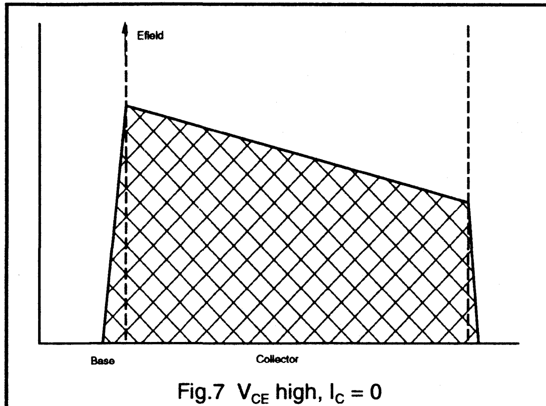


Fig.7 V_{CE} high, I_C = 0

If the collector voltage is held constant, and the collector current increased so that there is now some collector current flowing, this current will modify the charge distribution within the depletion region. The effect this has on the base is negligible because the base is very highly doped. The effect this has on the collector is significant because the collector is only lightly doped.

The collector current is due to the flow of electrons from the emitter to the collector. As the collector current increases the collector current density increases. This increase in collector current density is reflected in Fig.8 by an increase in the electron concentration in the collector.

At a certain collector current density, the negative charge of the electrons neutralises the positive space charge of the collector. The gradient of the electric field, dE/dx, is proportional to charge density. If the space charge is neutralised then the gradient of the electric field becomes zero. This is the situation illustrated in Fig.8. Note that the shaded area remains constant because the applied voltage remains constant. Therefore the peak value of electric field drops slightly.

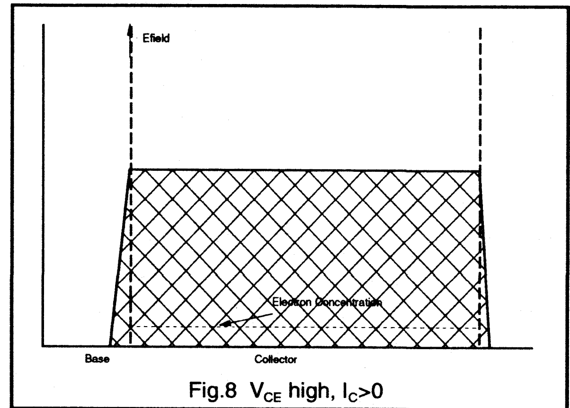


Fig.8 V_{CE} high, I_C>0

Keeping the collector emitter voltage constant, and pushing up the collector current density another step, increases the concentration of electrons in the collector still further. Thus the collector charge density is now negative, the gradient of electric field in the collector is now positive, and the peak electric field has shifted from the collector-base junction to the collector-back diffusion interface. This is shown in Fig.9.

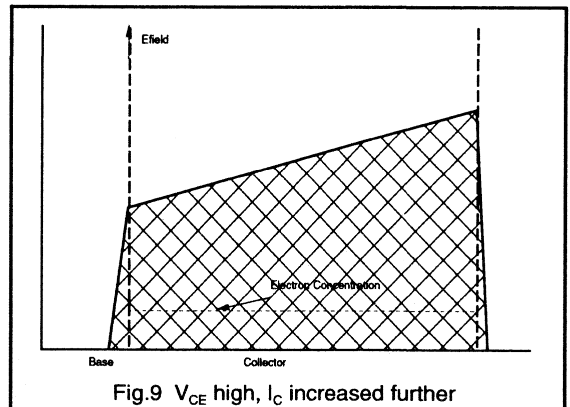


Fig.9 V_{CE} high, I_C increased further

Increasing the collector current density another step will further increase the positive gradient of electric field. The collector voltage is unchanged and so the shaded area must remain unchanged. Therefore the peak electric field is forced upwards. This is shown in Fig.10.

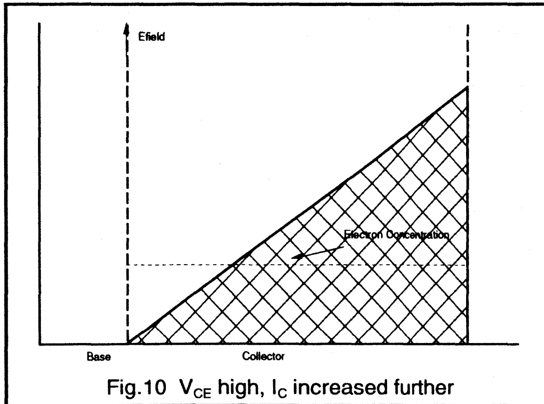


Fig.10 V_{CE} high, I_C increased further

At a certain critical value of peak electric field, E_{crit}, a regenerative breakdown mechanism takes place which causes the electron concentration in the collector to increase uncontrollably by a process known as *avalanche multiplication*. As the electron concentration increases, the gradient of electric field increases (because the gradient of electric field is proportional to charge density). The peak electric field is clamped by the breakdown and so the collector voltage drops. In most circuits the collapsing collector voltage will result in a further rise in collector current density, causing a further rise in electron concentration (ie positive feedback). This is shown in Fig.11.

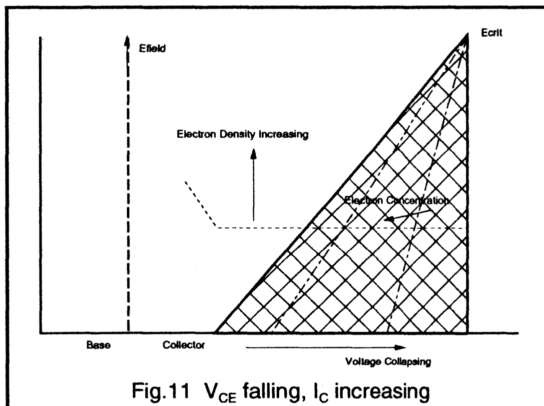


Fig.11 V_{CE} falling, I_C increasing

At approximately 30 V, the holes produced by the avalanche multiplication build up sufficiently to temporarily stabilize the system. However, with 30 V across the device and a high collector current flowing through it, a considerable amount of heat will be generated. Within less than one microsecond thermal breakdown will take place, followed by device destruction.

Safe Operating Area

It has been shown that the electric field profile, and hence the peak electric field, is dependant on the combination of collector current density and applied collector voltage. The peak electric field increases with increasing collector voltage (increase in shaded area in Figs 7 to 11). It also increases with increasing collector current density (increase in gradient of electric field). At all times the peak electric field must remain below the critical value. If the collector voltage is lowered then a higher collector current density is permitted. If the collector current density is lowered then a higher collector voltage is permitted.

Potentially destructive combinations of collector current density and collector voltage are most likely to occur during switching and during fault conditions in the circuit (eg a short circuited load). The safe operating areas give information about the capability of a given device under these conditions.

The collector current density is dependant on the collector current and the degree of current crowding in certain areas of the collector. The degree of current crowding is different for turn on (positive base voltage) and turn off (negative base voltage). Therefore the allowed combinations of collector current and collector voltage, collectively known as the safe operating area (SOAR) of the transistor, will be different for turn on of the transistor and turn off.

Forward SOAR

With a positive voltage applied to the base, the shape of the safe operating area for DC operation is that shown in Fig.12. Operation outside of the safe operating area is not allowed.

For pulsed operation the forward SOAR increases, and for small, low duty cycle pulses it becomes square. The forward SOAR provides useful information about the capabilities of the transistor under fault conditions in the circuit (eg. a short circuited load).

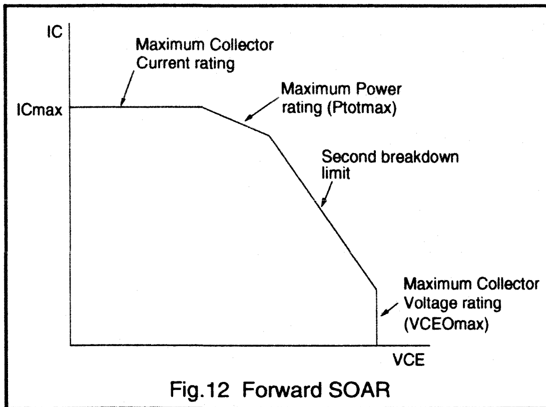


Fig.12 Forward SOAR

The safe operating area is designed to protect the current, power, voltage and second breakdown limits of the transistor. The current, power and voltage limits of the transistor have already been discussed. Note that the peak voltage rating is the V_{CEOmax} rating and not the $V_{CESMmax}$ rating. The $V_{CESMmax}$ rating only applies if the base emitter voltage is not greater than zero volts.

Sometimes shown on forward SOAR curves is an extension allowing higher voltages than V_{CEOmax} to be tolerated for short periods (of the order of 0.5 µs). This allows turn on of the transistor from a higher voltage than V_{CEOmax}. However, the pulses allowed are very short, and unless it can be guaranteed that the rated maximum pulse time will never be exceeded, transistor failures will occur. If the circuit conditions can be guaranteed then there is no danger in making use of this capability.

As mentioned in the previous section, second breakdown is triggered by combinations of high collector voltage and high collector current density. With a positive voltage applied to the base, the region of highest current density is at the edges of the emitter as shown in Fig.13.

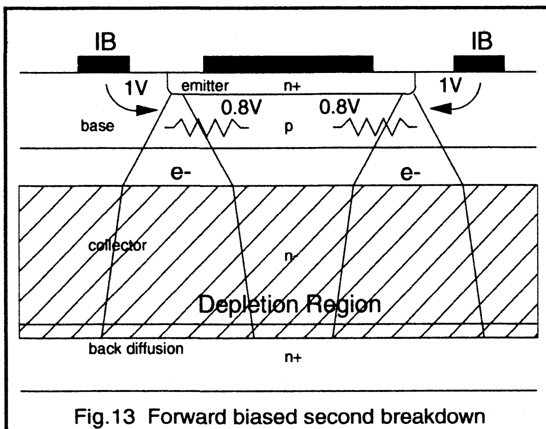


Fig.13 Forward biased second breakdown

The base region under the emitter constitutes a resistance (known as the *sub emitter resistance*). With a positive voltage applied to the base, the sub emitter resistance will mean that the areas of the emitter which are nearest to the base have a higher forward bias voltage than the areas furthest from the base. Therefore the *edges* of the emitter have a higher forward bias voltage than the centre and so they receive a higher base current.

As a result of this the edges of the emitter conduct a substantial proportion of the collector current when the base is forward biased. If the collector current is high then the current density at the edges of the emitter is also high. There will be some spreading out of this current as it traverses the base. When the edge of the depletion region is reached, the current is sucked across by the electric field.

If the transistor is conducting a high current and also supporting a high voltage, then the current density will be high when the current reaches the edge of the depletion region. If the current density is beyond that allowed at the applied voltage, then the second breakdown mechanism is triggered (as explained in the previous section) and the device will be destroyed.

With a positive base current flowing, the region of highest current density is at the edges of the emitter. A forward SOAR failure will therefore produce burns which originate from the edge of one of the emitter fingers.

Forward SOAR failure becomes more likely as pulse width and/or duty cycle is increased. Because the edges of the emitter are conducting more current than the centre, they will get hotter. The temperature of the emitter edges at the end of each current pulse is a function of the pulse width and the emitter current. Longer pulse widths will increase the temperature of the emitter edges at the end of each current pulse. Higher duty cycles will leave insufficient time for this heat to spread. In this manner, combinations of long pulse width and high duty cycle can give rise to cumulative heating effects. Current will crowd towards the hottest part of the emitter. There is therefore a tendency for current to become concentrated in very narrow regions at the edges of the emitter fingers, and as pulse width and/or duty cycle is increased the degree of current crowding increases. This is the reason why the forward SOAR for DC operation is as shown in Fig.12, but for pulsed operation it is enlarged and for small, low duty cycle pulses it becomes square.

Reverse SOAR

During turn on of the transistor, the high resistance of the collector region is reduced by the introduction of holes (from the base) and electrons (from the emitter). This process, known as *conductivity modulation*, is the reason why bipolar transistors are able to achieve such a low collector voltage during the on state, typically 0.2 V. However, during turn off of the transistor, these extra holes and electrons

constitute a stored charge which must be removed from the collector before the voltage supporting depletion region can develop.

To turn off the transistor, a negative voltage is applied to the base and a reverse base current flows. During turn off of the transistor, it is essential that the device stays within its reverse bias safe operating area (RBSOAR). The shape of a typical RBSOAR curve is as shown in Fig.14.

With no negative voltage applied to the base, the RBSOAR is very much reduced, as shown in Fig.14. This is particularly important to note at power up and power down of power supplies, when rail voltages are not well defined (see section on improving reliability).

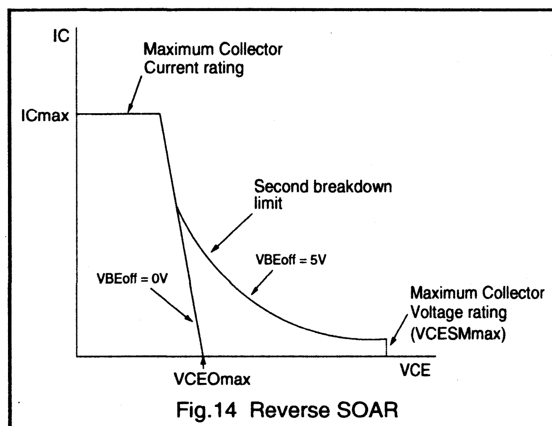


Fig.14 Reverse SOAR

On applying a negative voltage to the base, the charge stored in the collector areas nearest to the base contacts will be extracted, followed by the charge stored in the remaining collector area. Holes not extracted through the base contact are free to diffuse into the emitter where they constitute a base current which keeps the emitter active. During the transistor storage time, the collector charge is being extracted through the base, but the emitter is still active and so the collector current continues to flow.

During the transistor fall time, the voltage supporting depletion region is being developed and therefore the collector voltage is rising. In addition to this, the negative voltage on the base is causing holes to drift towards the base contact where they are neutralised, thus preventing holes from diffusing towards the emitter.

This has two effects on the collector current. Firstly, the rising collector voltage results in a reduction in the voltage across the collector load, and so the collector current starts to drop. Secondly, the extraction of holes through the base will be most efficient nearest to the base contacts (due to the sub emitter resistance), and so the collector current becomes concentrated into narrow regions under the centre of the emitter fingers (furthest from the base). This is shown in Fig.15. This current crowding effect leads to an increase in the collector current density during turn off, even though the collector current itself is falling.

Thus for a portion of the fall time, the collector voltage is rising and the collector current density is also rising. This is a critical period in the turn off phase. If the turn off is not carefully controlled the transistor may be destroyed during this period, due to the onset of the second breakdown mechanism described earlier.

During this critical period, the collector current is concentrated into a narrow region under the centre of the emitter. RBSOAR failure will therefore produce burns which originate from the centre of one of the emitter fingers.

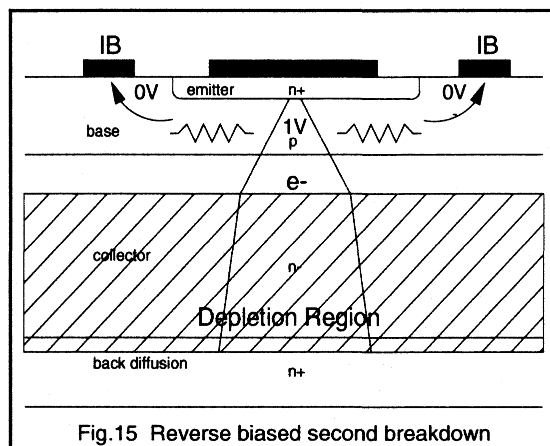


Fig.15 Reverse biased second breakdown

Useful tips as an aid to circuit design

In recent years, the Philips Components Power Semiconductor Applications Laboratory (P.S.A.L.) has worked closely with a number of HVT users. It has become apparent that there are a number of important circuit design features which if overlooked invariably give rise to circuit reliability problems. This section addresses each of these areas and offers guidelines which, if followed, will enhance the overall performance and reliability of any power supply.

Improving turn on

There is more to turning on a high voltage transistor than simply applying a positive base drive. The positive base drive must be at least sufficient to keep the transistor saturated at the current it is required to conduct. However, transistor gain as specified in data sheets tends to be assessed under static conditions and therefore assumes the device is already on.

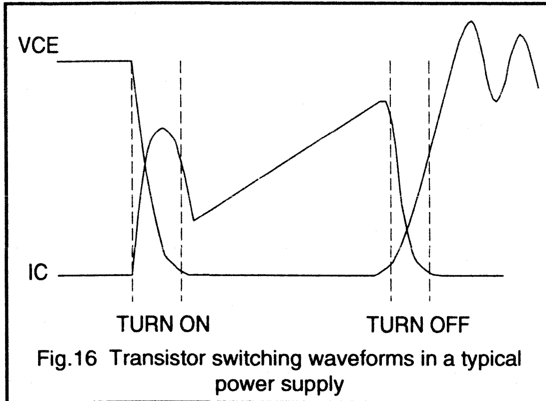


Fig.16 Transistor switching waveforms in a typical power supply

Note 1. *The base current requirements at turn on of the transistor are higher than the static gain would suggest.*

The conductivity modulation process, described at the beginning of the previous section, occurs every time the transistor is turned on. The faster the charges are introduced into the collector, the faster the collector resistance will drop, allowing the collector voltage to drop to its saturation level. The rate at which the collector charge is built up is dependent on the applied base current and the applied collector current. In order to turn the transistor on quickly, and hence minimise the turn on dissipation, the transistor needs to be overdriven until the collector voltage has dropped to its saturation level. This is achieved by having a period of overshoot at the start of the base current pulse. The turn on waveforms are shown in Fig.17.

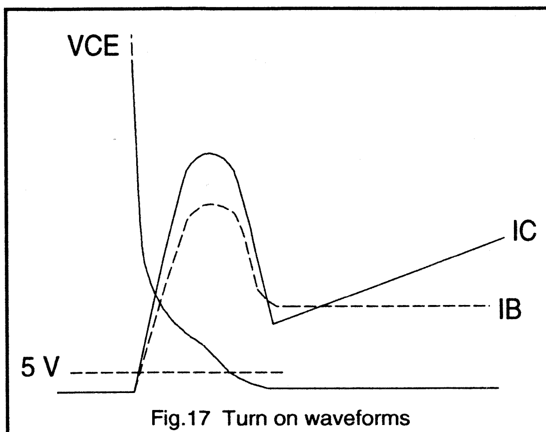


Fig.17 Turn on waveforms

Note 2. *A fast rising base current pulse with an initial period of overshoot is a desirable design feature in order to keep the turn on dissipation low.*

The base current overshoot is achieved by having a capacitor in parallel with the forward base drive resistor (see Fig.18). The RC time constant determines the overshoot period and as a first approximation it should be comparable to the transistor storage time. The capacitor value is then adjusted until the overshoot period is almost over by the time the transistor is saturated. This is the optimum drive condition. A resistor in series with the capacitor (typically R/2) can be used to limit the peak base current overshoot and remove any undesirable oscillations.

The initial period of overshoot is especially necessary in circuits where the collector current rises quickly (ie square wave switching circuits and circuits with a high snubber discharge current). In these circuits the transistor would otherwise be conducting a high collector current during the early stages of the turn on period where the collector voltage can still be high. This would lead to an unacceptable level of turn on dissipation.

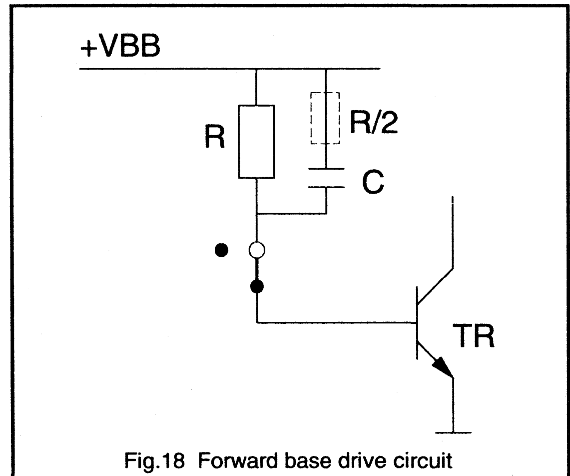


Fig.18 Forward base drive circuit

Note 3. *Square wave switching circuits, and circuits with a high snubber discharge current, are very susceptible to high turn on dissipation. Using an RC network in series with the forward base current path increases the turn on speed and therefore overcomes this problem.*

It should also be noted that during power up of power supply units, when all the output capacitors of the supply are discharged, the collector current waveform is often very different to that seen under normal running conditions. The rising edge of the collector current waveform is often faster, the collector current pulse width is often wider and the peak collector current value is often higher.

In order to prevent excessive collector current levels (and transformer saturation) a 'soft start' could be used to limit the collector current pulse width during power up. Alternatively, since many power supply designs are now using current mode control, excessive collector current can be avoided simply be setting the overcurrent threshold at an acceptable level.

Note 4. *Using the 'soft start' and/or the overcurrent protection capability of the SMPS control IC prevents excessive collector current levels at power up.*

Improving turn off

As far as the collector current is concerned, optimum turn off for a particular device is determined by how quickly the structure of the device will allow the stored charge to be extracted. If the device is turned off too quickly, charge gets trapped in the collector when the collector base junction recovers. Trapped charge takes time to recombine leading to a long collector current tail at turn off and hence high turn off losses. On the other hand, if the device is turned off too slowly, the collector voltage starts to rise prematurely (ie while the collector current is at its peak). This would also lead to high turn off losses.

Note 1. *Turning the transistor off either too quickly or too slowly leads to high turn off losses.*

Optimum turn off is achieved by using the correct combination of reverse base drive and storage time control. Reverse base drive is necessary to prevent storage times from being too long (and also to give the maximum RBSOAR). Storage time control is necessary to prevent storage times from being too short.

Storage time control is achieved by the use of a small inductor in series with the reverse base current path (see Fig.19). This controls the slope of the reverse base current (as shown in Fig.20) and hence the rate at which charge is extracted from the collector. The inductor, or *'base coil'*, is typically between 1 and 6 µH, depending on the reverse base voltage and the required storage time.

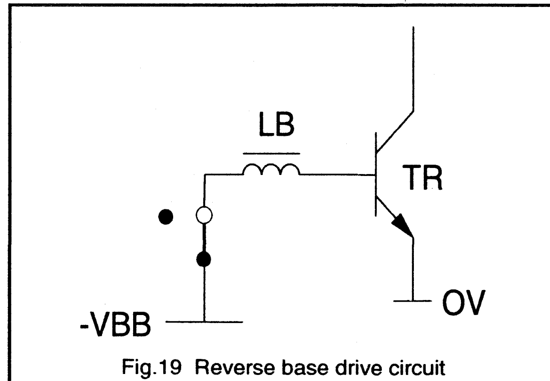


Fig.19 Reverse base drive circuit

Note 2. *Applying a base coil in series with the reverse base current path increases the transistor storage time but reduces both the fall time and the turn off losses.*

Applying this small base inductor will usually mean that the base emitter junction of the transistor is brought into breakdown during part of the turn off cycle. This is not a problem for the device because the current is controlled by the coil and the duty cycle is low.

If the transistor being used is replaced by a transistor of the same technology but having either a higher current rating or a higher voltage rating, then the volume of the collector increases. If the collector volume increases then the volume of charge in the collector, measured at the same saturation voltage, also increases. Therefore the required storage time for optimum turn off increases and also the required negative drive energy increases.

Overdriving the transistor (ie. driving it well into saturation) also increases the volume of stored charge and hence the required storage time for optimum turn off. Conversely, the required storage time for a particular device can be reduced by using a desaturation network such as a Baker clamp. The Baker clamp reduces the volume of stored charge by holding the transistor out of heavy saturation.

Note 3. *The required storage time for optimum turn off and the required negative drive energy will both increase as the volume of stored charge in the collector is increased.*

The reverse base current reaches its peak value at about the same time at which the collector current reaches its peak value. The turn off waveforms are shown in Fig.20.

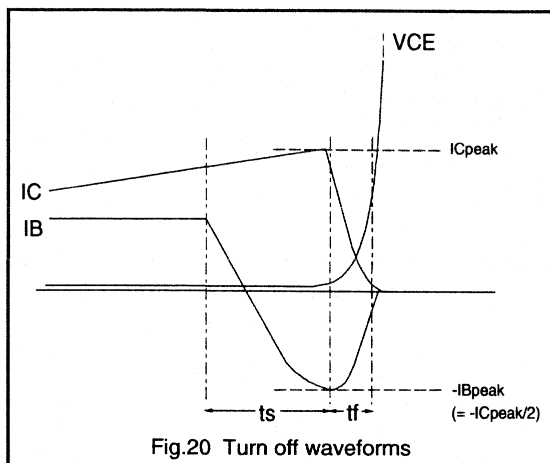


Fig.20 Turn off waveforms

Note 4. *For optimum turn off of any transistor, the peak reverse base current should be half of the peak collector current and the negative drive voltage should be between 2 and 5 volts.*

As far as the collector voltage is concerned, the slower the dV/dt the lower the turn off dissipation. Control of the collector dV/dt is achieved by the use of a snubber network (see Fig.21). The snubber capacitor also controls the collector voltage overshoot and thus prevents overvoltage of the transistor.

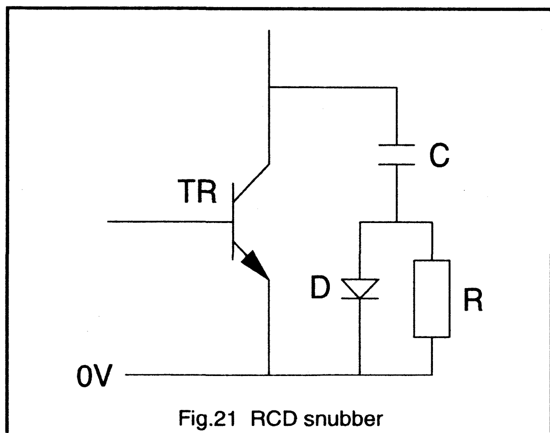


Fig.21 RCD snubber

High collector dV/dt at turn off can bring an additional problem for the transistor. A charging current flows through the collector base (Miller) capacitance of the device, and according to the law, I = C x dV/dt, this charging current increases in magnitude with increasing dV/dt. If this current enters the base then the transistor can begin to turn back on. Control of the collector dV/dt is usually enough to prevent this from happening. If this is insufficient then the base emitter impedance must be reduced by applying a resistor and/or capacitor between base and emitter to shunt some of this current.

Note 5. *High collector dV/dt at turn off leads to parasitic turn on if the charging current of the transistor Miller capacitance is not shunted away from the base.*

High collector dI/dt at turn off can also bring problems if the inductance between the emitter and the base ground reference is too high. The falling collector current will induce a voltage across this inductance which takes the emitter more negative. If the voltage on the emitter falls below the voltage on the base then the transistor can begin to turn back on. This problem is more rare but if it does arise then adding a resistor and/or capacitor between base and emitter helps to keep the base and emitter more closely coupled. At all times it is important to keep the length of the snubber wiring to an absolute minimum.

Note 6. *High collector dI/dt at turn off leads to parasitic turn on if the inductance between the emitter and the base ground reference is too high.*

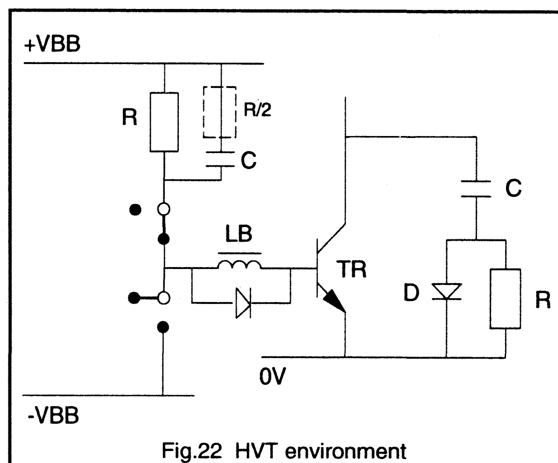


Fig.22 HVT environment

Improving reliability

In the majority of cases, the most stressful circuit conditions occur during power up of the SMPS, when the base drive is least well defined and the collector current is often at its highest value. However, the electrical environment at power up is very often hardly considered, and potentially destructive operating conditions go unnoticed.

A very common circuit reliability problem is RBSOAR failure occurring on the very first switching cycle, because the reverse drive to the base needs several cycles to become established. With no negative drive voltage on the base of the transistor, the RBSOAR is reduced (as discussed earlier). To avoid RBSOAR failure, the collector voltage must be kept below V_{CEOmax} until there is sufficient reverse drive energy available to hold the base voltage negative during the turn off phase.

Even with the full RBSOAR available, control of the rate of rising collector voltage through the use of a snubber is often essential in order to keep the device within the specified operating limits.

Note 1. *The conditions at power up often come close to the safe operating limits. Until the negative drive voltage supply is fully established, the transistor must be kept below its* V_{CEOmax}.

Another factor which increases the stress on many components is increased ambient temperature. It is essential that the transistor performance is assessed at the full operating temperature of the circuit. As the temperature of the transistor chip is increased, both turn on and turn off losses may also increase. In addition to this, the quantity of stored charge in the device rises with temperature, leading to higher reverse base drive energy requirements.

Note 2. *Transistor performance should be assessed under all operating conditions of the circuit, in particular the maximum ambient temperature.*

A significant proportion of power supply reliability problems could be avoided by applying these two guidelines alone. By making use of the information on how to improve turn on and turn off, small design changes can be made to the circuit which will enhance the electrical performance and reliability of the transistor, leading to a considerable improvement in the performance and reliability of the power supply as a whole.

2.1.3 Base circuit design for high voltage bipolar transistors in power converters

Fast high voltage switching transistors, such as the BUT11 and BUT12, the BUW13, the BUV47 and BUV48, all have helped simplify the design of converters circuits for power supply applications. Because the breakdown voltage of these transistors is high (from 850 to 1000V), they are suitable for operation direct from the rectified 220V or 240V mains supply. Furthermore, their fast switching properties allow the use of converter operating frequencies at up to 30kHz (with emitter switching techniques pushing this figure past 100kHz Ref[1]).

The design of converter circuits using high-voltage switching transistors requires a careful approach. This is because the construction of these transistors and their behaviour in practical circuits is different from those of their low-voltage counterparts. In this article solutions to base circuit design for transistor converters and comparable circuits are developed from a consideration of the construction and the inherent circuit behaviour of high voltage switching transistors.

Switching behaviour

Fig.1 shows a complete period of typical collector voltage and current waveforms for a power transistor in a switching converter. The turn-on and turn-off intervals are indicated. The switching behaviour of the transistor during these two intervals, and the way it is influenced by the transistor base drive, will now be examined.

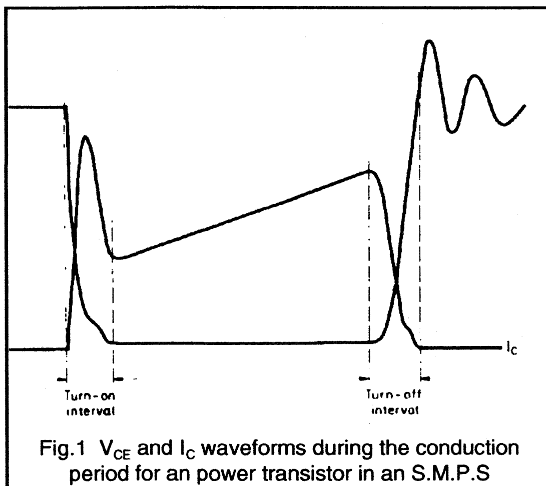


Fig.1 V_{CE} and I_C waveforms during the conduction period for an power transistor in an S.M.P.S

Turn-on behaviour

A particular set of voltage and current waveforms at the collector and base of a converter transistor during the turn-on interval is shown in Fig.2(a). Such waveforms are found in a power converter circuit in which a (parasitic) capacitance is discharged by a collector current pulse at transistor turn-on. The current pulse due to this discharge can be considered to be superimposed on the trapezoidal current waveform found in basic converter operation.

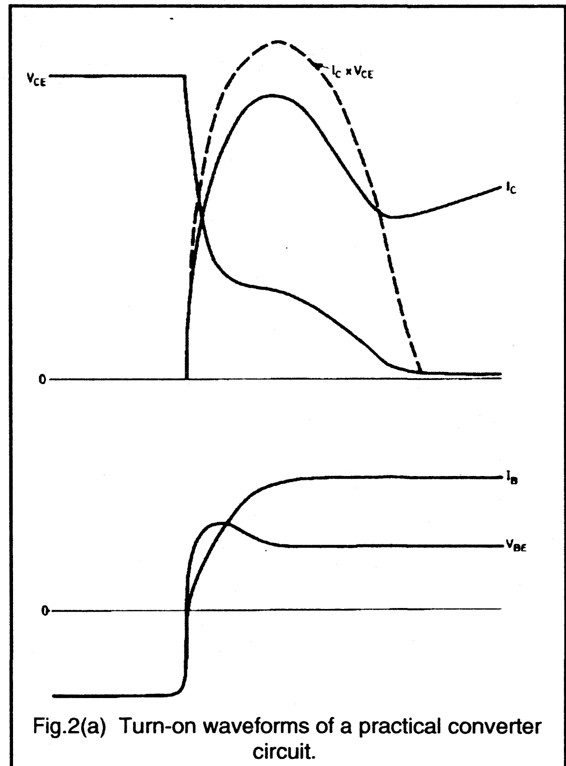


Fig.2(a) Turn-on waveforms of a practical converter circuit.

A positive base current pulse I_B turns on the transistor. The collector-emitter voltage V_{CE} starts to decrease rapidly and the collector current I_C starts to increase. After some time, the rate of decrease of V_{CE} reduces considerably, and V_{CE} remains relatively high because of the large collector current due to the discharge of the capacitance. Thus, the turn-on transient dissipation (shown by a broken line) reaches a high value.

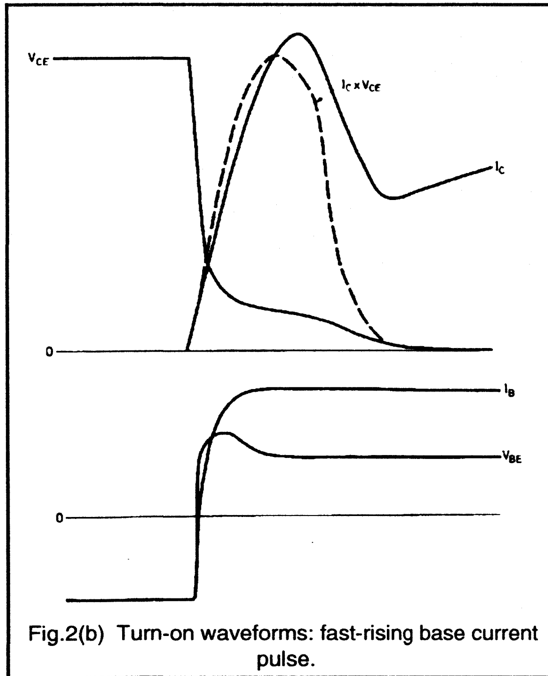


Fig.2(b) Turn-on waveforms: fast-rising base current pulse.

The collector current then decreases to a trough before assuming the normal trapezoidal waveform. This is again followed by a rapid decrease in V_{CE}, which reaches the saturation value defined by the collector current and base current of the particular transistor.

Fig.2(b) depicts a similar situation but for a greater rate of rise of the base current. The initial rapid decrease in V_{CE} is maintained until a lower value is reached, and it can be seen that the peak and average values of turn-on dissipation are smaller than they are in Fig.2(a).

Fig.2(c) shows the effect on the transistor turn-on behaviour of a very fast rising base current pulse which initially overshoots the final value. The collector-emitter voltage decreases rapidly to very nearly the transistor saturation voltage. The turn-on dissipation pulse is now lower and much narrower than those of Figs.2(a) and 2(b).

From the situations depicted in Figs.2(a), 2(b) and 2(c), it follows that for the power transistor of a converter circuit the turn-on conditions are most favourable when the driving base current pulse has a fast leading edge and overshoots the final value of I_B.

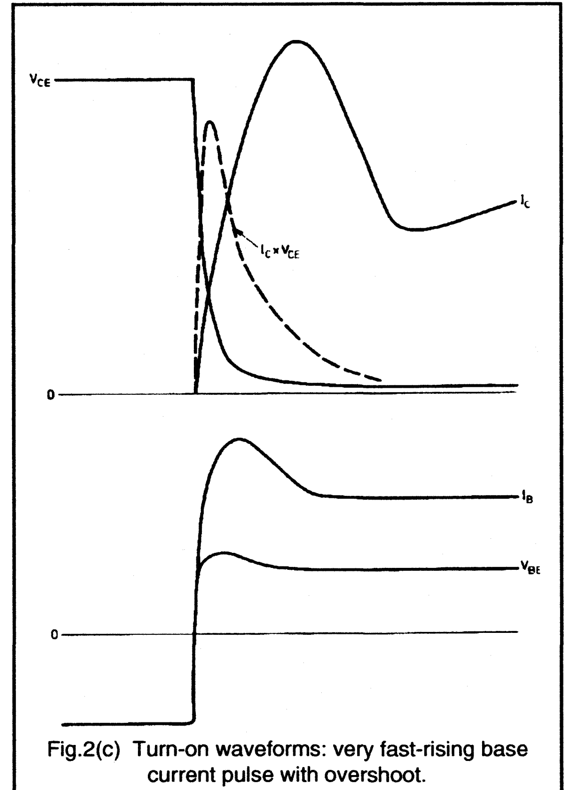


Fig.2(c) Turn-on waveforms: very fast-rising base current pulse with overshoot.

Turn-off behaviour

The waveforms which occur during the turn-off interval indicated in Fig.1 are shown on an expanded timescale and with four different base drive arrangements in Figs.3(a) to 3(d). These waveforms can be provided by base drive circuits as shown in Figs.4(a) to 4(c): the circuit of Fig.4(a) provides the waveforms of Figs.3(a); the circuit of Fig.4(b) those of Fig.3(b) and, with an increased reverse drive voltage, Fig.3(c); the circuit of Fig.4(c) provides the waveforms of Figs.3(d). The waveforms shown are typical of those found in the power switching stages of S.M.P.S, and television horizontal deflection circuits, using high-voltage transistors.

In practical circuits, the waveform of the collector-emitter voltage is mainly determined by the arrangement of the collector circuit. The damping effect of the transistor on the base circuit is negligible except during the initial part of the turn-off period, when it only causes some delay in the rise of the V_{CE} pulse.

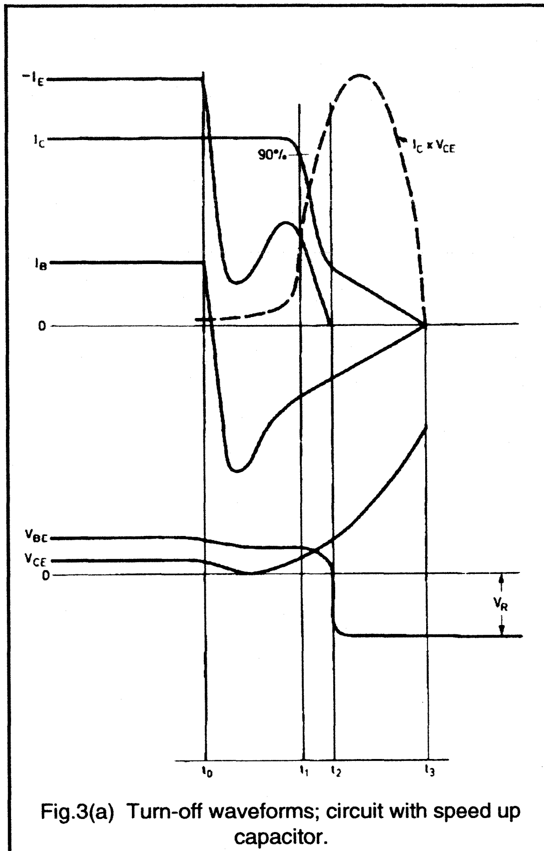


Fig.3(a) Turn-off waveforms; circuit with speed up capacitor.

The $I_C \times V_{CE}$ (turn-off dissipation) pulse is dependent on both the transistor turn-off time and the collector current waveshape during turn-off. Turn-off dissipation pulses are indicated in Figs.3(a) to 3(d) by the dashed lines.

The circuit of Fig.4(a) incorporates a speed up capacitor, an arrangement often used with low-voltage transistors. The effect of this is as shown in Fig.3(a), a very rapid decrease in the base current I_B, which passes through a negative peak value, and becomes zero at t_3. The collector current I_C remains virtually constant until the end of the storage time, at t_1, and then decreases, reaching zero at t_3. The waveform of the emitter current, I_E, is determined by I_C and I_B, until it reaches zero at t_2, when the polarity of the base-emitter voltage V_{BE} is reversed.

After time t_2, when V_{BE} is negative and I_E is zero, the collector base currents are equal and opposite, and the emitter is no long effective. Thus, the further decrease of collector current is governed by the reverse recovery process of the transistor collector-base diode. The reverse recovery 'tail' of I_C (from t_2 to t_3) is relatively long, and it is clear the turn-off dissipation is high.

In the circuit of Fig.4(b) the capacitor is omitted. Fig.3(b) shows that the negative base current is limited to a considerably lower value than in the previous case. All the currents I_B, I_C and I_E reach zero at time t_3. The transistor emitter base junction becomes reverse biased at t_2, so that during the short interval from t_2 to t_3 a small negative emitter current flows.

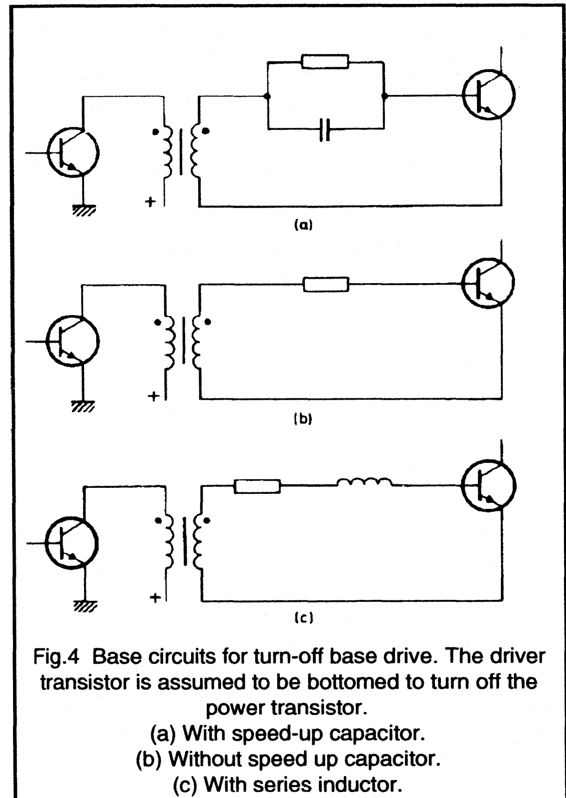


Fig.4 Base circuits for turn-off base drive. The driver transistor is assumed to be bottomed to turn off the power transistor.
(a) With speed-up capacitor.
(b) Without speed up capacitor.
(c) With series inductor.

The emitter current, determined by the collector current and by the (driven) base current, therefore maintains control over the collector until it reaches zero. Furthermore, the collector current has a less pronounced tail and so the fall time is considerably shorter than that of Fig.3(a). The turn-off dissipation is also lower than in the previous case.

Increasing the reverse base drive voltage in the circuit of Fig.4(b), with the base series resistance adjusted so that the same maximum reverse base current flows, gives rise to the waveforms shown in Fig.3(c). The collector current tail is even less pronounced, and the fall time shorter than in Fig.3(b).

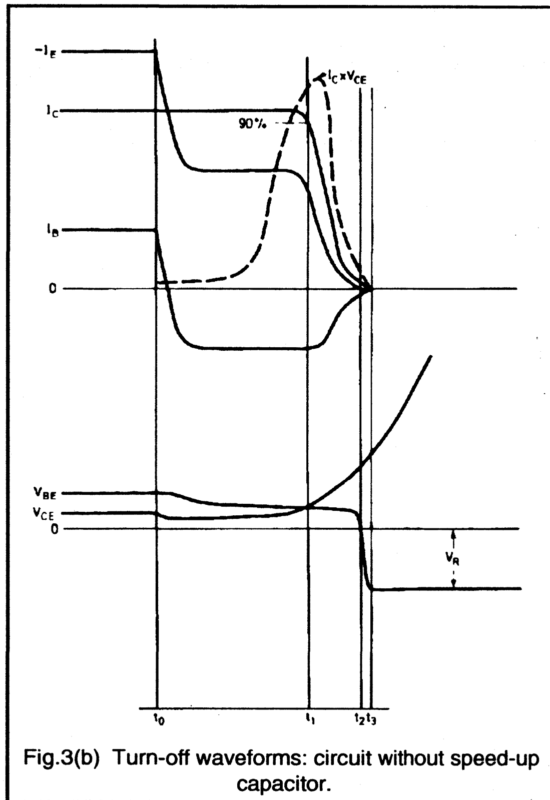


Fig.3(b) Turn-off waveforms: circuit without speed-up capacitor.

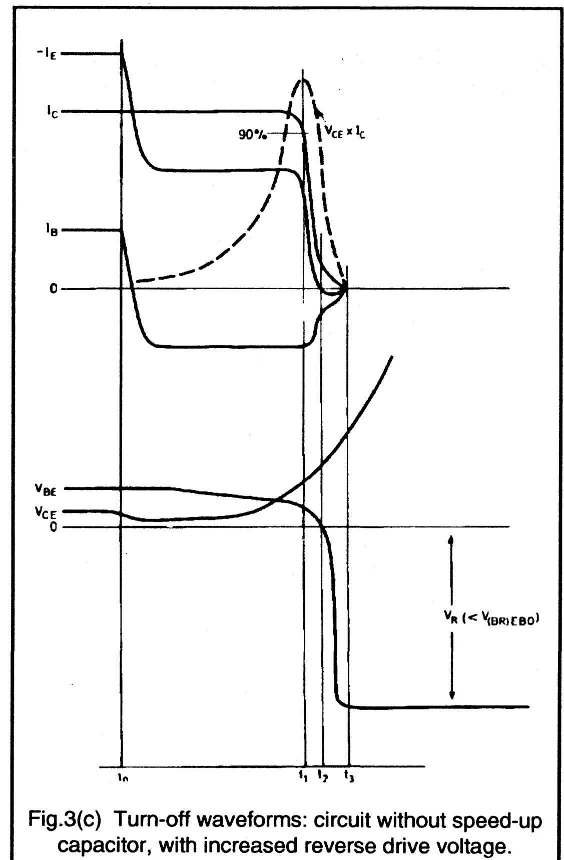


Fig.3(c) Turn-off waveforms: circuit without speed-up capacitor, with increased reverse drive voltage.

A further improvement in turn-off behaviour can be seen in the waveforms of Fig.3(d), which are obtained by including an inductor in the base circuit as in Fig.4(c). The rate of change of the negative base current is smaller than in the preceding cases, and the negative peak value of the base current is smaller than in Fig.3(a). The collector current I_C reaches zero at t_3, and from t_3 to t_4 the emitter and base currents are equal. At time t_2 the polarity of V_{BE} is reversed and the base-emitter junction breaks down. At time t_4 the negative base-emitter voltage decreases from the breakdown value $V_{(BR)EBO}$ to the voltage V_R produced by the drive circuit.

The collector current fall time in Fig.3(d) is shorter than in any of the previous cases. The emitter current maintains control of the collector current throughout its decay. The large negative value of V_{BE} during the final part of the collector current decay drives the base-emitter junction into breakdown, and the junction breakdown voltage determines the largest possible reverse voltage. The turn-off of the transistor is considerably accelerated by the application (correctly timed) of this large base emitter-voltage, and the circuit gives the lowest turn-off dissipation of those considered.

The operation of the base-emitter junction in breakdown during transistor turn-off, as shown in Fig.3(d) has no detrimental effects on the behaviour of transistors such as the BUT11 or BU2508 types. Published data on these transistors allow operation in breakdown as a method of achieving reliable turn-off, provided that the $-I_{B(AV)}$ and $-I_{BM}$ ratings are not exceeded.

It is evident from Figs.3(a) to 3(d) that the respective turn-off dissipation values are related by:-

$$P_{off(a)} > P_{off(b)} > P_{off(c)} > P_{off(d)}$$

The fall times (related in each case to the interval from t_1 to t_3) are given by:-

$$t_{f(a)} > t_{f(b)} > t_{f(c)} > t_{f(d)}$$

The storage times (equal to the interval from t_0 to t_1) are:-

$$t_{s(a)} < t_{s(b)} < t_{s(d)}$$

where the subscripts (a), (b), (c) and (d) refer to the waveforms of Figs.3(a), 3(b), 3(c) and 3(d) respectively. It follows that the circuit of Fig.4(c), which provides the waveforms of Fig.3(d), gives the most favourable turn-off power dissipation. It has, however, the longest storage time.

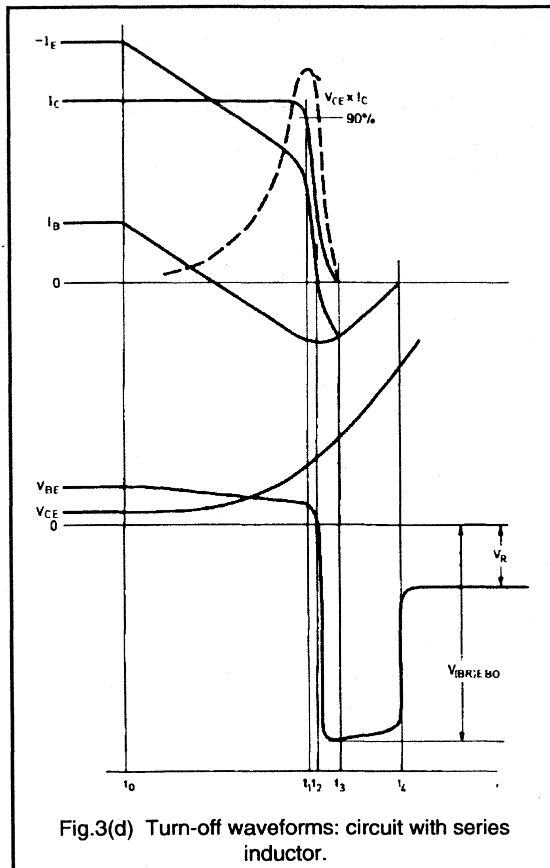


Fig.3(d) Turn-off waveforms: circuit with series inductor.

From consideration of the waveforms in Figs.3(a) to 3(d), it can be concluded that optimum turn-off of a high voltage transistor requires a sufficiently long storage time determined by the turn-off base current and a sufficiently large negative base-emitter voltage correctly timed with respect to the collector current waveform.

The phenomena which have been described in this section become more pronounced when the temperature of the operating junction of the transistor is increased: in particular, the fall times and storage times are increased. The design of a base drive circuit should therefore be checked by observing the waveforms obtained at elevated temperatures.

Optimum base drive circuitry

From the foregoing study of the required base current and base-emitter voltage waveforms, a fundamental base circuit arrangement to give optimum turn-on and turn-off of high voltage switching transistor will now determined. It will be assumed that the driver stage is transformer-coupled to the base, as in Fig.5(a), and that the driver transformer primary circuit is such that a low impedance is seen, looking into the secondary, during both the forward and reverse drive pulses. The complete driver circuit can then be represented as an equivalent voltage source of $+V_1$ volts during the forward drive period and $-V_2$ volts during the reverse drive/bias period. This is shown in Fig.5(b).

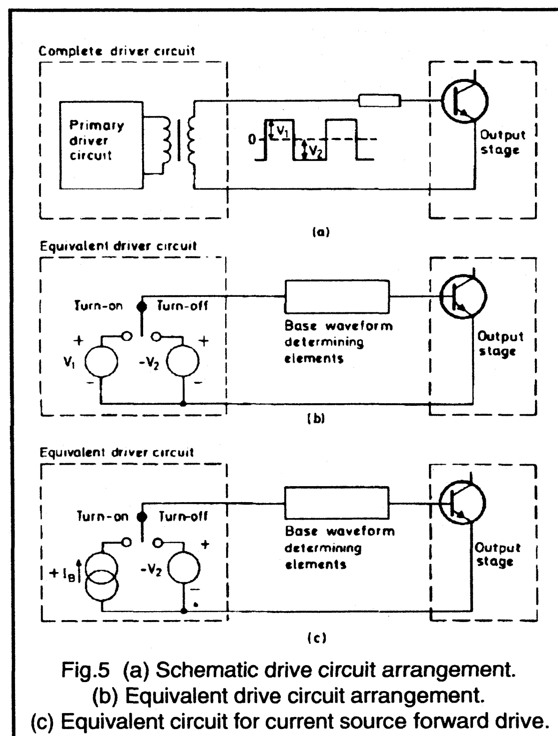


Fig.5 (a) Schematic drive circuit arrangement.
(b) Equivalent drive circuit arrangement.
(c) Equivalent circuit for current source forward drive.

Forward base drive can also be obtained from a circuit which acts as a current source rather than a voltage source. This situation, where the reverse drive is still obtained from a voltage source, is represented in Fig.5(c). The basic circuit arrangements of Figs.5(b) and 5(c) differ only with respect to forward drive, and will where necessary be considered separately.

Comparable base drive waveforms can, of course, be obtained from circuits differing from those shown in Figs.5(b) and 5(c). For such alternative circuit configurations the following discussion is equally valid.

Base series resistor

Most drive circuits incorporate a resistor R_B in series with the base. The influence of the value of this resistor on the drive characteristic will be briefly discussed.

Voltage source forward drive.

In circuits with a voltage source for forward drive, shown in a simplified from in Fig.6(a), the following parameters determine the base current:-

The transistor base characteristic ;

The value of the base resistor R_B;

The forward drive voltage V_1.

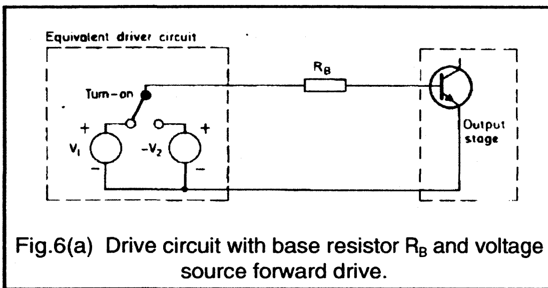


Fig.6(a) Drive circuit with base resistor R_B and voltage source forward drive.

Fig.6(b) shows how the tolerances in these parameters affect the base current. It is clear that to avoid large variations in I_B, the tolerances in R_B and V_1 should be minimised. The voltage drop across R_B reduces the dependence of I_B on the spreads and variations of the transistor $V_{BE(on)}$. For good results the voltage drop across R_B must not be less than $V_{BE(on)}$.

Current source forward drive

In circuits where a current source is used for forward drive, the forward base current is independent of spreads and variations of $V_{BE(on)}$. The base current level and tolerances are governed entirely by the level and tolerances of the drive. A separate base series resistor is therefore unnecessary, but is nevertheless included in many practical current-source-driven circuits, to simplify the drive circuit design. The following discussions will assume that a series base resistor R_B always forms part of the base drive network.

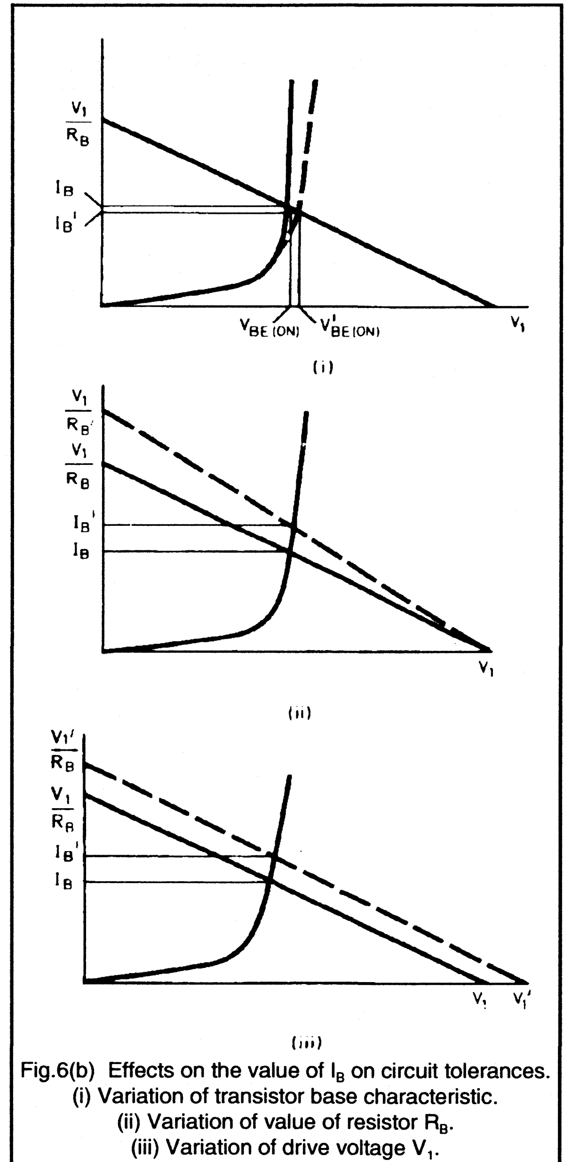


Fig.6(b) Effects on the value of I_B on circuit tolerances.
(i) Variation of transistor base characteristic.
(ii) Variation of value of resistor R_B.
(iii) Variation of drive voltage V_1.

Turn-off arrangement

To initiate collector current turn-off, the drive voltage is switched at time t_0 from the forward value $+V_1$ to the reverse value $-V_2$.

Fig.7(a) Turn-off waveforms of the circuit of Fig.7(b)

The desired turn-off voltage and current waveforms are obtained by adding various circuit elements to the basic resistive circuit of Fig.6(a). A convenient method of achieving the desired slowly-decreasing base current is to use a series inductor L_B as shown in Fig.7(b). The turn-off waveforms obtained by this method are shown in Fig.7(a).

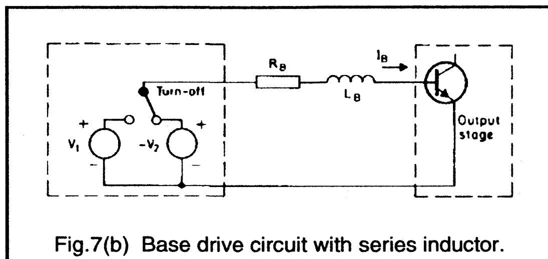


Fig.7(b) Base drive circuit with series inductor.

Base series inductor

At time t_0 the base current starts to decrease from the forward drive value I_{B1} with a slope equal to:-

$$\frac{-V_2 \;-\; (+V_{BE(on)})}{L_B}$$

For a considerable time after t_0, the (decreasing) input capacitance of the transistor maintains a charge such that there is no perceptible change in V_{BE}. At time t_2 the amount of charge removed by the negative base current ($-I_B$) is insufficient to maintain this current, and its slope decreases.

At time t_3, when:-

$$\frac{d\,I_B}{dt}=0 \quad where \quad I_B=I_{B2}$$

$$V_{BE} \;=\; -V_2-R_B I_{B2}$$

Immediately after t_3, the stored energy in L_B gives rise to a voltage peak tending to increase the reverse bias of the transistor. The voltage is clamped by the base-emitter breakdown voltage, so that:-

$$V_{BE} = -V_{(BR)EBO}$$

At time t_4 the negative base current starts to decrease with an initial slope equal to:-

$$\frac{-V_2 + V_{(BR)EBO}}{L_B}$$

At t_5 the base current reaches zero. The base-emitter voltage then changes from $-V_{(BR)EBO}$ to the value $-V_2$, the level of the drive voltage. As has been demonstrated, the collector storage time, t_s is an important parameter of the drive circuit turn-off behaviour. Fig.7(a) shows that the value of t_s can be calculated approximately from:-

$$\frac{-V_2 + V_{(BR)EBO}}{L_B}.t_s = I_{B1} - I_{B2}$$

and this expression is sufficiently accurate in practice. In most cases the base current values are related by:-

$$\left(\frac{I_{B2}}{I_{B1}}\right) \approx 1 \ to \ 3$$

In the case where $(-I_{B2} / I_{B1}) = 2$, the collector storage time is given by:-

$$t_s = \frac{3 I_{B1} L_B}{-V_2 - (+V_{BE(on)})}$$

In practical circuits, design considerations frequently indicate a relatively small value for V_2. The required value of t_s is then obtained with a small value of L_B, and consequently the energy stored in the inductor ($1/2 \, L_B I_{B2}^2$) is insufficient to maintain the base-emitter junction in the breakdown condition. Fig.7(a) shows that breakdown should continue at least until the collector current is completely turned off. The higher the transistor junction temperature, the more stored energy is necessary to maintain breakdown throughout the increased turn-off time.

These phenomena are more serious in applications where the storage time must be short, as is the case for the BUV47 and BUV48 transistors. For horizontal deflection output transistors such as the BU508 and BU2508, which require a much longer storage time, the base inductance usually stores sufficient energy for correct turn-off behaviour.

Diode assisted base inductor

It is possible to ensure the storage of sufficient turn-off energy by choosing a relatively large value for V_2. Where a driver transformer is employed, there is then a corresponding increase in V_1. To obtain the desired value of forward base current, the base resistance R_B must also be large. A large value of R_B, however, diminishes the effect of L_B on the transistor turn-off behaviour, unless R_B is bypassed by a diode as in Fig.8.

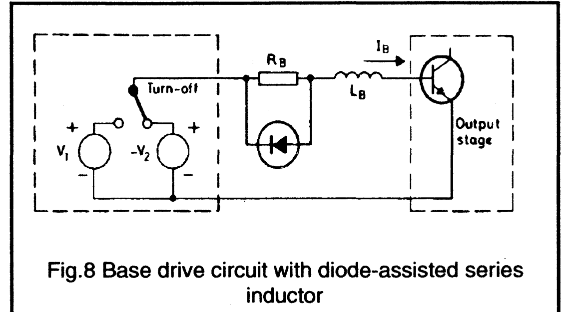


Fig.8 Base drive circuit with diode-assisted series inductor

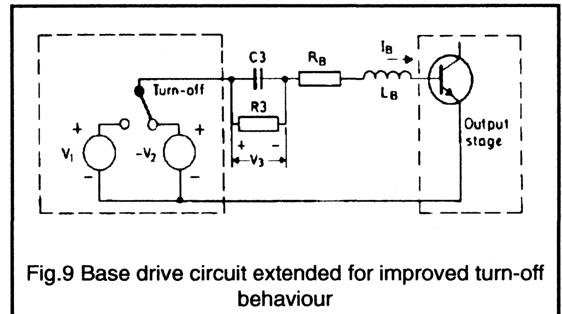


Fig.9 Base drive circuit extended for improved turn-off behaviour

Turn-off RC network

Improved turn-off behaviour can be obtained without increasing V_2, if additional circuit elements are used. An arrangement used in practice is shown in Fig.9, and consists of network R_3C_3 which is connected in series with R_B and L_B.

A voltage V_3 is developed across C_3 because of the forward base current. (This voltage drop must be compensated by a higher value of V_1). When reverse current flows at turn-off, the polarity of V_3 is such that it assists the turn-off drive voltage V_2. Using the same approximation as before, the storage time is given by:-

$$t_s = \frac{3 I_{B1} L_B}{-(V_2 + V_3) - (+V_{BE(on)})}$$

The same value of t_s now requires a larger value of L_B. The energy stored in L_B is therefore greater and the transistor can more reliably be driven into breakdown for the time required.

The waveforms of Fig.7(a) are equally applicable to the circuit of Fig.9, if V_2 is replaced by $(V_2 + V_3)$. In practice V_3 will not remain constant throughout the storage time, and replacing V_3 by its instantaneous value will make a slight difference to the waveforms.

Turn-on arrangements

It has been shown that for optimum turn-on of a high voltage switching transistor, the turn-on base current pulse must have a large amplitude and a fast leading edge with overshoot. The inductance L_B included in the circuits derived for optimum turn-off (Figs.7 to 9), however makes it difficult to produce such a turn-on pulse. The additional components (R_1, C_1, D_1) in the circuit of Fig.10(a) help to solve this problem as shown by the waveforms of Fig.10(b).

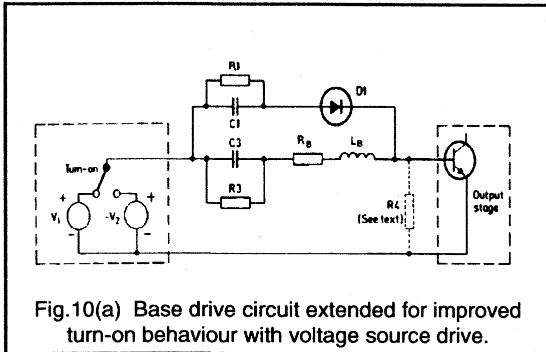


Fig.10(a) Base drive circuit extended for improved turn-on behaviour with voltage source drive.

At the instant of turn-on, network R_1C_1 in series with D_1 provides a steep forward base current pulse. The turn-off network is effectively by-passed during the turn-on period by C_1 and D_1. The time-constant R_1C_1 of the turn-on network should be chosen so that the forward current pulse amplitude is reduced virtually to zero by the time the transistor is turned on.

The turn-on network of Fig.10(a) can also be added to the diode-assisted turn-off circuit of Fig.8. In circuits which are forward driven by a current source, the overshoot required on the turn-on base current pulse must be achieved by appropriate current source design.

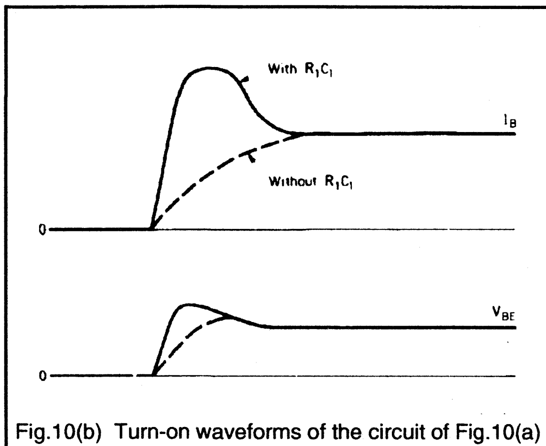


Fig.10(b) Turn-on waveforms of the circuit of Fig.10(a)

Practical circuit design

The base drive circuit of Fig.10(a) combines the drive voltage sources $+V_1$ and $-V_2$ with circuit elements R_B, L_B, R_3C_3 and $R_1C_1D_1$, which, if correctly dimensioned, allow optimum transient behaviour of the switching transistor. Not all these elements, however, will be necessary in every case for good results.

In circuits where the collector current rate of rise is limited by collector circuit inductance, the turn-on network $R_1C_1D_1$ can be omitted without danger of excessive collector dissipation at turn-on. In circuits where the base series inductance L_B is sufficiently large to give complete turn-off, network R_3C_3 can be omitted. Networks $R_1C_1D_1$ and R_3C_3 are superfluous in horizontal deflection circuits which use BU508, BU2508 transistors or similar types.

A discrete components for inductance L_B need not be always included, because the leakage inductance of the driver transformer is sometimes sufficient.

The omission of R_B from circuits which are forward driven by a voltage source should generally be considered bad design practice. It is, however, possible to select component values such that the functions of R_1C_1 and R_3C_3 are combined in a single network.

In some cases, the circuits of Figs 7 to 10 may generate parasitic oscillations (ringing). These can usually be eliminated by connecting a damping resistor R_4 between the transistor base and emitter, as shown in broken lines in Fig.10(a).

Physical behaviour of high-voltage switching transistors

Base circuit design for high-voltage switching transistors will now be considered with respect to the physical construction of the devices. To achieve a high breakdown voltage, the collector includes a thick region of high resistivity material. This is the major difference in the construction of high and low voltage transistors.

The construction of a triple-diffused high voltage transistor is represented schematically in Fig.11(a). The collector region of a n-p-n transistor comprises a high resistivity n- region and a low resistivity n+ region. Most of the collector voltage is dropped across the n- region. For semiconductor material of a chosen resistivity, the thickness of the n- region is determined by the desired collector breakdown voltage. The thickness of the n+ region is determined by technological considerations, in particular the mechanical construction of the device. Fig.11(b) shows the impurity concentration profile of the transistor of Fig.11(a).

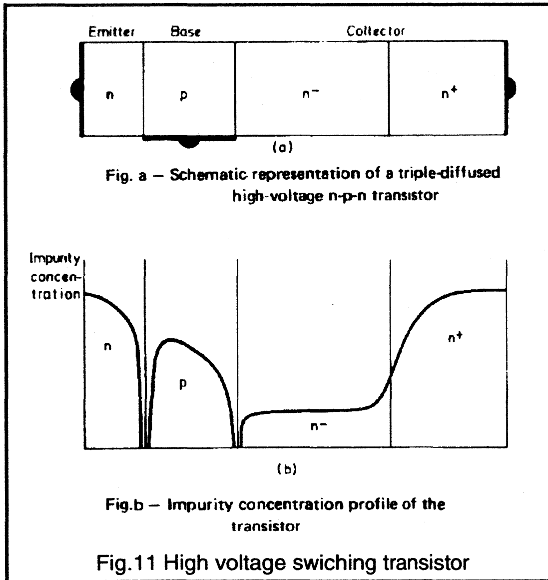


Fig.11 High voltage swiching transistor

For good switching performance, the high voltage blocking characteristic of the transistor structure must be modified at transistor turn-on, so that a low forward voltage condition is exhibited. One method of achieving this is to inject a large number of carriers through the base to the collector region. The high resistivity of the n- region is then "swamped" by excess carriers. This effect is often referred to as a collector-width modulation.

The following discussion of the physical changes which occur at transistor turn-on and turn-off is based on a much simplified transistor model; that is, the one dimensional charge control model. Fig.12 shows such a model of a low-voltage transistor, and assumes a large free carrier-to-doping concentration ratio in the base due to the carriers injected from the emitter. Line *a* represents the free carrier concentration in the base for transistor operation in the active region (V_{CB}>0), and line *c* that for the saturated condition (V_{CB}<0). Line *b* represents the concentration at the onset of saturation, where V_{CB}=0. The slope of the free carrier concentration line at the collector junction is proportional to the collector current density, and therefore, to the collector current.

Turn-on behaviour

The carrier concentration profile of a high-voltage transistor during turn-on is shown in Fig.13. Line 1 represents a condition where relatively few carriers are injected into the base from the emitter. Let line 1 be defined as representing the onset of saturation for the metallurgic collector junction; that is, point 1(C'). In this case V_{CB}=0, whereas the externally measured collector voltage is very high, because of the voltage drop across the high-resistivity collector region.

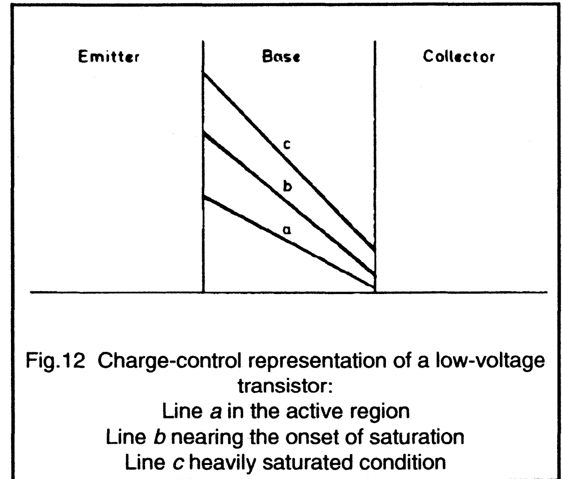


Fig.12 Charge-control representation of a low-voltage transistor:
Line *a* in the active region
Line *b* nearing the onset of saturation
Line *c* heavily saturated condition

Line 2 in Fig.13(a) represents a high level of carrier injection into the base from the emitter. Carriers have also penetrated the high-resistivity collector region as far as point 1(C'), and so the base region is now, in effect, extended to this point and the effective width of the collector region is reduced. The voltage drop across the collector region, caused by the collector current which is proportional to the concentration gradient at point 2(C'), is therefore less than the voltage drop which occurred with the level of carrier injection on line 1.

Lines 3, 4 and 5 represent still higher carrier injection levels, and hence decreasing effective collector widths. The voltage drop across the effective collector also decreases.

In the situation represented by line 6, the entire high resistivity collector region has been flooded with excess carriers. The collector-base voltage is therefore so low that the transistor is effectively saturated. The low saturation voltage has been obtained at the expense of a large base current, and this explains why a high-voltage transistor has a low current gain, especially at large collector currents.

Fig.13(b) shows simplified collector current/voltage characteristics for a typical high voltage transistor. Between lines OQ and OP, voltage V_{CE} progressively decreases as excess carriers swamp the high-resistivity collector region. Line OP can be regarded as the 'saturation' line.

When the transistor is turned on, the carrier injection level increases from the very small cut-off level (not shown in Fig.13(a)) to the level represented by line 6 in Fig.13(a). The transistor operating point therefore moves from the cut-off position along the locus shown in Fig.13(b) to position 6, which corresponds to line 6 in Fig.13(a). The

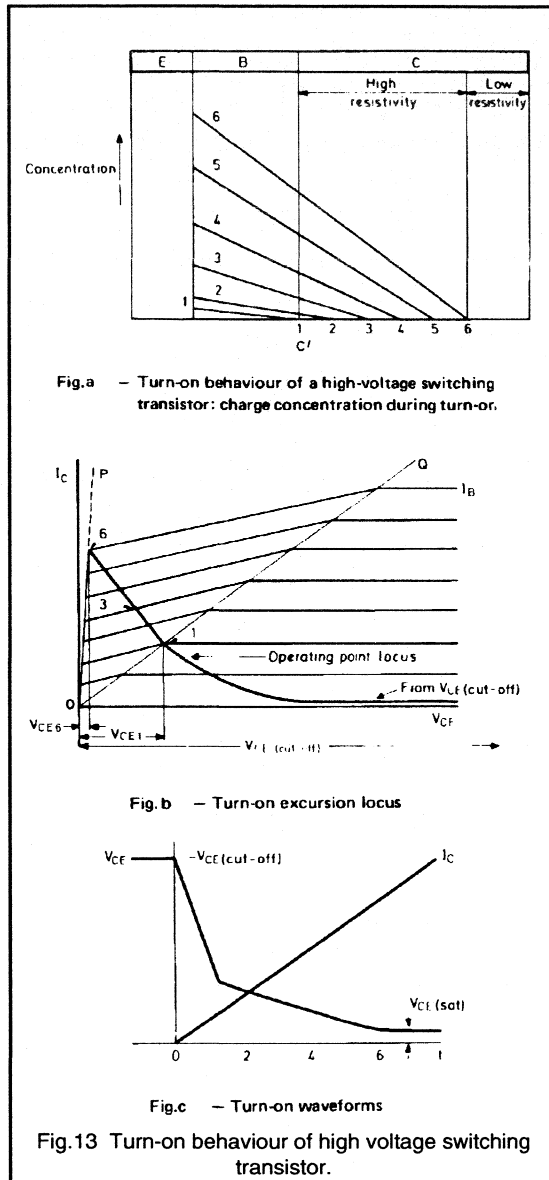


Fig.13 Turn-on behaviour of high voltage switching transistor.

effect of this process on I_C and V_{CE} is shown in Fig.13(c), where the time axis is labelled 0 to 6 to correspond to the numbered positions on the operating point locus of Fig.13(b) and the numbered lines on the carrier concentration diagram of Fig.13(a).

The time taken to reach the emitter injection level 6 is directly proportional to the turn-on time of the transistor. The rate of build-up of emitter injection depends on the peak amplitude and rise time of the turn-on base current pulse. The shortest turn-on time is obtained from a large amplitude base current pulse with a fast leading edge. Thus, physical considerations support the conclusion already drawn from a study of the circuit behaviour of the transistor.

Turn-off behaviour

The carrier concentration in the saturated transistor at the beginning of the turn-off period is represented by line 0 in Fig.14(a), corresponding to line 6 in Fig.13(a). As shown in Fig.14(b), the base current I_B gradually decreases, but I_C remains almost constant for some time, and $-I_E$ therefore decreases to match I_B. The resulting carrier concentration patterns are shown as lines 1 and 2 in Fig.14(a). This process is plotted against time in Fig.14(b) where, again, the graduation of the horizontal axis corresponds to that of the lines in Fig.14(a).

At time point 3 the emitter current has reduced to zero, and is slightly negative until point 6. Thus the carrier concentration lines 4 and 5 have negative slope. Complete collector current cut-off is reached before point 6. (This situation is not represented in Fig.14).

Excess carriers present in the collector region are gradually removed from point 0 onwards. This results in increasing collector voltage, because of the increasing effective width of the high-resistivity collector region.

Figs.14(a) and 14(b) depict a typical turn-off process giving good results with high voltage transistors; the waveforms of Fig.14(b) should be compared with those of Fig.3(d) and 7(a). A different process is shown in Figs.15(a) and 15(b). The initial situation is similar (line 0, Fig.15(a)) but the base current has a steep negative slope. At time point 1 of Fig.15(b), the emitter current $-I_E$ has reached zero, and so the carrier concentration line 1 has zero slope at the emitter junction. The emitter-base junction is effectively cut off and only the relatively small leakage current (not shown in Fig.15(b)) is flowing. From point 1 onwards, therefore, the emitter has no influence on the behaviour of the transistor. The switching process is no longer 'transistor action', but the reverse recovery process of a diode. The carrier concentration pattern during this process is shown in Fig.15(a) in broken lines, with zero slope at the emitter junction because the emitter is inoperative.

The reverse recovery process is slow, because of the high resistivity of the collector region and the consequent slow decrease of collector current. (Collector and base currents are, of course, equal and opposite when the emitter is cut off). The turn-off dissipation increases progressively as the transition time from collector saturation to cut-off increases.

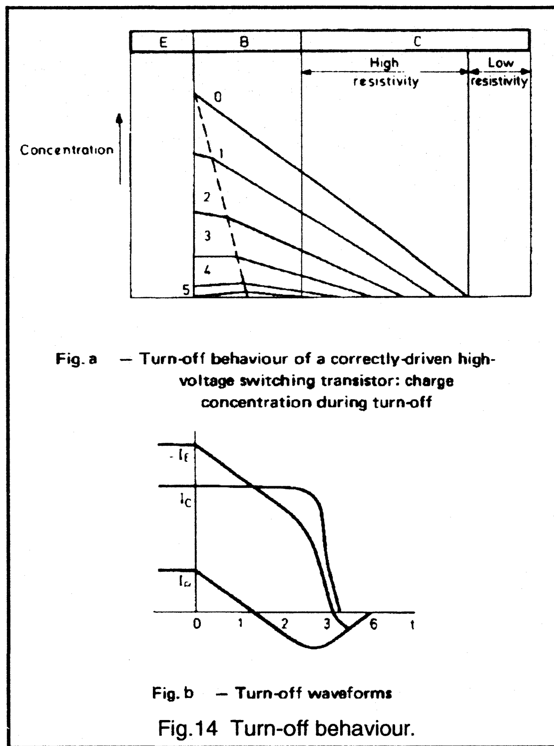


Fig. a — Turn-off behaviour of a correctly-driven high-voltage switching transistor: charge concentration during turn-off

Fig. b — Turn-off waveforms

Fig.14 Turn-off behaviour.

Furthermore, at higher junction temperatures the reverse recovery charge, and hence the duration of the recovery process, is greater.

The longer the turn-off time, then, the greater the turn-off dissipation, and hence the higher the device temperature which itself causes a further increase in turn-off time and dissipation. The avoid the risk of thermal runaway and subsequent transistor destruction which arises under these conditions, the turn-off drive must be such that no part of the turn-off is governed by the reverse recovery process of the collector base diode. Actual transistor action should be maintained throughout the time when an appreciable amount of charge is present in the transistor collector and base regions, and therefore the emitter should continue to operate to remove the excess charge.

There are many conditions of transistor turn-off which lie between the extreme cases of Figs.14(a) and 15(a). Circuits in which the operating conditions tend towards those shown in Fig.15(a) must be regarded as a potential source of unreliability, and so the performance of such circuits at elevated temperatures should be carefully assessed.

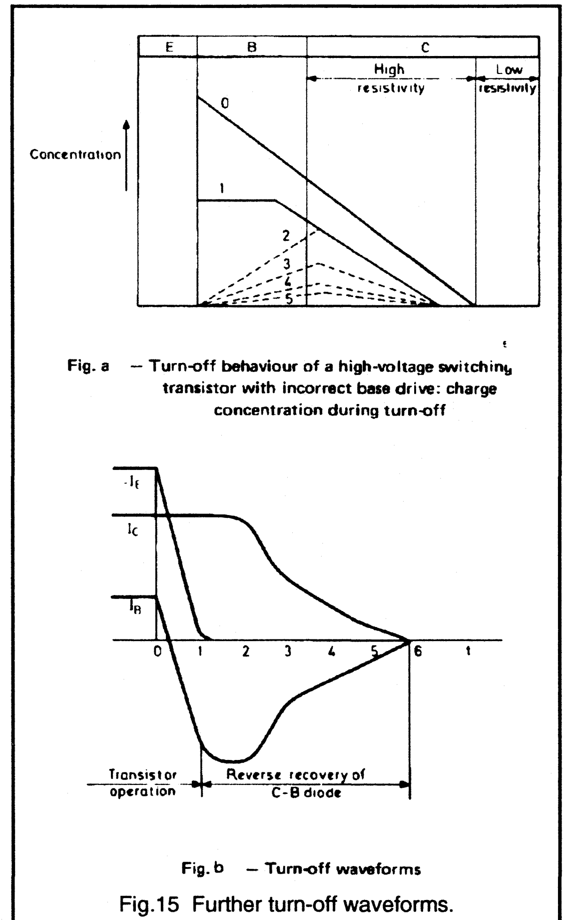


Fig. a — Turn-off behaviour of a high-voltage switching transistor with incorrect base drive: charge concentration during turn-off

Fig. b — Turn-off waveforms

Fig.15 Further turn-off waveforms.

Reference

[1] A 100kHz S.M.P.S using an emitter driven Darlington transistor. Chapter 2.3.3

2.1.4 Isolated power semiconductors for high frequency power supply applications

This section describes a 100 W off-line switcher using the latest component and application technology for cost-effective miniaturisation (see Ref.1). The power supply has a switching frequency of 500kHz with 1MHz output ripple. The section focuses on new power semiconductor components, and in particular the need for good thermal management and electrical isolation are considered. The isolated F-pack, SOT-186 and SOT-199, together with the ISOTOP are introduced. Philips has developed these packages for applications in S.M.P.S. The importance of screening to minimise conducted R.F.I is covered and supported with experimental results.

Introduction

There is an ever-growing interest in high frequency power supplies and examples are now beginning to appear in the market place. The strong motivation for miniaturisation is well founded and a comprehensive range of high frequency components is evolving to meet this important new application area, including:-

The output filter capacitor, which was traditionally an electrolytic type can be replaced by the lower impedance multi-layer ceramic type.

The output filter choke may be reduced in size and complexity to a simple U-core with only a few turns.

The benefits of reduced transformer size can be realised at high frequency by using core materials such as 3F3. However, transformer size is ultimately limited by creepage and clearance distances defined by international safety standards.

Power MOSFETs provide the almost ideal switch, since they are majority carrier devices with very low switching losses. Similarly, Schottky diodes are the best choice for the output rectifiers.

This paper concentrates on the semiconductors and introduces three new encapsulations:- the 'F-packs', SOT-186 and SOT-199 and ISOTOP and applies them to high frequency S.M.P.S.

Power MOSFETs in isolated packages

Making power supplies smaller requires devices such as MOSFETs to be used as the power switch at high frequency. At this high frequency the size and efficiency of the output filter can be dramatically improved. Present abstract perception of acceptable inefficiency in power semiconductors remains constant i.e 5 to 10% overall semiconductor loss at 500kHz is just as acceptable as at 50kHz. So throughout the trend to higher frequencies, the heatsink size has remained constant.

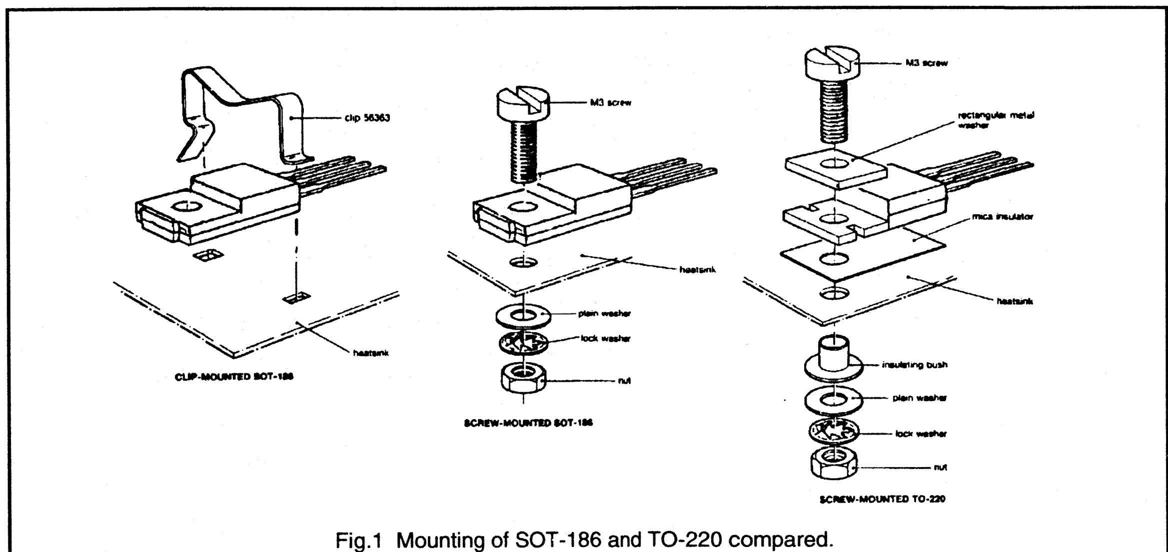


Fig.1 Mounting of SOT-186 and TO-220 compared.

At 50kHz it is possible to use the earthed open frame of the power supply as the heatsink. Then all semiconductors are laid out around the periphery of the p.c.b., and mounted with isolation onto the heatsink. To gain the minimum overall size from high frequency operation, this technique must become standard practice, to avoid having to leave clearance distances between primary and secondary side heatsinks. The component manufacturers are responding to the need for transistors with isolation by making them with a fully isolated package - the F-pack.

F-pack, SOT-186, is an encapsulation with a functionally isolating epoxy layer moulded onto its header, see Fig.1. This allows a common heatsink to be used with no further isolation components. With just a spring clip, an insulated mounting, (up to 1000V), of virtually all existing TO-220 components is possible without degrading performance. Screw mounted, the SOT-186 is still simplicity itself, there is no need for metal spacers, insulation bushes and mica insulators. Mounted either way, the F-pack reduces mounting hardware compared with that required for a standard TO-220.

The insulating layer of a SOT-186 can withstand more than 1000V, but the maximum voltage between adjacent leads is limited to 1000V. This is slightly less than the breakdown voltage between TO-220 legs due to the distance between the legs being reduced from 1.6mm to 1.05mm. However, the 375 µm thick epoxy gives more creepage and clearance between transistor legs and heatsink than a traditional mica washer of 50 µm. The capacitive coupling to an earthed heatsink is therefore reduced from 40pF to 13pF. This can be of significant help with the control of R.F.I.

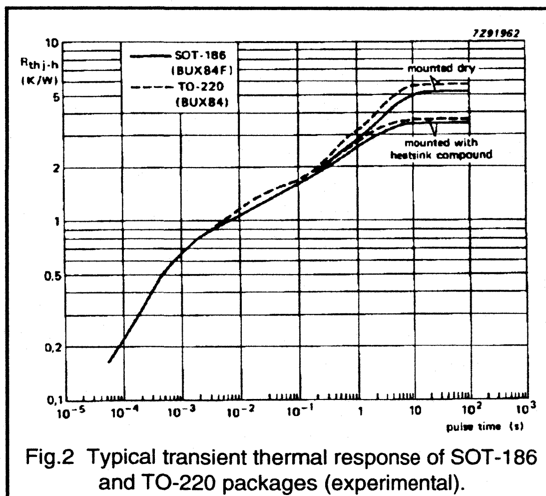


Fig.2 Typical transient thermal response of SOT-186 and TO-220 packages (experimental).

The transient thermal response of the SOT-186 and TO-220 encapsulations is shown in Fig.2. A BUX84F (SOT-186) and a BUX84 (TO-220) were used for the test. Each transistor was mounted on a heatsink at 25˚C. The BUX84 was mounted on a mica washer. The test conditions were given by: Mounting force = 30N; I_E = 1A; V_{CB} = 10V.

The thermal resistance of the F-pack is better than the standard package in free air because it is all black and slightly larger. The difference is quite small, 55K/W for the SOT186 and 70K/W for the TO-220. Mounted on a heatsink, the typical thermal resistance of the SOT-186 is slightly better than the standard TO-220, see Fig.2. However, the exact value of $R_{th(mb\text{-}hs)}$ depends on the following:

- Whether heatsink compound is used.
- The screws torque or pressure on the encapsulation.
- The flatness of the heatsink.

The flatness of the TO-220 metal heatsink is more controllable than the moulded epoxy on the back of the SOT-186. Therefore, the use of a heatsink compound with SOT-186 is of great importance. Once this is done the thermal characteristics of the two approaches are similar.

Schottky diodes in isolated packages

To be consistent with the small, single heatsink approach, the output rectifying diodes must be isolated from the heatsink too. Schottky diodes in SOT-186 are available now, and new encapsulations accommodating larger crystal sizes have been developed for higher powers. An F-pack version of SOT-93 called SOT-199 has therefore been developed. Two Schottky diodes can be mounted in a SOT-199 for lower power outputs up to a maximum of $I_{F(AV)}$ equal to 30 A. The SOT-199 package is similar to, but slightly larger than that shown in Fig.1, and can be mounted similarly.

The epoxy isolation is thicker at 475µm. This further reduces the capacitive coupling to heatsink when compared to a Schottky diode isolated with either 50µm mica or 250µm alumina. Equally important is the increase in the breakdown voltage, from a guaranteed 1000V to 1500V. As with SOT-186, the use of heatsink compound is advised to give good thermal contact.

In applications requiring an $I_{F(AV)}$ rating greater than 30 A, the range of suitable encapsulations has been extended by developing the ISOTOP. This is a mains-isolated encapsulation and will contain diodes which have $I_{F(AV)}$ ratings up to 2 x 80 A.

In conclusion, the combination of isolated packages allows an S.M.P.S to be designed with many devices thermally connected to, but electrically isolated from a single common heatsink.

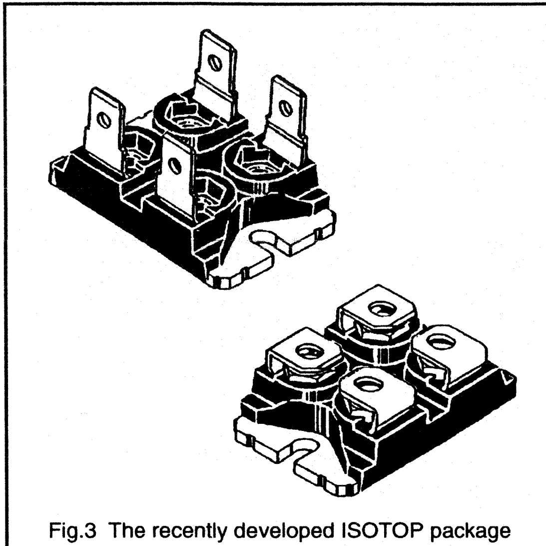


Fig.3 The recently developed ISOTOP package

Transistor characteristics affecting choice of high frequency converter

In this exercise only MOSFETs were considered practical for the target operating frequency of 500kHz. The range of converters to choose from is enormous if all the resonant circuits are included. The choice in this case is reduced by considering only the square wave types because:-

- The p.w.m modulation technique is well understood.
- The main output is easily controlled over a wide range of input voltages and output loads.
- A resonant tank circuit, which may increase size, is not needed.

It is recognised that there are many situations and components which equally affect the choice of converter. The transformer component has been studied in Ref.1. For maximum power through the transformer in a mains input, 500kHz, 100W power supply, a half-bridge converter configuration was chosen. The influence of the transistor is now examined.

The relationship of on-resistance $R_{DS(on)}$, with drain-source breakdown voltage, $V_{(BR)DSS}$, has been examined in Ref.2. It was shown that $R_{DS(on)}$ is proportional to $V_{(BR)DSS}$ raised to the power 2. This implies equal losses for equal total silicon area. The advantage is therefore with the forward / flyback circuits because they have easier drive arrangements and often only require one encapsulation. Particular attention is paid to the frequency dependent losses, which are now considered.

C_{OSS} and the loss during turn-on

No matter how fast the transistor is switched, in an attempt to avoid switching losses, there are always capacitances associated with the structure of the transistor, which will dissipate energy each time the transistor is turned on and off. For a BUK456-800A, 800V MOSFET of 20mm^2 chip size, the turn-off waveform is shown in Fig.4.

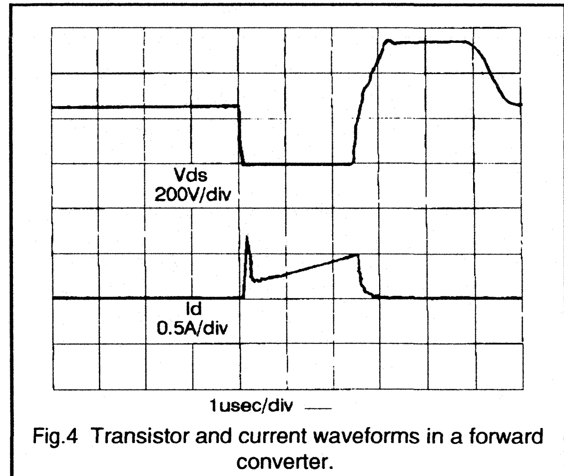


Fig.4 Transistor and current waveforms in a forward converter.

All loads have been reduced to nearly zero to highlight the turn-on current spike due to the capacitance of the circuit. The discharge of the output capacitance of the device will be similar but is unseen to the oscilloscope because it is completely internal to the device. The discharge of the energy is done in two different stages:-

Stage 1 - From the flyback voltage to the D.C link voltage.

This energy is mainly either returned to the supply or clamped in the inductance of the transformer by the secondary diodes, which releases it to supply the load when the primary switch turns on. This energy is not dissipated in the power supply.

Stage 2 - From the link voltage to the on-state voltage.

This energy is dissipated in the transistor when it turns on. The calculation of the effective output capacitance at this voltage involves integration to take into account the varying nature of the capacitance with the applied drain voltage. The general expression for energy stored in the output capacitance of a MOSFET is:-

$$E = 3.3 \; C_{oss(25V)} \; V_d^{1.5}$$

For a BUK456-800A switching on with V_{DS} = 325V, the energy is 1.6 µJ. Gate to drain capacitance is not taken into account but would probably add about 20% extra dissipation to take it to 1.9µJ. This is for a transistor operating in a fixed frequency flyback, forward, or push-pull

converter. A transistor in the half bridge circuit switches on from half the line voltage and so the losses in each transistor would be approximately a quarter of those in the previous converters. In self-oscillating power supplies the transistor switches on from 750 V. This would dissipate all of the stage (1) energy as well and so that could make approximately four times the loss in the transistor in this configuration. This example of a BUK456-800A operating at 500kHz, in a fixed frequency forward, flyback, or push pull system would dissipate 0.95 W internal to the device.

Stray capacitance around the circuit include mounting base to heatsink, which for a ceramic isolator is 18pF. The energy for this is simply calculated by using $0.5\ CV^2$, and is 1µJ when charged to 325 V. F-pack reduces this by about a factor of two.

In conclusion, the fixed frequency half-bridge system benefits from discharging from only half the d.c. link voltage and is the best choice to minimise these effects. There are two switches, so the overall benefit is only half, but the thermal resistance is also half, so the temperature rise of each transistor is actually four times less than in a forward converter. This makes this internal loss at 500kHz, 0.25 W in each transistor.

C_{ISS} and drive circuit losses

It is common to drive MOSFETs from a voltage source, through a series gate resistor. This gate resistor is seen usually to damp stray inductance ringing with the gate capacitance during turn on and off of the transistor. This effectively prevents spurious turn on. The resistor has another function when operating at a frequency of 500kHz, and that is to remove the dissipation of the energy of the gate capacitance from inside to outside the transistor. This is important because at frequencies in the MHz region the dissipation becomes the order of 1 W. A graph of charging the gate with a constant 1mA current source is shown in Fig. 5. The area under the curve was measured as 220µVs.

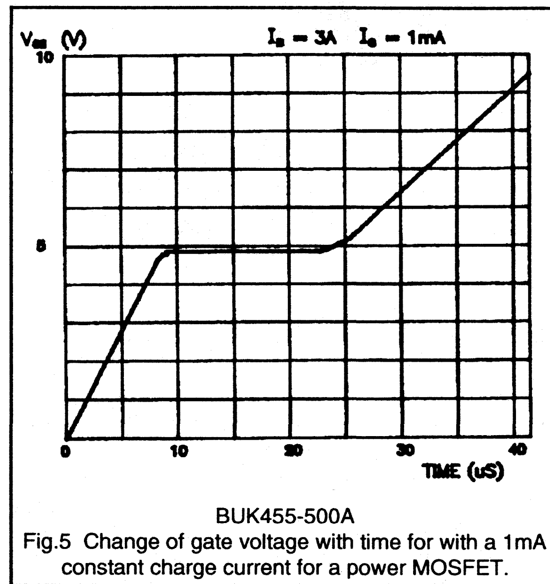
Therefore, at 10kHz, the power dissipation is 2mW and at 10MHz, 2W.

If the system chosen has two transistors, as in the half-bridge, then the dissipation will be doubled. Therefore, a single transistor solution is the most efficient to minimise these losses.

Concluding this section on the significant transistor characteristics, the power loss due to discharging internal MOSFET capacitances is seen to become significant around 500kHz to 1MHz affecting the efficiency of a 100W converter. The predominant loss is output capacitance, which is discharged by, and dissipated in $R_{DS(on)}$. Converters which reduce this loss are those which switch from a lower V_{DS}, i.e.:-

- Resonant converters which switch at zero voltage.
- Converters designed for rectified 110V a.c. mains rather than 250V a.c. mains.
- Square-wave converters which use a half-bridge configuration rather than forward, flyback, or push-pull circuits.

Self oscillating power supplies give higher losses because they discharge from the flyback voltage of 750V at turn-on.



BUK455-500A

Fig.5 Change of gate voltage with time for with a 1mA constant charge current for a power MOSFET.

SMPS design considerations

There are two major areas which influence the choice of converter to be considered here:-

- multiple outputs

- R.F.I

The influence of multiple outputs on the choice of converter.

If only one output is required then the half-bridge push-pull would be selected to minimise the loss due to output capacitance, as described in above.

If multiple outputs are specified, and some of these require rectifying diodes other than Schottky diodes, then the switching loss of power epitaxial diodes has to be considered. On outputs higher than 5V, epitaxial diodes would be a natural first choice. However, a 12V auxiliary output often has less current than a 5V output, so MOSFETs can compete better on forward volt drop. Then there is switching loss; a MOSFET can have less loss than an epitaxial diode, but the actual frequency at which it becomes effective is debatable.

Synchronous MOSFET rectifiers were first seen as a threat to Schottky diodes for use in low voltage outputs. They could rectify with less forward volt drop, albeit sometimes at a cost. MOSFET rectifiers are now more of a threat to epitaxial diodes. Applying these transistors is not as straightforward as it may first appear. Looking at flyback, forward and bridge outputs in turn:-

Flyback converter

A diode rectified output is replaced by a MOSFET, with no extra components added, (Fig.6). Putting the transistor in the negative line and orientating it with the cathode of the parasitic diode connected to the transformer, allows it to be driven well and does not threaten the gate oxide isolation. If the drive is slowed down by the addition of a gate resistor, the voltage across R_{DS} during transient switching can be large enough, such that when added to the output voltage, gives V_{GS} greater than that recommended in data. Fast turn-on is therefore essential for the good health of the transistor.

Forward converter

Normal diode rectifiers are replaced by MOSFETs in a forward output, as shown in Fig.6 with no extra components added. However, there is a problem at maximum input voltage. At minimum volts, the transformer winding supplies $V_{out} + V_{choke}$, where:-

$$V_{out} = V_{choke} = 12V \text{ (for a 12V output)}$$
at 50% mark/space ratio.

$$V_{trans} = 24V$$

At maximum input volts, the choke may have 2 or 3 times the voltage across it, which makes the total 36V or 48V. With the gate rated at 20V, the choke is necessary for the forward transistor, as shown in Fig.6, to supply the correct voltage. It may also be necessary for the flywheel diode, but this may be marginal depending on the input voltage range specified. This costs even more money, but may be considered good value if the loss in an epitaxial diode costs too much in efficiency.

Bridge converters

The circuit shown in Fig.7, at first glance looks attractive. Parasitic diodes are arranged never to come on, and thus do not cause switching losses themselves. Also, the choke voltage drop is less than in the forward case, which may indicate the that MOSFETs can be used without extra overwinds to protect the gate voltage.

However, the simple drive waveforms used here, which are naturally synchronised to the primary switches, do not bias the rectifying transistors on, when both the switches are off. During this time the transformer magnetising currents need a path to freewheel around. Normally this path is provided by the diodes. When the drive has been removed in the circuit example of Fig.7, this path no longer exists. To turn the transistor around so that their body diode can conduct during this freewheel time would only give diode turn-off loss, which is what the technique is intended to avoid. Any bypass diode has the same drawback. The correct drive waveforms are not even available from the choke. They can be generated most easily in conjunction with the primary switch waveforms, but involves expensive isolating drive toroids.

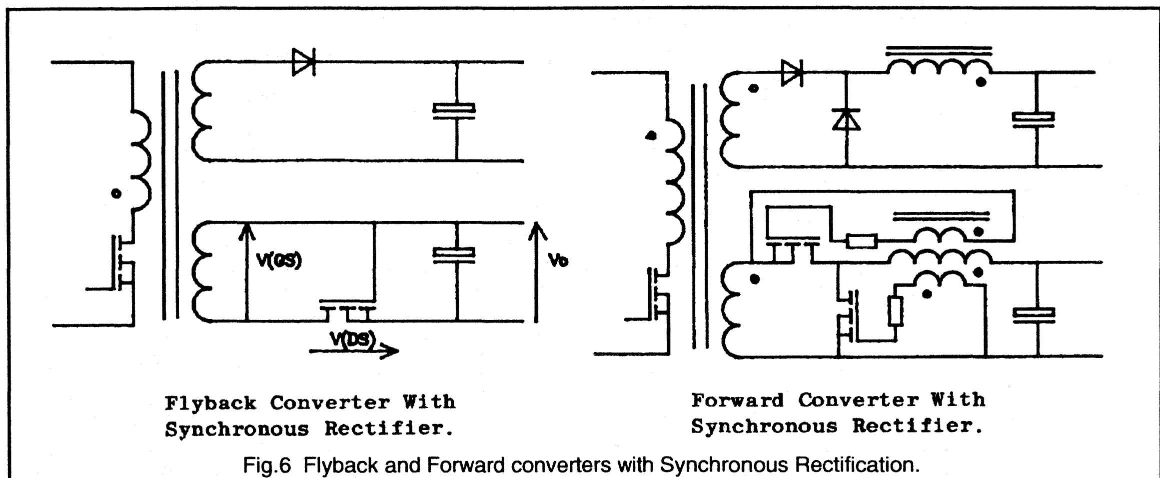


Fig.6 Flyback and Forward converters with Synchronous Rectification.

The conclusions as to which converters are most suitable, and how to connect the MOSFETs in the most cost-effective manner for a 12V output are:-

- A flyback MOSFET rectifier can be connected with no extra components.
- A forward MOSFET needs one overwind, maybe two.
- A bridge output requires drive toroids whose signal is not easily derivable from the secondary side waveforms.

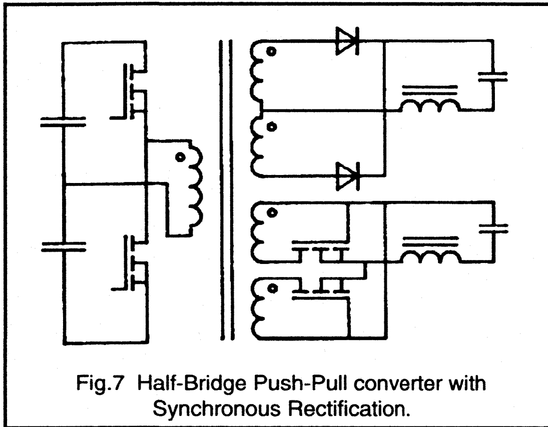


Fig.7 Half-Bridge Push-Pull converter with Synchronous Rectification.

Even though MOSFETs may have less switching loss than epitaxial diodes, they do have capacitance discharged each cycle. The only consolation is that it has a built-in 'anti-snap-off' feature. If the rectifiers are switching at low V_{DS} then this loss is indeed very low.

Influence of R.F.I. on the choice of converter

This section deals with R.F.I. considerations of primary switches and secondary rectifying diodes only. The techniques will be applied to a power supply operating at 500kHz that has been developed to deliver a single 5V output at 15A, from 250V a.c. mains-input. The converter choice is a half bridge push-pull circuit to minimise the loss in the circuit due to C_{OSS}.

A single heatsink arrangement is required to minimise size, so primary and secondary semiconductors need to be thermally cooled on the same heatsink. R.F.I. currents need to be prevented from coupling primary to secondary through the heatsink. Connection of R.F.I. screens underneath all components attached to the metal is not necessary when the structure of the semiconductors is understood.

Taking the rectifiers first:-

The arrangement of the output bridge is shown in Fig.8. The cathodes of the diodes are connected to the substrate within their encapsulation. Thus, as long as the cathodes are connected as close as possible to the ceramic capacitor, C3, of the output filter, the common cathode/capacitor junction is a solid state a.c. earth point. Therefore, no R.F.I. currents are connected into the common heatsink. An isolated encapsulation for an electrical arrangement such as this is all that is needed to minimise R.F.I. from diodes to heatsink. An encapsulation, such as the ISOTOP, which has been developed by Philips, would satisfy this requirement.

Considering next the primary power transistors:-

The arrangement of power transistors is also shown in Fig.8. The drain of the transistors are connected to the substrates of their encapsulations. Thus, as long as TR1 is connected as close as possible to the film-foil bridge capacitors, C1 and C2, the common drain/capacitor junction is a solid a.c. earth point. A SOT-186, SOT-199 or TO-220 with mica washers, may be suitable for TR1, the final selection being dependent on the isolation requirements. For TR2, the drain and therefore the substrate is modulated by the action of the circuit. Thus, without preventive action, R.F.I. currents will be coupled to the heatsink.

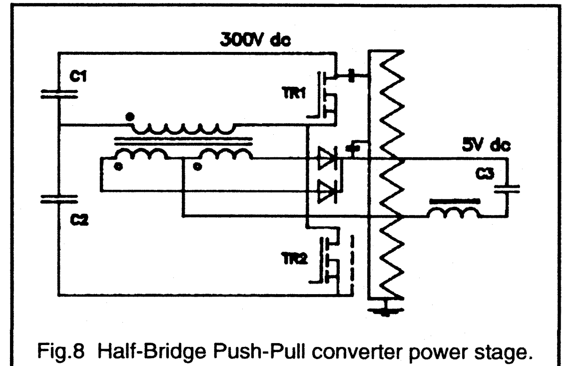


Fig.8 Half-Bridge Push-Pull converter power stage.

The transistor TR2 is in a similar situation to one in a flyback or forward configuration. A simple solution is to use a SOT-186 (F-pack), plus copper screen connected to the transistor source lead and the film-foil capacitor, C2, plus whatever degree of isolation is required to the heatsink. This assembly was tested, and the result was that the screen reduced the line R.F.I. peaks by an average of 10dB over the range 500kHz to 10MHz. A small percentage of this can be attributed to the distance that the copper screen moves the substrate away from the heatsink. Nevertheless, the majority is due to the inclusion of the 0.1mm thick copper screen.

The conclusion is that a variety of encapsulations are necessary to allow R.F.I. to be minimised when the power supply is constructed.

Conclusions

This paper shows how to calculate some of the limiting parameters in the application of semiconductors to high frequency SMPS. It also highlights new encapsulations developed for high frequency power conversion applications. Some of the range of encapsulations were demonstrated in a 500kHz half-bridge push-pull off-line switcher.

References

1. Improved ferrite materials and core outlines for high frequency power supplies. Chapter 2.4.1

2. PowerMOS introduction. Chapter 1.2.1

Output Rectification

2.2.1 Fast recovery epitaxial diodes for use in high frequency rectification.

In the world of switched-mode power supply (S.M.P.S) design, one of the most pronounced advances in recent years has been the implementation of ever increasing switching frequencies. The advantages include improved efficiency and an overall reduction in size, obtained by the shrinking volume of the magnetics and filtering components when operated at higher frequencies.

Developments in switching speeds and efficiency of the active switching power devices such as bipolars, Darlingtons and especially power MOSFETs, have meant that switching frequencies of 100kHz are now typical. Some manufacturers are presently designing p.w.m versions at up to 500kHz, with resonant mode topologies (currently an area of intensive academic research) allowing frequencies of 1MHz and above to be achievable.

These changes have further increased demands on the other fundamental power semiconductor device within the S.M.P.S - the power rectification diode.

Key Rectifier Characteristics.

In the requirements for efficient high frequency S.M.P.S rectification, the diode has to meet the following critical requirements:-

- Short reverse recovery time, t_{rr} ,for compatibility with high frequency use.
- Low forward voltage drop, V_F , to maximise overall converter efficiency.
- Low loss switching characteristics, which reduce the major frequency dependent loss in the diode.
- A soft reverse recovery waveform, with a low dI_R/dt rate, reduces the generation of unwanted R.F.I within the supply.

The Philips range of fast recovery epitaxial diodes (FREDs) have been developed to meet the requirements of high frequency, high power rectification. With many years experience in the development of epitaxial device technology, Philips offer the most comprehensive range of FREDs available. Some of their standard characteristics include:-

- A reverse blocking voltage range from 50V to 800V, and forward current handling capability from 1.7A to 100A. Thus, they are compatible for use in a wide range of S.M.P.S applications, from low voltage dc/dc converters right through to off-line ac/dc supplies. Philips epitaxial diodes are compatible with a range of output voltages from 10V to 200V, with the capability of supplying a large range of output powers. Several different package outlines are also available, offering the engineer flexibility in design.

- Very fast reverse recovery time, t_{rr} , as low as 20ns, coupled with inherent low switching losses permits the diode to be switched at frequencies up to 1MHz.

- Low V_F values, typically 0.8V, produce smaller on-state diode loss and increased S.M.P.S efficiency. This is particularly important for low output voltage requirements.

- Soft recovery is assured with the whole range of FREDs, resulting in minimal R.F.I generation.

Structure of the power diode

All silicon power diodes consist of some type of P-I-N structure, made up of a highly doped P type region on one side, and a highly doped N+ type on the other, both separated by a near intrinsic middle region called the base. The properties of this base region such as width, doping levels and recombination lifetime determine the most important diode characteristics, such as reverse blocking voltage capability, on-state voltage drop V_F, and switching speed, all critical for efficient high frequency rectification.

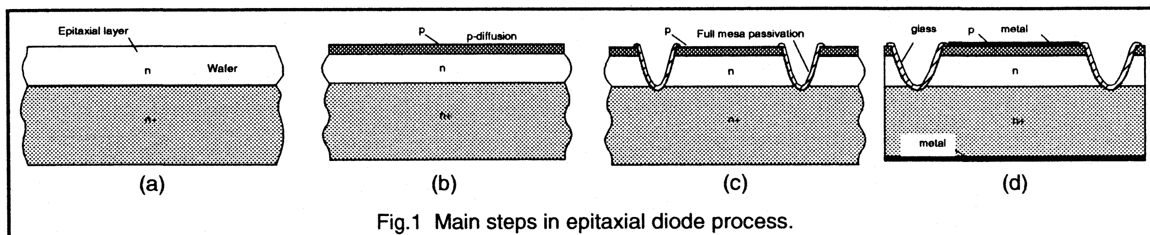


Fig.1 Main steps in epitaxial diode process.

A high blocking voltage requires a wide lightly doped base, whereas a low V_F needs a narrow base. Using a short base recombination lifetime produces faster recovery times, but this also increases V_F. Furthermore, in any P-N junction rectifier operating at high currents, carrier injection into the base takes place from both the P and N+ regions, helping to maintain a low V_F.

Technology

High voltage power diodes are usually manufactured using either double-diffused or an epitaxial technology. High injection efficiency into the base coupled with a narrow base width are essential for achieving a low V_F. High injection efficiency requires the slope of the diffusion profile at the P^+N and N^+N junctions to be very steep. Achieving a minimum base width requires very tight control of the lightly doped base layer. Both these criteria can be met using epitaxial technology.

Epitaxial process.

The epitaxial method involves growing a very lightly doped layer of silicon onto a highly doped N+ type wafer, see Fig.1(a). A very shallow P type diffusion into the epi layer is then made to produce the required P-I-N structure (Fig.1(b)). This gives accurate control of the base thickness such that very narrow widths may be produced. Abrupt junction transitions are also obtained, thus providing for the required high carrier injection efficiency. The tighter control of width and junction profile also provides a tighter control of Q_s, hence, the switching recovery times are typically ten times faster than double diffused types.

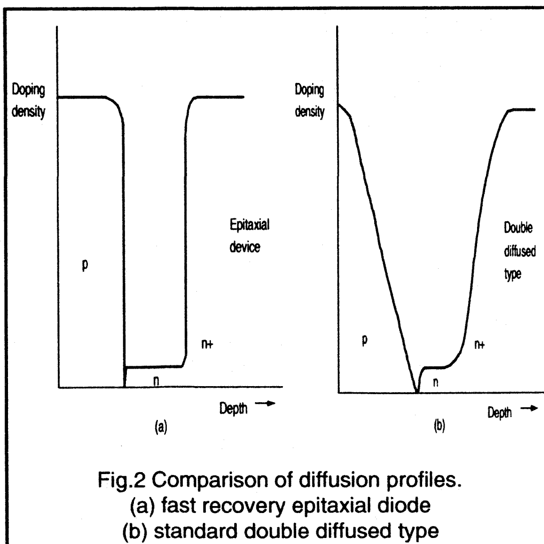


Fig.2 Comparison of diffusion profiles.
(a) fast recovery epitaxial diode
(b) standard double diffused type

Double-diffused process

Double diffusion requires deep diffusions of the P+ and N+ regions into a slice of lightly doped silicon, to produce the required base width. This method is fraught with tolerance problems, resulting in poor control of the base region. The junction transitions are also very gentle, producing a poor carrier injection efficiency. The combination of the two produces a higher V_F value, and also a poor control of stored charge in the base, Q_s, leading to a relatively slow switching speed.

Fig.2 gives a comparison of the diffusion profiles for the two methods.

Lifetime control

To achieve the very fast recovery time and low stored charge, Q_s, required for high frequency rectification it is necessary to introduce lifetime killing (gold doping) into the base of the diode. This produces a lower Q_s and faster reverse recovery time, t_{rr}. Unfortunately, doping also has the effect of increase V_F. Fig.3 shows a graph of normalised V_F versus the minority carrier lifetime for a 200V and 500V device. It can be seen that there is an optimum lifetime for each voltage grade. below which the V_F increases dramatically.

Philips have been using gold-killing techniques for well over twenty years, and combining this with epitaxial technology, results in the excellent low V_F, t_{rr} and Q_s combinations found in the FRED range.

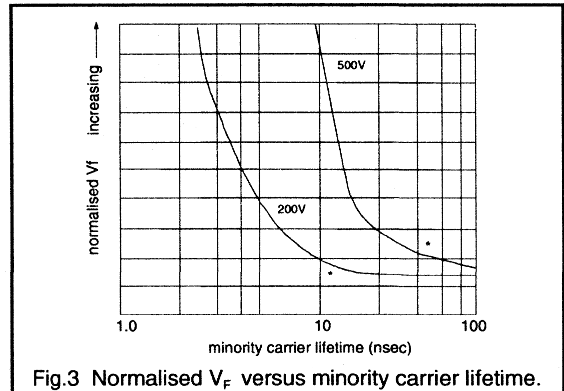


Fig.3 Normalised V_F versus minority carrier lifetime.

Passivation

To ensure that the maximum reverse blocking potential of the diode is achieved, it is necessary to ensure that high fields do not occur around the edges of the chip. This is achieved by etching a trough in the epitaxial layer and depositing a special glass into it (Fig 1(c)). Known as full mesa glass passivation, it achieves stable reverse blocking characteristics at high voltages by reducing charge

build-up, and produces a strong chip edge, reducing the risk of assembly damage. This means that the diodes are rugged and reliable, and also allows all devices to be fully tested on-slice.

Finally, Fig.1(d) shows the chip after it has been diced and metallised. The rectifier is then assembled into a wide selection of different power packages, the standard TO-220 outline being one example.

Characteristics

Forward conduction loss

Forward conduction loss is normally the major component of power loss in the output rectification diodes of an S.M.P.S. For all buck derived output stages, for example the forward converter shown in Fig.4, the choke current always flows in one or other of the output diodes (D1 and D2).

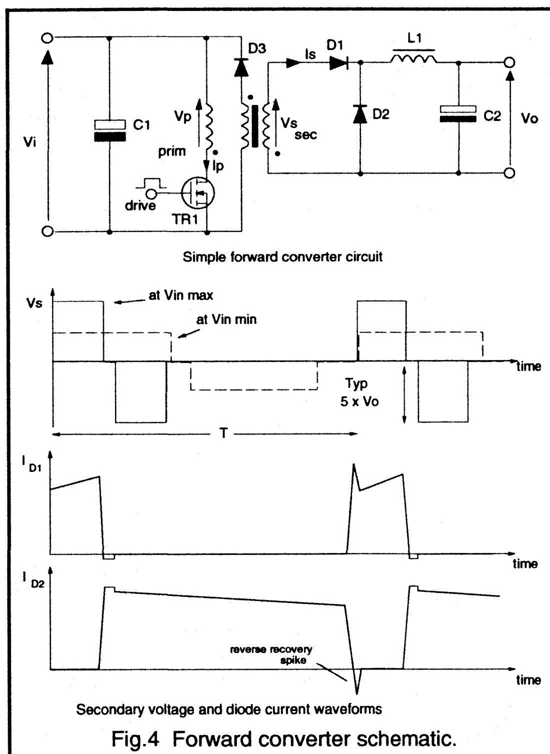


Fig.4 Forward converter schematic.

The output voltage is always lowered by the diode forward voltage drop V_F such that:-

$$V_o + V_f = V_s D \qquad (1)$$

Where D is the transistor duty cycle. Thus, the resulting power loss due to V_F of the output rectifiers is:-

$$P_{on} loss = V_f I_o \qquad (2)$$

where I_o is the output load current of the converter. The loss as a percentage of the output power is thus:-

$$\frac{V_f I_o}{V_o I_o} = \frac{V_f}{V_o} \qquad (3)$$

This loss in efficiency for a range of standard S.M.P.S outputs is shown in Fig.5. It is clear that V_f needs to be kept to an absolute minimum particularly for low output voltages if reasonable efficiency is to be achieved.

To accommodate variations in the input voltage, the output rectifiers are usually chosen such that their blocking voltage capability is between 4 and 8 times the output voltage. For the lowest output voltages, Schottky diodes should be the first choice. Unfortunately, the characteristically low V_f of the Schottky cannot be maintained at voltages much higher than 50V. For outputs above 10V, fast recovery epitaxial diodes are the most suitable rectifiers.

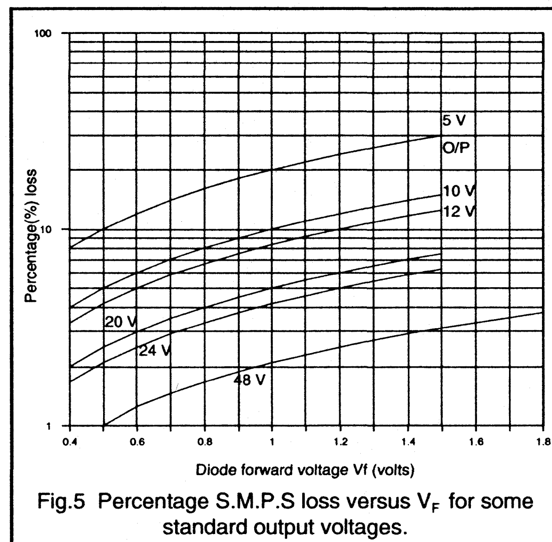


Fig.5 Percentage S.M.P.S loss versus V_F for some standard output voltages.

Fig.6 shows an example of V_F versus forward current I_F, for the Philips BYV32 series, rated from 50V to 200V and with a maximum output current of 20A. This reveals the low V_F values typical of the epitaxial technique.

From Fig.6 and equation 2, it is possible to estimate the loss due to the output rectifiers in an S.M.P.S. For example, for a 12V, 20A output, a conduction loss of 17W typical and 20W maximum is obtained. This corresponds to a worst case loss of 8 % of total output power, normally an acceptable figure.

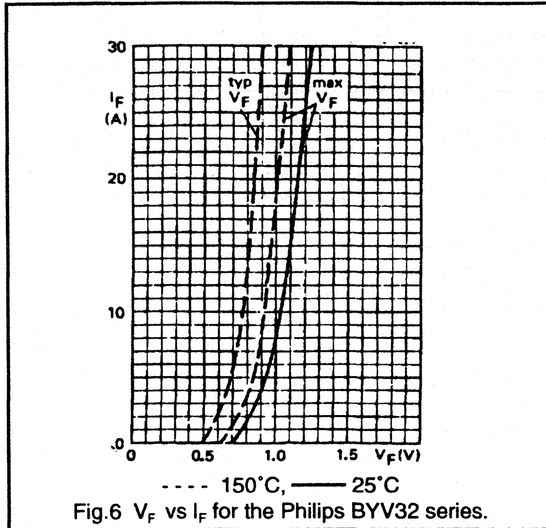


Fig.6 V_F vs I_F for the Philips BYV32 series.

Philips devices offer some of the lowest V_F values on the market. Maximum as well as typical values are always quoted at full rated currents in the datasheets. However this is not the case with all manufacturers, and care should be taken when comparing Philips devices with those of the manufacturers.

Reverse recovery

a) Q_S, t_{rr} and I_{rrm}

Following V_F, the most important feature of a high frequency rectifier is the reverse recovery characteristic. This affects S.M.P.S performance in several ways. These include increased diode switching loss, higher peak turn on current and dissipation in the power transistors, and increased generation of electro-magnetic interference (e.m.i) and voltage transient oscillations in the outputs. Clearly, the rectifier must have optimum reverse recovery characteristics to keep this catalogue of effects to a minimum.

When the P-N diode is conducting forward current, a charge is built up in the base region, consisting of both electrons and holes. It is the presence of this charge which is the key to achieving low V_f. The higher the forward current, the greater is this stored charge. In order to commutate the diode (i.e switch the device from forward conduction into reverse blocking mode) this charge has to be removed from the diode before the base can sustain any reverse blocking voltage. The removal of this charge manifests itself as a substantial transient reverse current spike, which can also generate a reverse voltage overshoot oscillation across the diode.

The waveforms of the reverse recovery for a fast rectifier are shown in Fig.7. The rectifier is switched from its forward conduction at a particular rate, called dI_F/dt. Stored charge begins to be extracted after the current passes through zero, and an excess reverse current flows. At this point the charge is being removed by both the forcing action of the circuit, and recombination within the device (dependent upon the base characteristics and doping levels).

At some point the charge has fallen to a low enough level for a depletion region to be supported across the base, thus allowing the diode to support reverse voltage. The peak of reverse current, I_{rrm} occurs just after this point. The time for the current to pass through zero to its peak reverse value is called t_a. From then on, the rectifier is in blocking mode, and the reverse current then falls back to zero, as the remainder of the stored charge is removed mostly by recombination. The time for the peak reverse current to fall from its maximum to 10% of this value is called t_b.

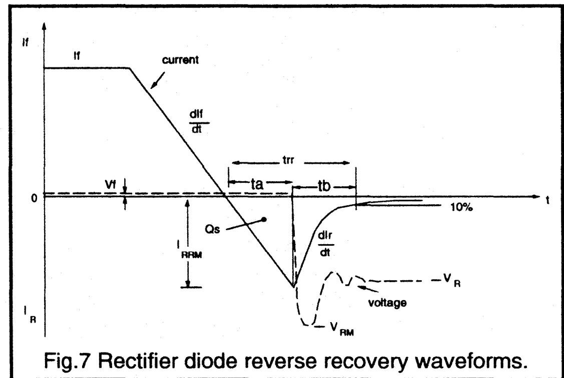


Fig.7 Rectifier diode reverse recovery waveforms.

The stored charge, Q_s,is the area under the current-time curve and is normally quoted in nano-Coulombs. The sum of t_a and t_b is called the rectifier reverse recovery time, t_{rr} and gives a measure of the switching speed of the rectifier.

Factors influencing reverse recovery

In practice, the three major parameters t_{rr}, Q_s and I_{rrm} are all dependent upon the operating condition of the rectifier. This is summarised as follows:-

- Increasing the forward current, I_F, increases t_{rr}, Q_s and I_{rrm}.
- Increasing the dI_F/dt rate by using a faster transistor and reducing stray inductance, significantly decreases t_{rr}, but increases Q_s and I_{rrm}. High dI_F/dt rates occur in the high frequency square wave switching found in S.M.P.S applications. (MOSFETs can produce very small fall times, resulting in very fast dI_F/dt).
- Increasing diode junction temperature, T_j increases all three.
- Reducing the reverse voltage across the diode, V_r , also slightly increases all three.

Specifying reverse recovery

Presently, all manufacturers universally quote the t_{rr} figure as a guide. This figure is obtained using fixed test procedures. There are two standard test methods normally used:-

Method 1

Referring to the waveform of Fig.7:

I_F = 1A; dI_F/dt =50A/µsec; V_r > 30V; T_j= 25˚C.

t_{rr} is measured to 10% of I_{rrm}.

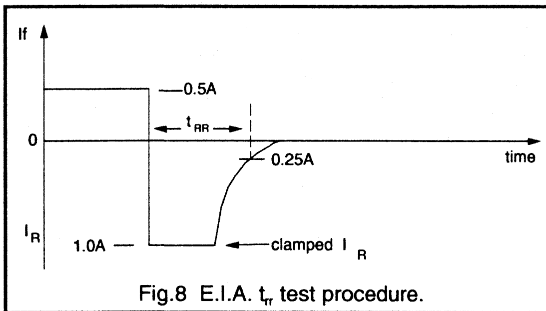


Fig.8 E.I.A. t_{rr} test procedure.

Method 2

I_F = 0.5A, the reverse current is clamped to 1A and t_{rr} is measured to 0.25A.

This is the Electronics Industries Association (E.I.A) test procedure, and is outlined in Fig.8.

The first and more stringent test is the one used by Philips. The second method, used by the majority of competitors will give a t_{rr} figure typically 30% lower than the first, i.e. will make the devices look faster. Even so, Philips have the best t_{rr} / Q_s devices available on the market. For example, the Philips BYW29 200V, 8A device has a t_{rr} of 25ns, the competitor devices quote 35ns using the easier second test. This figure would be even higher using test method 1.

Reverse recovery is specified in data by Philips in terms of all three parameters t_{rr}, Q_s and I_{rrm}. Each of these parameters however is dependent on exact circuit conditions. A set of characteristics is therefore provided showing how each varies as a function of dI_f/dt, forward current and temperature, Fig. 9. These curves enable engineers to realise what the precise reverse recovery performance will be under circuit operating conditions. This performance will normally be worse than indicated by the quoted figures, which generally speaking do not reflect circuit conditions. For example, a BYW29 is quoted as having a t_{rr} of 25 ns but from the curves it may be as high as 90 ns when operated at full current and high dI_F/dt. Similarly a quoted Q_s of 11 nC compares with the full current worst case of 170 nC.

In the higher voltage devices (500V and 800V types) t_{rr} and Q_s are much higher, and will probably be the most critical parameters in the rectification process. Care must be taken to ensure that actual operating conditions are used when estimating more realistic values.

Frequency range

Fig.10 compares the recovery of a Philips 200V FRED with a double diffused type. The FRED may be switched approximately 10 times faster than the double diffused type. This allows frequencies of up to 1MHz to be achieved with the 200V range.

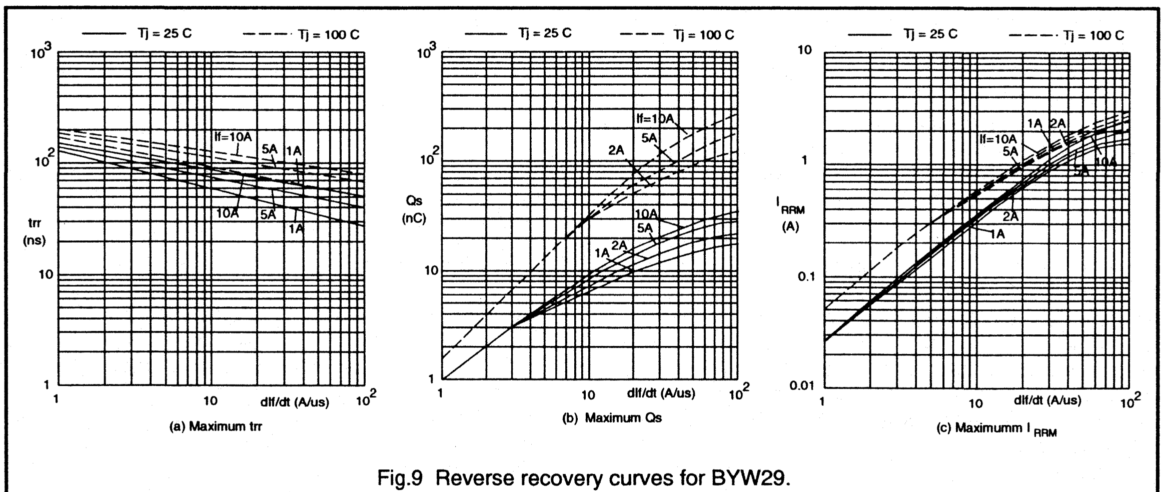


Fig.9 Reverse recovery curves for BYW29.

In the higher voltage devices where the base width is increased to sustain the reverse voltage, the amount of stored charge increases, as does the t_{rr}. For a 500V device, 500kHz operation is possible, and for 800V typically 200kHz is realistic.

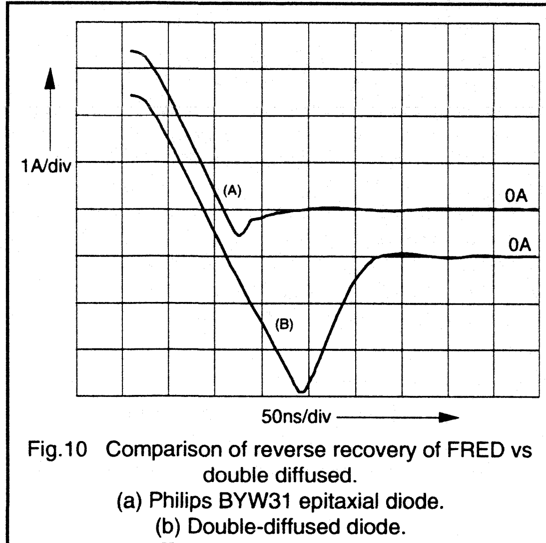


Fig.10 Comparison of reverse recovery of FRED vs double diffused.
(a) Philips BYW31 epitaxial diode.
(b) Double-diffused diode.

Effects on S.M.P.S operation

In order to analyse the effects of reverse recovery on the power supply, a simple non-isolated buck converter shown in Fig.11 is considered. The rectifier in this application, D1 is used in a freewheel mode, and conducts forward current during the transistor off-time.

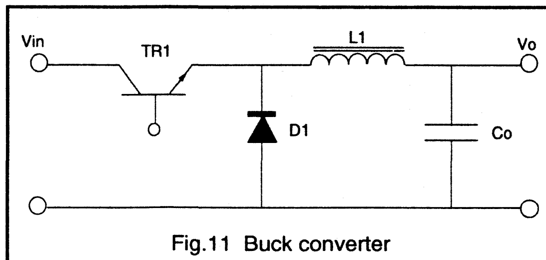


Fig.11 Buck converter

The waveforms for the diode and transistor switch during the reverse recovery of the diode, when the transistor turns on again are given in Fig.12.

As the transistor turns on, the current ramps up in the transistor as it decays and reverses in the diode. The dI_F/dt is mainly dependent on the transistor fall time, and to some extent the circuit parasitic inductances. During the period t_a the diode has no blocking capability and therefore the transistor must support the supply voltage. The transistor thus simultaneously supports a high voltage and conducts both the load current and the reverse recovery current implying a high internal power dissipation. After time t_a the diode blocking capability is restored and the voltage across the transistor begins to fall. It is clear that a diode with an I_{rrm} half the value of I_F will effectively double the peak power dissipation in the transistor at turn on. In severe cases where a high I_{rrm} / t_{rr} rectifier is used, transistor failure could occur by exceeding the peak current or power dissipation rating of the device.

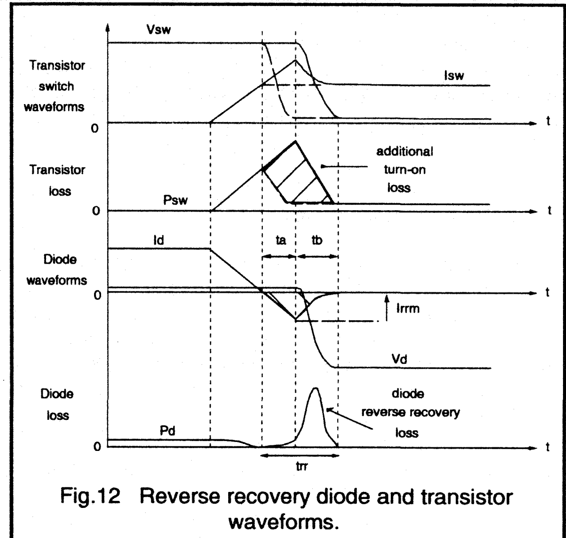


Fig.12 Reverse recovery diode and transistor waveforms.

There is also an additional loss in the diode to be considered. This is a product of the peak I_{rrm} and the diode reverse voltage, V_r. The duration of current recovery to zero will effect the magnitude of the diode loss. However in most cases the additional transistor loss is much greater than the diode loss.

Diode loss calculation

As an example of the typical loss in the diode, consider the BYW29, 8A, 200V device as the buck freewheel diode, for the following conditions:-

I_F = 8A; V_r =100V; dI_F/dt = 50A/µs;
T_j = 25˚C; duty ratio D = 0.5; f = 100KHz

The diode reverse recovery loss is given by:-

$$P_{rr} = \frac{1}{2} \cdot V_r \cdot I_{rrm} \cdot t_b \cdot f$$

From the curves of Fig.7 t_{rr}=35ns, I_{rrm} = 1.5A. Assuming t_b = t_{rr}/2 gives:

$$P_{rr} = \frac{1}{2} \cdot 100 \cdot 1.5 \cdot 17.5 \cdot 100\mathrm{k} = 132\mathrm{mW}$$

This is still small compared to the diode V_F conduction loss of approximately 3.6 W. However, at T_j=100˚C, dI_F/dt=100A/µs and f=200kHz, the loss becomes 1.05W, which is fairly significant. In the higher voltage devices where t_{rr} and I_{rrm} are significantly worse, then the frequency dependent switching loss will tend to dominate, and can be higher than the conduction loss. This will limit the upper frequency of operation of the diode.

The turn on current spike generated in the primary circuits due to diode reverse recovery can also seriously effect the control of the S.M.P.S when current mode control is used (where the peak current is sensed). An RC snubber is usually required to remove the spike from the sense inputs. Good reverse recovery removes the need for these additional components.

b) Softness and dI_R/dt

When considering the reverse recovery characteristics, it is not just the magnitude (t_{rr} and I_{rrm}) which is important, but also the shape of the recovery waveform. The rate at which the peak reverse current, I_{rrm} falls to zero during time, t_b is also important. The maximum rate of this slope is called dI_R/dt and is especially significant. If this slope is very fast, it will generate significant radiated and conducted electrical noise in the supply, causing R.F.I problems. It will also generate high transient voltages across circuit inductances in series with the diode, which in severe cases may cause damage to the diode or the transistor switch by exceeding breakdown limits.

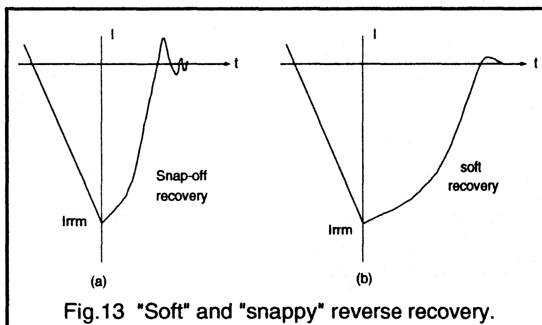


Fig.13 "Soft" and "snappy" reverse recovery.

A diode which exhibits an extremely fast dI_R/dt is said to have a "snap-off" or"abrupt" recovery, and one which returns at a relatively smooth, gentle rate to zero is said to have a soft recovery. These two cases are shown in the waveforms in Fig.13. The softness is dependent upon whether there is enough charge left in the base, after the full spread of the depletion region in blocking mode, to allow the current to return to zero smoothly. It is mainly by the recombination mechanism that this remaining charge is removed during t_b.

Maintaining t_b at a minimum would obviously give some reduction to the diode internal loss. However a snappy rectifier will produce far more R.F.I and transient voltages. The power saving must therefore be weighed against the additional cost of the snubbers and filtering which would otherwise be required if the rectifier had a snappy characteristic.

The frequency range of R.F.I generated by dI_R/dt typically lies in the range of 1MHz to 30MHz, the magnitude being dependent upon how abrupt the device is. One secondary effect that is rarely mentioned, is the additional transformer losses that will occur due to the extremely high frequencies generated inside it by the diode recovery waveform. For example, core loss at 10MHz for a material designed to operate at 100kHz can be significant. There will also be additional high frequency loss in the windings due to the skin effect. In this case the use of a soft device which generates a lower frequency noise range, will reduce these losses.

Characterising softness

A method currently used by some manufacturers to characterise the softness of a device is called the softness factor, S. This is defined as the ratio of t_b over t_a.

$$softness factor, \quad S = \frac{t_b}{t_a}$$

An abrupt device would have S much less than 1, and a soft device would have S greater than 1. A compromise between R.F.I and diode loss is usually required, and a softness factor equal to 1 would be the most suitable value for a fast epitaxial diode.

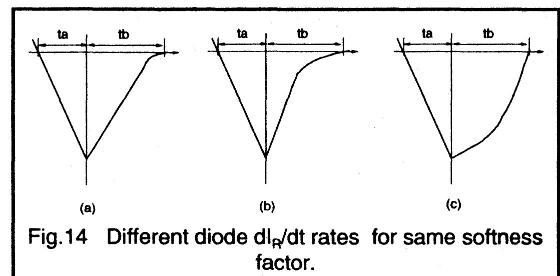


Fig.14 Different diode dI_R/dt rates for same softness factor.

Although the softness factor does give a rough guide to the type of recovery and helps in the calculation of the diode switching loss, it does not give the designer any real idea as to the dI_R/dt that the rectifier will produce. Hence levels of R.F.I and overvoltages could be different for devices with the same softness factor. This is shown in Fig.14, the three characteristics have the same softness factor, but completely different dI_R/dt rates.

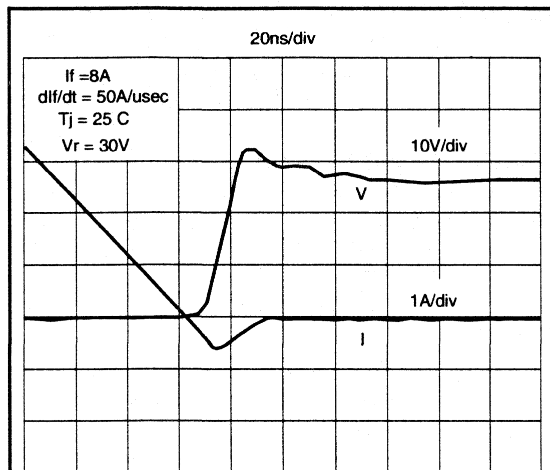
In practice a suitable level for dI_R/dt would be to have it very similar in magnitude to dI_F/dt. This would keep the noise generated to a minimum.

At present there is no universal procedure used by manufactures to characterise softness, and so any figures quoted must be viewed closely to check the conditions of the test.

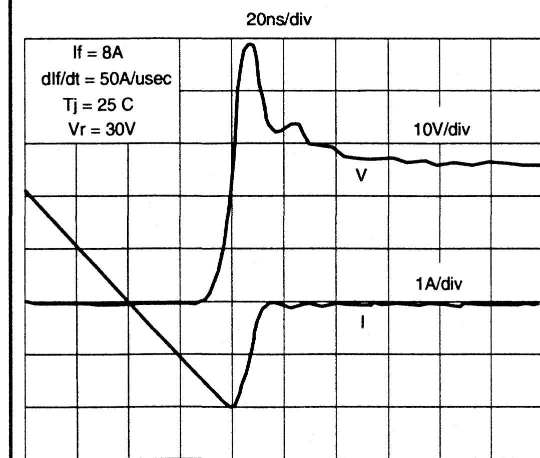
Comparison with competitor devices

Fig.15 compares a BYV32 with an equivalent competitor device. This test was carried out using an L.E.M Q_s test unit.

The conditions for each diode were identical. The results were as follows:-



(a)



(b)

Fig.15 Comparison of softness of reverse recovery.
(a) Philips BYV32 200V 8A device
(b) Equivalent competitor device

BYV32:- $S = 1.2$, $dI_R/dt = 40A/\mu s$, Voltage overshoot = 5V

Competitor:- $S = 0.34$, $dI_R/dt = 200A/\mu s$, Voltage overshoot = 22V

The Philips device was far superior. Apart from the very low Q_s and I_{rrm} values obtained, the S factor was near 1 and the dI_R/dt rate was less than the original dI_F/dt of $50A/\mu s$. These excellent parameters produce minimal noise and the very small overshoot voltage shown. The competitor device was much snappier, the dI_R/dt was 4 times the original dI_F/dt, and caused a much more severe overshoot voltage with the associated greater R.F.I. The diode loss is also higher in the competitor device even though it is more abrupt, since Q_s and I_{rrm} are larger.

The low Q_s of the Philips FRED range thus maintains diode loss to a minimum while providing very soft recovery. This means using a Philips type will significantly reduce R.F.I. and dangerous voltage transients, and in many cases reduce the power supply component count by removing the need for diode snubbers.

Forward recovery

A further diode characteristic which can effect S.M.P.S operation is called the forward recovery. Although, this is not normally as important as the reverse recovery effects in rectification, it can be particularly critical in some special applications.

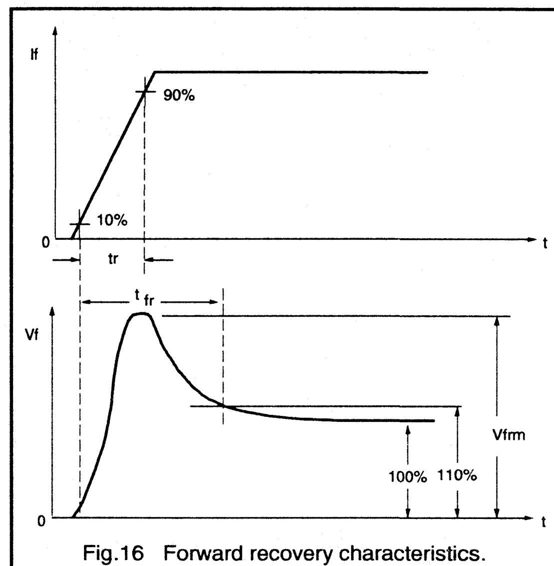


Fig.16 Forward recovery characteristics.

Forward recovery is caused by the lack of minority carriers in the rectifier p-n junction during diode turn on. At the instant a forward bias is applied, there are no carriers present at the junction. This means that at the start of conduction, the diode impedance is high, and an initial forward voltage overshoot will occur. As the current flows and charge builds up, conductivity modulation (minority carrier injection) takes place. The impedance of the rectifier falls and hence, the forward voltage drop falls rapidly back to the steady state value.

The peak value of the forward voltage is known as the forward recovery voltage, V_{frm}. The time from the forward current reaching 10% of the steady state value, to the time the forward voltage falls to within 10% of the final steady state value is known as the forward recovery time (Fig.16).

The magnitude and duration of the forward recovery is normally dependent upon the device and the way it is commutated in the circuit. High voltage devices will produce larger V_{frm} values, since the base width and resistivity (impedance) is greater.

The main operating conditions which affect V_{fr} are:-

- I_f; high forward currents, which produces higher V_{fr}.
- Current rise time, t_r ; a fast rise time produces higher V_{fr}.

Effects on s.m.p.s.

The rate of rise in forward current in the diode is normally controlled by the switching speed of the power transistor. When the transistor is turned off, the voltage across it rises, and the reverse voltage bias across the associated rectifier falls. Once the diode becomes forward biased there is a delay before conduction is observed. During this time, the transistor voltage overshoots the d.c supply voltage, while it is still conducting a high current. This can result in the failure of the transistor in extreme cases if the voltage rating is exceeded. If not, it will simply add to the transistor and diode dissipation. Waveforms showing this effect are given in Fig.17.

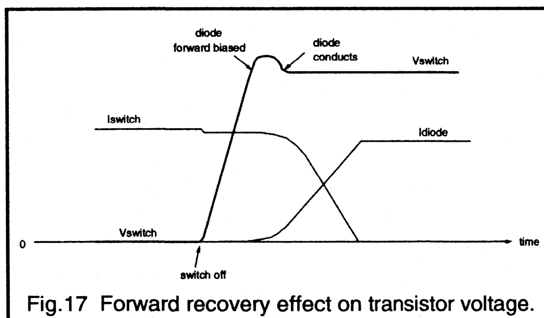


Fig.17 Forward recovery effect on transistor voltage.

Table.1 outlines typical V_{frm} values specified for rectifiers of different voltage rating. This shows the relatively low values obtained. No comparable data for any of the competitor devices could be found in their datasheets. It should be noted that in most S.M.P.S rectifier applications, forward recovery can be considered the least important factor in the selection of the rectifier.

Device type	V_{BR} (Volts)	I_f (Amps)	dI_f/dt (A/µs)	typ V_{frm} (Volts)
BYW29	200	1.0	10	0.9
BYV29	500	10	10	2.5
BYR29	800	10	10	5.0

Table.1 V_{frm} values for different Philips devices.

Reverse leakage current

When a P-N junction is reversed biased, there is always an inherent reverse leakage current that flows. In any piece of undoped semiconductor material there is a thermally generated background level of electron and hole pairs. These pairs also naturally recombine, such that an equilibrium is established. In a p-n junction under reverse voltage conditions, the electric field generated will sweep some of the free carriers generated out of the device before they can recombine, hence, causing a leakage current. This phenomena is shown in Fig. 18.

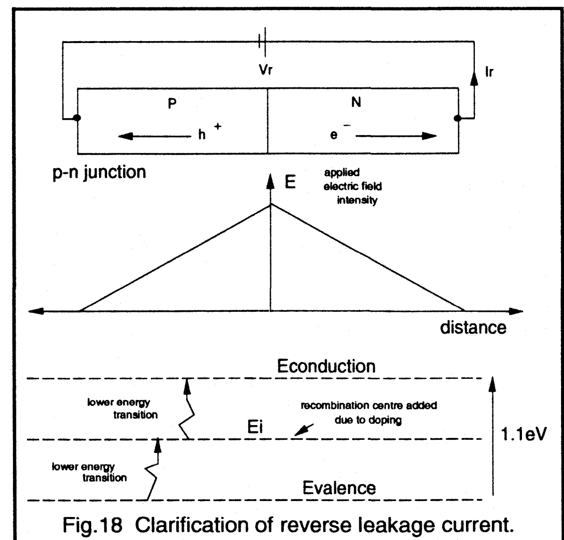


Fig.18 Clarification of reverse leakage current.

When the rectifier base is gold doped to decrease Q_s and t_{rr}, a new energy level is introduced, very close to the centre of the semiconductor energy band gap. This provides lower energy transition paths as shown, and thermal generation

(and recombination) of hole-electron pairs is more frequent. Thus, the reverse leakage current is greater still in the killed, fast rectifier.

Since the pairs are generated thermally, it is obvious that raising the junction temperature will increase the leakage significantly. For example, the leakage current of a FRED can increase by up to 20 times by raising the junction temperature, T_j from 25˚C to 100˚C. This increase can be far greater in other diode technologies.

Many S.M.P.S designers have a misconception about leakage current, and believe that it renders the rectifier poor quality, giving high losses, and is unreliable. This is not so. Leakage is a naturally occurring effect, and is present in all rectifiers. The leakage in an S.M.P.S diode is normally extremely small and stable, with very little effect on the rectification process. Some manufacturers have over-emphasised the benefits of very low leakage devices, claiming that they have great advantages. However, this will be shown to be groundless, since any reduction in the overall diode power loss will be minimal.

In practice, the reverse leakage current only becomes significant at high operating temperatures (above 75˚C) and for high reverse blocking voltages (above 500V), where the product of reverse voltage and leakage current (hence, power loss) is higher. Even then, the leakage current is still usually lower than 1mA.

Table.2 lists the maximum leakage currents for some of devices from the Philips range (gold killed), revealing low levels, even in the higher voltage devices, achieved through optimised doping.

Device type	$V_{BR(max)}$ (Volts)	max I_r (mA) T_j =100˚C full V_{rrm}	max I_r (µA) T_j=25˚C full V_{rrm}
BYW29	200	0.6	10
BYV29	500	0.35	10
BYR29	800	0.2	10

Table.2 Maximum reverse leakage currents for Philips devices.

The power dissipation due to leakage is a static loss , and depends on the product of the reverse voltage and the leakage current over a switching cycle. A worst case example is given below where the data sheet leakage current maximum is used at maximum reverse blocking voltage of the diode.

S.M.P.S example:-Flyback converter

Consider first the BYV29-500 as the output rectifier in the discontinuous flyback converter (Note. the reverse blocking occurs during the transistor on time, and a minimum duty of 0.25 has been assumed). The BYV29-500 could generate a possible maximum output voltage of 125V. The maximum leakage power loss is:-

$$P_L = 500\text{V} \cdot 0.35\text{mA} \cdot 0.25 = 43.75\text{mW}$$

Alternatively, for the BYR29-800 maximum rectified output is approximately 200V, and by similar calculations, its maximum loss is 40mW. Lower output voltages would give leakage losses lower than this figure.

These types of calculation can be carried out for other topologies and similar low values are obtained.

Ruggedness

In the harsh environment of the power rectifiers in an S.M.P.S, transient conditions may occur where the maximum reverse blocking voltage of the rectifiers is exceeded. In severe cases this may lead to device failure. These problems can be caused by transient spikes on the mains input supply, switching noise or overvoltage transients generated in the circuit parasitic inductances.

To improve reliability under such severe conditions Philips FREDs, specified with an 'E' suffix in the type number have a guaranteed ruggedness rating. The term ruggedness is used to indicate that the device has been designed to absorb energy during momentary periods of overvoltage. The exact level of ruggedness is quoted in the data sheet in terms of the energy dissipated in the diode from a 20 mH inductance. For example the BYV32E has a 30 mJ rating and the BYV42E a 40 mJ rating. All other characteristics of the rugged devices are the same as those for the standard type.

Conclusion

The Philips range of Fast Recovery Epitaxial Diodes is among the most comprehensive in the industry. The devices have been designed to exhibit the lowest possible V_f while minimising the major reverse recovery parameters, Q_s, t_{rr} and I_{rrm}. Because of the low Q_s switching losses within the circuit are minimised allowing use up to very high frequencies. The soft recovery characteristic engineered into all devices makes them suitable for use in todays applications where low R.F.I. is an important consideration. Soft recovery also provides additional benefits such as reduced high frequency losses in the transformer core and, in some cases, the removal of snubbing components. For those applications where the rectifier may be exposed to dangerous overvoltage transients, improved safety and reliability can be achieved by selecting a component with a guaranteed ruggedness rating.

FRED Selection Guide

Single Diodes

Type Number	Outline	$I_{F(AV)}$ max (A)	Voltage Grades (V)									
			50	100	150	200	300	400	500	600	700	800
BYW29 (E)	TO-220AC	8	*	*	*	*						
BYV29	TO-220AC	9					*	*	*			
BYR29	TO-220AC	8							*	*	*	*
BYV79 (E)	TO-220AC	14	*	*	*	*						
BYW30	DO-4	14	*	*	*	*						
BYT79	TO-220AC	14					*	*	*			
BYV30	DO-4	14					*	*	*			
BYR79	TO-220AC	14							*	*	*	*
BYR30	DO-4	14							*	*	*	
BYW31	DO-4	28	*	*	*	*						
BYV31	DO-4	28					*	*	*			

Dual Diodes (Common cathode)

Type Number	Outline	$I_{F(AV)}$ max (A)	Voltage Grades (V)									
			50	100	150	200	300	400	500	600	700	800
BYV40 (E)	SOT-223	1.5		*	*	*						
BYQ27	SOT-82	10	*	*	*	*						
BYQ28 (E)	TO-220AB	10	*	*	*	*						
BYT28	TO-220AB	10					*	*	*			
BYR28	TO-220AB	10							*	*	*	*
BYV32 (E)	TO-220AB	20	*	*	*	*						
BYV34	TO-220AB	20					*	*	*			
BYR34	TO-220AB	20							*	*	*	*
BYV42 (E)	TO-220AB	30	*	*	*	*						
BYV72 (E)	SOT-93	30	*	*	*	*						
BYV44	TO-220AB	30					*	*	*			
BYV74	SOT-93	30					*	*	*			

Single Diodes (Electrically isolated Package)

Type Number	Outline	$I_{F(AV)}$ max	Voltage Grades (V)									
		(A)	50	100	150	200	300	400	500	600	700	800
BYW29F (E)	SOT-186	8	*	*	*	*						
BYV29F	SOT-186	9					*	*	*			
BYR29F	SOT-186	8							*	*	*	*
BYV74F	S0T-199	14					*	*	*			

Dual Diode (Electrically Isolated Package)

Type Number	Outline	$I_{F(AV)}$ max	Voltage Grades (V)										
		(A)	50	100	150	200	300	400	500	600	700	800	1000
BYQ28F (E)	SOT-186	10	*	*	*	*							
BYV32F (E)	SOT-186	12	*	*	*	*							
BYV72F (E)	SOT-199	20	*	*	*	*							
BYV74F	SOT-199	20					*	*	*				

Twin Diodes (Electrically Isolated Package)

Type Number	Outline	$I_{F(AV)}$ max	Voltage Grades (V)										
		(A)	50	100	150	200	300	400	500	600	700	800	1000
BYT230PI	SOT227A	60				*	*	*		*	*	*	*
BYT230PIV	SOT227B	60				*	*	*		*	*	*	*
BYV54 (E)	SOT227A	100	*	*	*	*							
BYV54V	SOT227B	100											

(E) denotes availablity in a rugged version.

2.2.2 The new range of Schottky diodes from Philips Components

The Schottky diodes from Philips have always had good forward characteristics and excellent switching performance. With this new, more extensive range of Schottky diodes come the additional benefits of stable, low leakage reverse characteristics and unsurpassed levels of guaranteed ruggedness.

The performance improvements have been achieved by changing both the design and the processing of Schottky diode wafers. The changes are the products of the continuing programme of research in the field of Schottky barrier technology being carried out at Stockport.

This report will look at the new range, the improvements that have been made and the changes that have produced them.

New process

The manufacturing process for all the devices in the new range includes several changes which have significantly improved the quality and performance of the product.

Perhaps the most significant change, is moving the production of the Schottky wafers from the bipolar processing facility into the PowerMOS clean room. The Schottky diode is a 'surface' device - its active region is right at the conductor / semiconductor interface, not deep within the silicon crystal lattice. This means that it can usefully exploit the high precision equipments and extremely clean conditions needed to produce MOS transistors. In some respects Schottkies have more in common with MOS transistors than they do with traditional bipolar products. In one respect they are identical - their quality can be dramatically improved by:-

- growing purer oxide layers,
- depositing metal onto cleaner silicon
- more precise control of ion implantation.

Another change has been in the method of producing the Schottky barrier. The original method was to 'evaporate' molybdenum onto the surface of the silicon. In the new process a Pt/Ni layer is 'sputtered' on to the surface and then a heat treatment is used to produce a Pt/Ni silicide. This has the effect of moving the actual conductor / semiconductor interface a small distance away from the surface and into the silicon.

The advantage of this change is that it puts the barrier in an environment where the conditions are more homogeneous, resulting in a more consistent barrier. This consistency produces devices in which every part of the active area has the same reverse characteristic.

An important logistical change has been the introduction of 100mm wafers. This has significantly increased the capacity of the wafer fabrication facilities in Stockport. The effect of this will be to reduce throughput times which means better responsiveness to customers' requirements.

Ruggedness

The RUGGEDNESS of a Schottky diode is a measure of its ability to withstand the surge of power generated by the reverse current which flows through it when the applied reverse voltage exceeds its breakdown voltage. Operation in this mode is, of course, outside the boundaries of normal operation - it always exceeds the V_{RRM} rating of the device. However, situations can arise where the voltages present in the circuit far exceed the expectations of the designer. If devices are damaged by these conditions then the equipment they are in may fail. Such failures often result in equipments being condemned as unreliable. In recognition of this, Philips will now supply devices which operate reliably during both normal and abnormal operation.

All the Schottky diodes supplied by Philips now have two guaranteed reverse surge current ratings:-

I_{RRM} - guarantees that devices can withstand repetitive reverse current pulses ($t_p = 2\mu s$; $\Delta = 0.001$) of greater than the quoted value,

I_{RSM} - guarantees that single, 100µs pulses of the rated value can be applied without damage.

At the moment these ratings are quoted as either 1A or 2A, depending on device size. It should be understood that these figures do not represent the limit of device capability. They do, however, represent the limit of what, experience suggests, might be needed in most abnormal operational situations.

In an attempt to determine the actual ruggedness of the new devices, a series of destructive tests were carried out. The results shown in Fig.1 give the measured reverse ruggedness of different sizes of device. It clearly shows that even small devices easily survive the 1A I_{RRM} / I_{RSM} limit and that the larger devices can withstand reverse currents greater than the 85A that the test gear was designed to deliver.

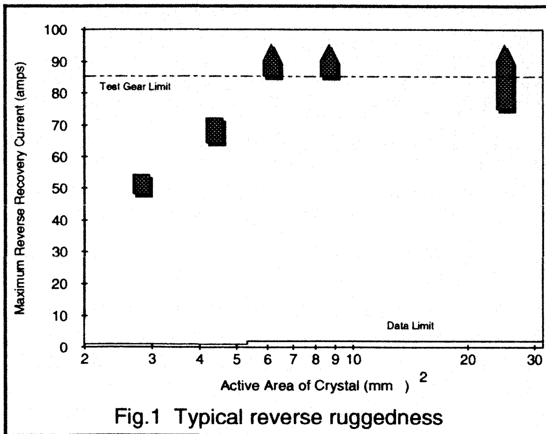


Fig.1 Typical reverse ruggedness

Reverse leakage

The reverse characteristic of any diode depends upon two factors - 'bulk' and 'edge' leakage. The first is the current which leaks through the reverse biased junction in the main active area of the device. The second is the leakage through the junction around its periphery - where the junction meets the outside world. Attention must be paid to both of these factors if a high performance diode is to be produced. During the development of the new range of Philips Schottky diodes both of these factors received particular attention.

Bulk leakage

To achieve low forward voltage drop and very fast switching, Schottky diodes use the rectifying properties of a conductor / semiconductor interface. The 'height' of the potential barrier has a significant effect upon both the forward voltage drop and the reverse leakage. High barriers raise the V_F and lower the general reverse leakage level. Conversely low barrier devices have a lower V_F but higher leakage. So the choice of barrier height must result in the best compromise between leakage and V_F to produce devices with the best all round performance

The height of a Schottky barrier depends, to a large extent, upon the composition of the materials at the interface. So the selection of the barrier metal and the process used for its deposition is very important. The final decision was made with the help of the extensive research and device modeling facilities available within the Philips organisation. The materials and processes that were selected, have significantly reduced the bulk leakage of the new range of Schottky diodes. It is believed that this present design gives the optimum balance between leakage and V_f that is currently achievable.

Edge leakage

The other component influencing the reverse characteristic is edge leakage. In a diffused diode the mechanisms which operate at edge of the active area - where the junction meets the outside world - are different from those which operate in the centre. The Schottky barrier is the same as a diffused junction in this respect. The field at the edge of a simple (untreated in any way) Schottky barrier is very high and as a consequence the leakage through the junction at the periphery can also be very high.

In diffused diodes the edge of the junction is treated by 'passivating' it. In a Schottky diode the edge of the barrier is treated by implanting a shallow, very low dose, p region around the periphery of the active area. This region, called a 'guard ring', effectively replaces the high field periphery of the barrier. It is now the characteristics of the guard ring which determine the edge leakage and not those of the Schottky barrier.

In this way the mechanisms controlling the two elements of leakage are now independent and can be adjusted separately, eliminating the need for compromises. This freedom, and a combination of good design and the close tolerance control - achievable with ion implantation - ensures that the characteristics are excellent, having both good stability and very low leakage.

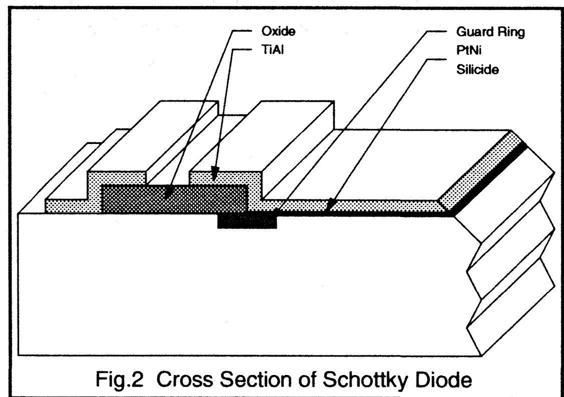


Fig.2 Cross Section of Schottky Diode

Overall leakage

As mentioned earlier good reverse characteristics rely upon both the edge and bulk leakages being good. By eliminating the interactions between the mechanisms and by concentrating on optimising each, it has been possible to improve both edge and bulk leakage characteristics. This has allowed Philips to produce Schottky diodes with typical room temperature, reverse currents as low as 20µA - guaranteed 100µA max. (PBYR645CT) - considerably lower than was ever achieved with molybdenum barrier devices.

Range

The Schottky diode was designed to be used as the rectifier and flywheel diode in the 5V output of high frequency SMPS. These supplies are fitted into equipments whose power requirements vary widely. Satisfying these needs efficiently means that an equally wide range of supplies has to be produced. In recognition of this Philips have produced a range of diode packages with current ratings from 6A to 400A. With this range it is possible to produce power supplies of 20W to 2000W output - higher powers are achievable with parallelling.

The full range of Philips Schottky diodes is shown in Table 1. At the heart of the range are the 'PBYR' devices. The numbers and letters following the PBYR prefix are compatible with industry standards. These figures give an indication of a device's structure (single, twin or dual) and its current and voltage rating. An explanation of the numbers are given in Table 2. Care has been taken to ensure compatibility between Philips devices and those from other suppliers, which share number/letter suffices. It is hoped that this will ease the process of equivalent type selection.

Included in the range are a group of devices with 'BYV1xx' numbers. These devices are a selection of the most popular types from the previous Philips Schottky range. They have proved to be conveniently sized devices which have a mix of ratings and characteristics not matched by other manufacturers. Although these are 'old' numbers, delivered devices will have been manufactured by the new process and will therefore be better. However, changing the production process of established types can often cause concern amongst customers. Philips have recognised this and, during the development, took particular care to ensure that all the new devices would be as closely comparable as possible with previously delivered product. Clarification is given in the cross reference guide given in Table.3.

Summary

This range of Schottky diodes enhances the ability of Philips Components to meet all the requirements needs of the SMPS designer. The well established range of epitaxial diodes, bipolar and PowerMOS transistors, ICs and passive components is now complemented by a range of Schottky diodes with:-

- very low forward voltage drop,
- extremely fast reverse recovery,
- a low leakage reverse characteristics, achieved WITHOUT compromising overall system efficiency
- stable characteristics at both high and low temperatures
- guaranteed ruggedness, giving reliability under both normal and abnormal operating conditions.

Table 1 Range of Schottky Diodes

Single Diode

Type Number	Outline	$I_{F(AV)}$ (A) per diode	$I_{O(AV)}$ (A) per device	Voltage Grades (V)			
				30	35	40	45
PBYR7**	TO220AC	7.5	7.5		*	*	*
PBYR10**	TO220AC	10	10		*	*	*
BYV120**	DO-4	15	15	*	*	*	*
PBYR16**	TO220AC	16	16		*	*	*
BYV121**	DO-4	30	30	*	*	*	*

Dual Diodes - Common Cathode

Type Number	Outline	$I_{F(AV)}$ (A) per diode	$I_{O(AV)}$ (A) per device	Voltage Grades (V)			
				30	35	40	45
PBYR2**CT	SOT223	1	2		*	*	*
PBYR6**CT	SOT82	3	6		*	*	*
BYV118**	TO220AB	5	10		*	*	*
PBYR15**CT	TO220AB	7.5	15		*	*	*
BYV133**	TO220AB	10	20		*	*	*
PBYR20**CT	TO220AB	10	20		*	*	*
BYV143**	TO220AB	15	30		*	*	*
PBYR25**CT	TO220AB	15	30		*	*	*
PBYR30**PT	SOT93	15	30		*	*	*
PBYR300**CT	TO244	150	300		*	*	*
PBYR400**CT	TO244	200	400		*	*	*

Dual Diodes - Common Cathode (Electrically Isolated Package)

Type Number	Outline	$I_{F(AV)}$ (A) per diode	$I_{O(AV)}$ (A) per device	Voltage Grades (V)			
				30	35	40	45
BYV118F**	SOT186 (3 leg)	5	10		*	*	*
PBYR15**CTF	SOT186 (3 leg)	7.5	15		*	*	*
BYV133F**	SOT186 (3 leg)	10	20		*	*	*
PBYR20**CTF	SOT186 (3 leg)	10	20		*	*	*
BYV143F**	SOT186 (3 leg)	15	30		*	*	*
PBYR25**CTF	SOT186 (3 leg)	15	30		*	*	*
PBYR30**PTF	SOT199	15	30		*	*	*

Single Diodes (Electrically Isolated Package)

Type Number	Outline	$I_{F(AV)}$ (A) per diode	$I_{O(AV)}$ (A) per device	Voltage Grades (V)			
				30	35	40	45
PBYR7**F	SOT186 (2 leg)	7.5	7.5		*	*	*
PBYR10**F	SOT186 (2 leg)	10	10		*	*	*
PBYR16**F	SOT186 (2 leg)	16	16		*	*	*

Twin Diodes (Electrically Isolated Package)

Type Number	Outline	$I_{F(AV)}$ (A) per diode	$I_{O(AV)}$ (A) per device	Voltage Grades (V)			
				30	35	40	45
PBYR120**T	SOT227A	60	120		*	*	*
PBYR120**TV	SOT227B	60	120		*	*	*
PBYR160**T	SOT227A	80	160		*	*	*
PBYR160**TV	SOT227B	80	160		*	*	*

Table 2 'PBYR' Types - explanation of the numbering system

The numerical part of the type number gives information about the current and voltage rating of the devices. The final two digits are the voltage grade. The number(s) preceding these, give an indication of the current rating. This figure must be used with care. Single and dual devices derive this number in different ways so the data sheet should be consulted before final selection is made.

Letters after the type number indicate that the device is NOT a single diode package. The codes used by Philips can be interpreted as follows:-

CT - means that the device is a Dual device and the cathodes of the two diodes are connected together.

PT - means the device is a dual with common cathode but for compatibility reasons 'CT' cannot be used.

T - indicates the package will contain two independent diodes with NO shared connections. The package will be ISOTOP with Faston terminals.

TV - means that there will be a two independent diodes in an ISOTOP package fitted with screw terminals

For example

PBYR1645 a device consisting of a single diode with an average current rating ($I_{F(AV)}$)of 16 A and a reverse voltage capability of 45 V.

PBYR30040CT a dual device - two diodes sharing a common cathode connection. The device has a voltage rating of 40 V and an output current ($I_{O(AV)}$) rating of 300 A

Table 3 Cross Reference Guide

Single Diodes

Old Type	Intermediate Type	New Type
BYV19-**	none	PBYR7**
none	none	PBYR10**
BYV39-**	none	PBYR16**
BYV20-**	BYV120-**	none
BYV21-**	BYV121-**	none
BYV22-**	withdrawn	none
BYV23-**	withdrawn	none

Dual Diodes - Common Cathode

Old Type	Intermediate Type	New Type
none	none	PBYR6**CT
BYV18-**	BYV118-**	none
BYV33-**	BYV133-**	PBYR15**CT
none	none	PBYR20**CT
BYV43-**	BYV143-**	PBYR25**CT
BYV73-**	none	PBYR30**PT
none	none	PBYR300*CT
none	none	PBYR400*CT

FULL PACK Dual Diodes - Common Cathode

Old Type	Intermediate Type	New Type
none	BYV118F-**	none
BYV33F-**	BYV133F-**	PBYR15**CTF
none	none	PBYR20**CTF
BYV43F-**	BYV143F-**	PBYR25**CTF

Twin Diodes (Electrically Isolated Package)

Old Type	Intermediate Type	New Type
none	BYV222-**	PBYR120**TV
none	BYV223-**	PBYR160**TV

2.2.3 An Introduction To Synchronous Rectifier Circuits Using PowerMOS Transistors.

Replacing diodes with very low $R_{DS(on)}$ POWERMOS transistors as the output rectifiers in Switch Mode Power Supplies operating at high operating frequencies can lead to significant increases in overall efficiency. However, this is at the expense of the extra circuitry required for transistor drive and protection. In applications where efficiency is of over-riding importance (such as high current outputs below 5V) then synchronous rectification becomes viable.

This paper investigates two methods of driving synchronous rectifiers:-

(i) Using extra transformer windings.

(ii) Self-driven without extra windings.

Multi-output power supplies do not easily lend themselves to extra transformer windings (Although there is usually only one very low output voltage required in each supply). Therefore, the self-driven approach is of more interest. If the additional circuitry and power devices were integrated, an easy to use, highly efficient rectifier could result.

Introduction.

The voltage drop across the output diode rectifiers during forward conduction in an SMPS absorbs a high percentage of the watts lost in the power supply. This is a major problem for low output voltage applications below 5V (See section 2.2.1). The conduction loss of this component can be reduced and hence, overall supply efficiency increased by using very low $R_{DS(on)}$ POWERMOS transistors as synchronous rectifiers (for example, the BUK456-60A).

The cost penalties involved with the additional circuitry required are usually only justified in the area of high frequency, low volume supplies with very low output voltages. The methods used to provide these drive waveforms have been investigated for various circuit configurations, in order to assess the suitability of the POWERMOS as a rectifier.

The main part of the paper describes these circuit configurations which include flyback, forward and push-pull topologies.to control the synchronous rectifiers. To control the synchronous rectifiers they either use extra windings taken from the power transformer or self-driven techniques.

The PowerMOS as a synchronous rectifier.

POWERMOS transistors have become more suitable for low voltage synchronisation for the following reasons:-

(1) The cost of the POWERMOS transistor has fallen sharply in recent years.

(2) Very low $R_{DS(on)}$ versions which yield very low conduction losses have been developed.

(3) The excellent POWERMOS switching characteristics and low gate drive requirements make them ideal for high frequency applications.

(4) Parallelling the POWERMOS devices (which is normally straight forward) will significantly reduce the $R_{DS(on)}$, thus providing further increases in efficiency. This process is not possible with rectifier diodes since they have inherent forward voltage offset levels.

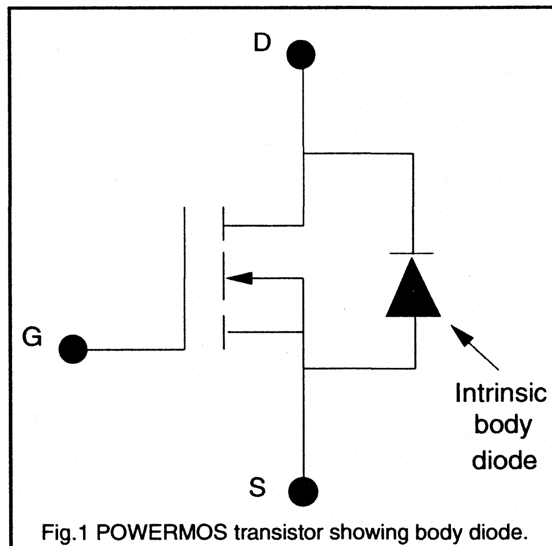


Fig.1 POWERMOS transistor showing body diode.

Design constraints.

When the POWERMOS transistor shown in Fig.1 is used as a synchronous rectifier, the device is configured such that the current flow is opposite to that for normal operation i.e. from source to drain. This is to ensure reverse voltage blocking capability when the transistor is turned off, since there will be no current path through the parasitic body diode. This orientation also gives a degree of safety. If the gate drive is lost, the body diode will then perform the rectification, albeit at a much reduced efficiency.

Unfortunately, this configuration has limitations in the way in which it can be driven. The device gate voltage must always be kept below ± 30V. The on-resistance ($R_{DS(on)}$) of the device must be low enough to ensure that the on-state voltage drop is always lower than the V_f of the POWERMOS intrinsic body diode. The gate drive waveforms have to be

derived from the circuit in such a way as to ensure that the body diode remains off over the full switching period. For some configurations this will be costly since it can involve discrete driver I.C.s and isolation techniques.

If the body diode was to turn-on at any point, it would result in a significant increase in the POWERMOS conduction loss. It would also introduce the reverse recovery characteristic of the body diode, which could seriously degrade switching performance and limit the maximum allowable frequency of operation.

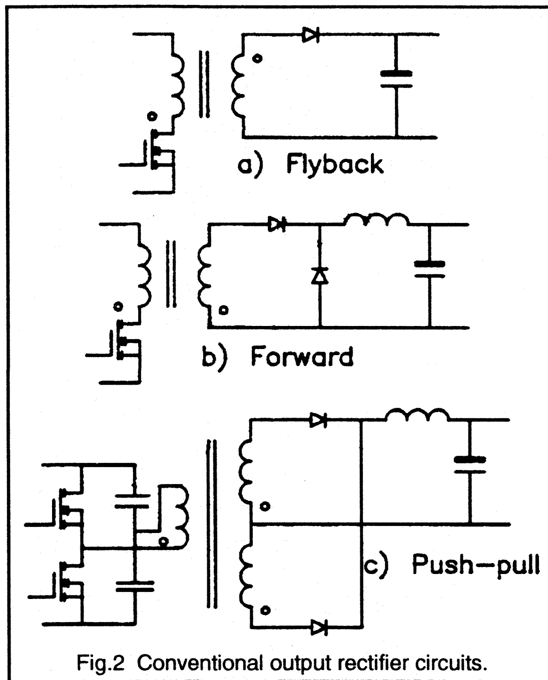


Fig.2 Conventional output rectifier circuits.

It is well known that the $R_{DS(on)}$ of the POWERMOS is temperature dependent and will rise as the device junction temperature increases during operation. This means that the transistor conduction loss will also increase, hence, lowering the rectification efficiency. Therefore, to achieve optimum efficiency with the synchronous rectifier it is important that careful design considerations are taken (for example good heat-sinking) to ensure that the devices will operate at as low a junction temperature as possible.

Transformer Driven Synchronous Rectifiers.

The conventional output rectifier circuits for the flyback, forward and push-pull converters are shown in Fig.2. These diodes can be replaced by POWERMOS transistors which are driven off the transformer as shown in Fig.3. These configurations can be summarised as follows:-

(a) Flyback converter - this is very straight forward; the gate voltage can be maintained at below 30V and the body diode will not come on.

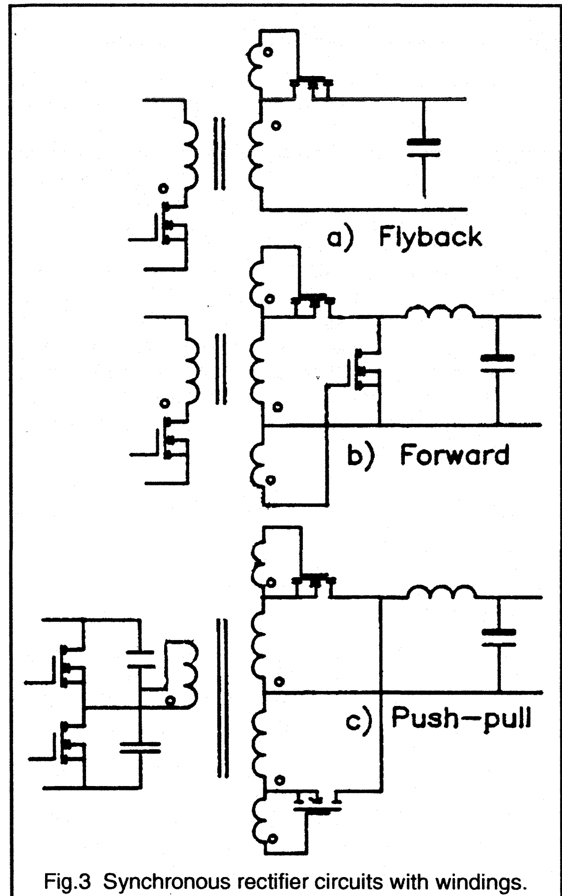


Fig.3 Synchronous rectifier circuits with windings.

(b) Forward converter - the gate drives for the two transistors can be maintained below 30V. However, due to the shape of the transformer waveforms, the freewheel rectifier will not have a square wave signal and the body diode could come on.

(c) Push-pull converter - deriving the gate drives for the two synchronous rectifiers from the transformer means that during the dead time which occurs each switching cycle, both transistors are off. There is nowhere for the circulating current to go and body diodes will come on to conduct this current. This is not permissible because of the slow characteristics of the less than ideal body diode. Therefore, the push-pull configuration cannot be used for synchronous rectification without the costly derivation of complex drive waveforms.

One significant advantage of using this topology is that the r.m.s. current of the rectifiers and hence, overall conduction loss is significantly lower in the push-pull than compared with the forward or flyback versions.

Self-Driven Synchronous Rectifiers.

The disadvantage of the transformer driven POWERMOS is the requirement for extra windings and extra pins on the power transformer. This may cause problems, especially for multi-output supplies. A method of driving the transistors without the extra transformer windings would probably be more practical. For this reason basic self-driven synchronous rectifier circuits were investigated.

It should be noted that the following circuits were based upon an output of 5V at 10A. In practice, applications requiring lower voltages such as 2 or 3 volts at output currents above 20A will benefit to a far greater extent by using synchronous rectification. For these conditions the efficiency gains will be far more significant. However, the 5V output was considered useful as a starting point for an introductory investigation.

(a) The Flyback converter.

An experimental circuit featuring the flyback converter self-oscillating power supply was developed. This was designed to operate at a switching frequency of 40kHz and delivered 50W (5V at 10A).

Directly substituting the single rectifier diode with the POWERMOS transistor as is shown in Fig.4(a) does not work because the gate will always be held on. The gate is Vo above the source so the device will not switch.

Therefore, some additional circuitry is required to perform the switching, and the circuitry used is shown in Fig.4(b). The BUK456-60A POWERMOS transistor which features a typical $R_{DS(on)}$ of 24mΩ (at 25˚C) was used as the synchronous rectifier for these basic configurations.

The drive circuit operates as follows: the pnp transistor switches on the POWERMOS and the npn switches it off. Good control of the POWERMOS transistor is possible and the body diode does not come on. The waveforms obtained are also shown in Fig.4.

If the small bipolar transistors were replaced by small POWERMOS devices, then this drive circuit would be a good candidate for miniaturisation in a Power Integrated Circuit. This could provide good control with low drive power requirements.

Unfortunately, the single rectifier in a flyback converter must conduct a much higher r.m.s. current than the two output diodes of the buck derived versions (for the same output power levels). Since, the conduction loss in a POWERMOS is given by $I_{D(r.m.s)}{}^2.R_{DS(on)}$, it is clear that the flyback, although simple does not lend itself as well to the achieving large increases in efficiency when compared to other topologies that utilise POWERMOS synchronous rectifiers.

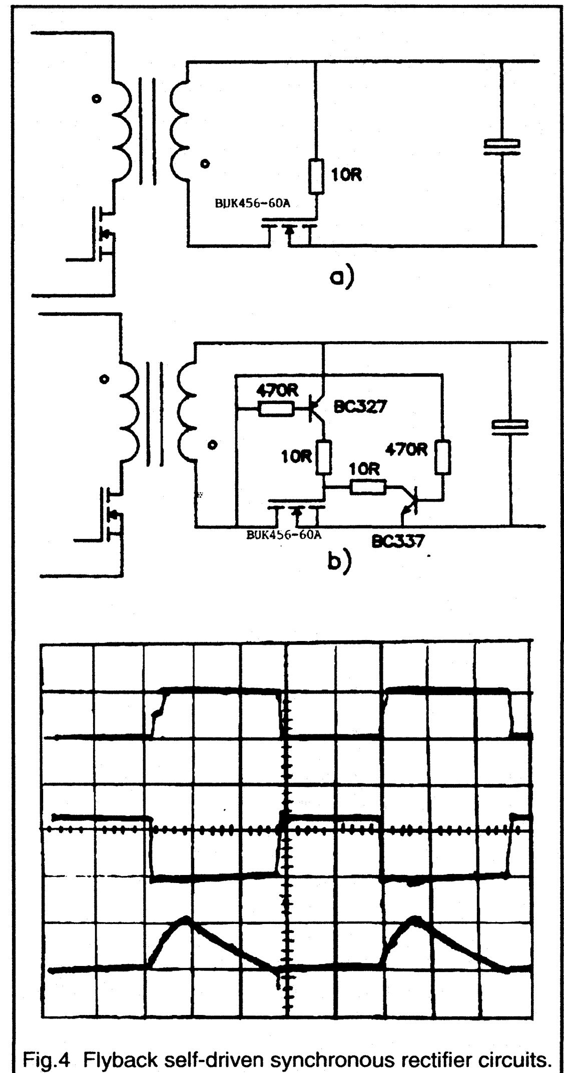
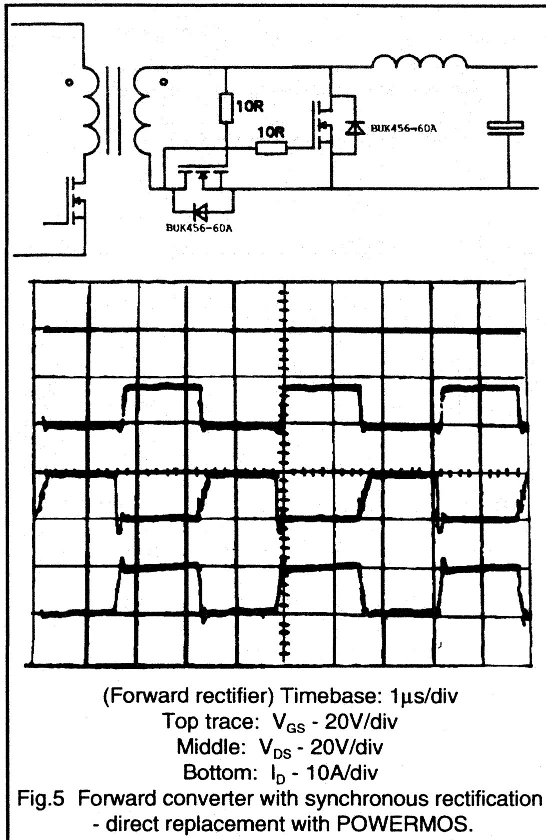


Fig.4 Flyback self-driven synchronous rectifier circuits.

(b) The Forward converter.

An experimental self-driven circuit based on the Forward converter was then investigated. In this version the frequency of operation was raised to 300kHz with the supply again delivering 5V at 10A.

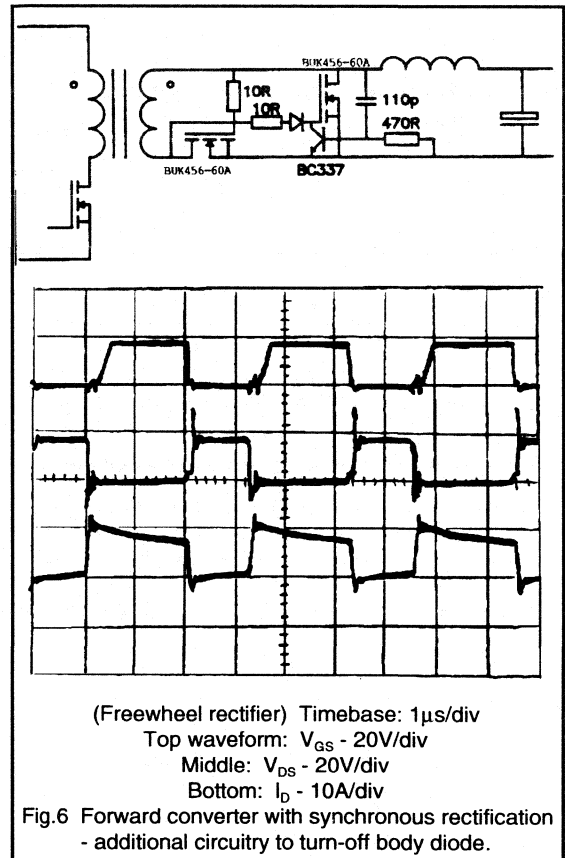


(Forward rectifier) Timebase: 1µs/div
Top trace: V_{GS} - 20V/div
Middle: V_{DS} - 20V/div
Bottom: I_D - 10A/div

Fig.5 Forward converter with synchronous rectification - direct replacement with POWERMOS.

The direct replacement of the output diodes with POWERMOS transistors is shown in Fig.5. In this arrangement, the gate sees the full voltage across the transformer winding. Therefore, the supply input voltage range must be restricted to ensure the gate of the POWERMOS is not driven by excessively high voltages. This would occur during low primary transistor duty cycle conditions. The waveforms obtained for the forward synchronous rectifier this configuration are also shown in Fig.5.

In this case the method of control is such that the gate is referenced to the source via the drain-source body diode. This clamps the gate, enabling it to rise to a voltage which will turn the POWERMOS on. If the body diode was not present, the gate would always remain negative with respect to the source and an additional diode would have to be added to provide the same function.

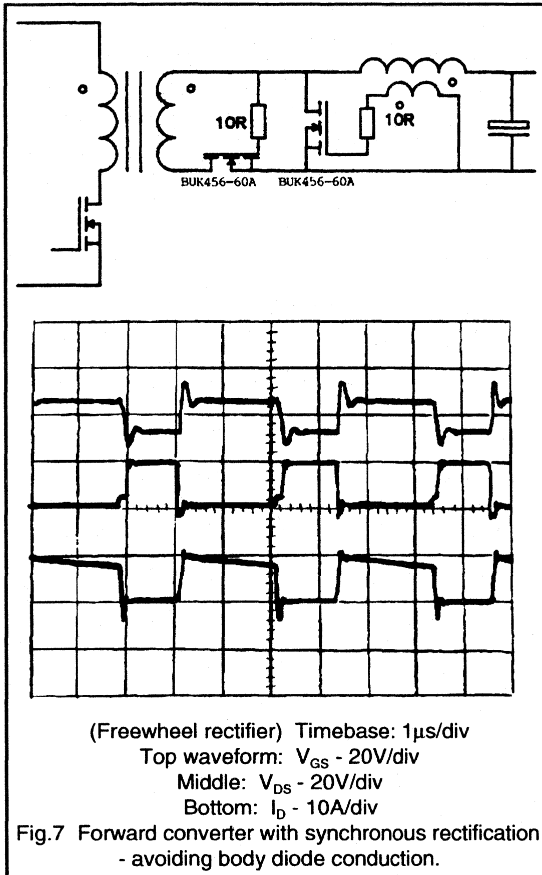


(Freewheel rectifier) Timebase: 1µs/div
Top waveform: V_{GS} - 20V/div
Middle: V_{DS} - 20V/div
Bottom: I_D - 10A/div

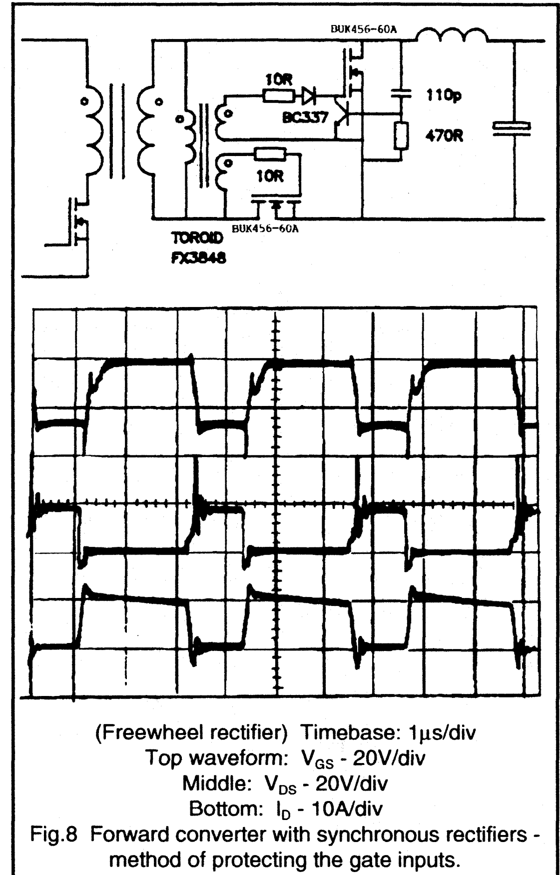
Fig.6 Forward converter with synchronous rectification - additional circuitry to turn-off body diode.

Additional circuitry is required to turn off the freewheel synchronous rectifier. This is due to the fact that the when freewheel POWERMOS conducts, the body diode will take the current first before the gate drive turns the device on. An additional transistor can be used to turn off the POWERMOS in order to keep conduction out of the body diode. This additional transistor will short the gate to ground and ensures the proper turn-off of the POWERMOS. The circuit with this additional circuitry and the resulting freewheel rectifier waveforms are given in Fig.6.

A very simple circuit configuration can used in which body diode conduction in the freewheel synchronous rectifier does not occur. By driving the freewheel rectifier from the output choke via a closely coupled winding, a much faster turn-on can be achieved because the body diode does not come on. This circuit configuration and associated waveforms are shown in Fig.7.



(Freewheel rectifier) Timebase: 1μs/div
Top waveform: V_{GS} - 20V/div
Middle: V_{DS} - 20V/div
Bottom: I_D - 10A/div
Fig.7 Forward converter with synchronous rectification - avoiding body diode conduction.



(Freewheel rectifier) Timebase: 1μs/div
Top waveform: V_{GS} - 20V/div
Middle: V_{DS} - 20V/div
Bottom: I_D - 10A/div
Fig.8 Forward converter with synchronous rectifiers - method of protecting the gate inputs.

To avoid gate over-voltage problems a toroid can been added which will provide the safe drive levels. This toroid effectively simulates extra transformer windings without complicating the main power transformer design. The limitations of this approach are that there will be extra leakage inductance and that an additional wound component is required. The applicable circuit and waveforms for this arrangement are given in Fig.8.

Conclusions

The main advantage of POWERMOS synchronous rectifiers over existing epitaxial and Schottky diodes rectifiers is the increase in efficiency. This is especially true for applications below 5V, since the development of very low $R_{DS(on)}$ POWERMOS transistors allows very significant efficiency increases. It is also very easy to parallel the POWERMOS transistors in order to achieve even greater efficiency levels.

The difficulties involved with generating suitable drives for the POWERMOS synchronous rectifiers tend to restrict the number of circuits for which they are suitable. It will also significantly increase the cost of the supply compared with standard rectifier technology.

The circuit examples outlined in this paper were very basic, however, they did show what can be achieved. The flyback configuration was the simplest, and there were various possibilities for the forward converters.

Recent work has shown that there are topologies more suited to using MOSFET synchronous rectifiers (featuring low rectifier r.m.s. current levels) such as the push-pull. These can achieve overall power supply efficiency levels of up to 90% for outputs of 5V and below. However, the discrete control circuitry required is quite complex and requires optical/magnetic isolation, since the waveforms must be derived from the primary-side control.

The true advantage of synchronous rectifiers may only be reached when the drive circuit and POWERMOS devices are hybridised into Power Integrated Circuits. However, in applications where the efficiency performance is of more importance than the additional costs incurred, then POWERMOS synchronous rectification is presently the most suitable technique to use.

Design Examples

2.3.1 Mains input 100 W forward converter SMPS: MOSFET And Bipolar transistor solutions featuring ETD cores.

The following two switched-mode power supplies described are low cost easy to assemble units, intended primarily for the large number of equipment manufacturers who wish to build power supplies in-house.

The designs are based upon recent technologies and both feature ETD (Economic Transformer Design) ferrite cores. The first design features a high voltage Bipolar transistor, the BUT11 at a switching frequency of 50kHz. The second design is based around a power MOSFET transistor, the BUK456-800A whose superior switching characteristics allow higher switching frequencies to be implemented. In this case 100kHz was selected for the MOSFET version allowing the use of smaller and cheaper magnetic components compared with the lower frequency version.

Both supplies operate from either 110/120 or 220/240 V mains input, and supply 100W of output power to a regulated 5V, 20A with low power auxiliary outputs at ±12V. The PowerMOS solution provides an increase in efficiency of 5% compared to the Bipolar version, and both have been designed to meet stringent R.F.I. specifications.

ETD ferrite cores have round centre poles and constant cross-sectional area, making them ideally suited for the windings required in high-frequency S.M.P.S. converters. The cores are available with clips for rapid assembly, and the coil formers are suitable for direct mounting onto printed circuit boards.

The ETD cores, power transistors and power rectifiers featured are part of a comprehensive range of up-to-date components available from Philips from which cost effective and efficient S.M.P.S designs can be produced.

50kHz Bipolar version

Circuit description

The circuit design which utilises the Bipolar transistor is shown in Fig.1. This is based upon the forward converter topology, which has the advantage that only one power switching transistor is required.

An operating frequency of 50kHz was implemented using a BUT11 transistor (available in TO-220 package or isolated SOT-186 version). This was achieved by optimising the switching performance of the BUT11 Bipolar power transistor TR5, by careful design of the base drive circuitry and by the use of a Baker clamp. The 50kHz operating frequency allows the size and the cost of the transformer and choke to be reduced compared with older Bipolar based systems which worked around 20kHz.

The base drive waveform generated by IC1 is buffered through TR3 and TR4 to the switching transistor TR5. Although operating from a single auxiliary supply line, the drive circuit provides optimum waveforms. At turn-off inductor L3 controls the rate of change of reverse bias current ($-dI_B/dt$). The reverse base-emitter voltage is provided by capacitor C16 (charged during the on-time). The resulting collector current and voltage waveforms are profiled by a snubber network to ensure that the transistor SOAR limits are not exceeded.

Voltage regulation of the 5V output is effected by means of an error signal which is fed back, via the CNX82A opto-coulper, to IC1 which adjusts the transistor duty cycle. Over-current protection of this output is provided by monitoring the voltage developed across the 1Ω resistor, R28 and comparing this with an internal reference in IC1. Voltage regulation and over-current protection for the 12V outputs are provided by the linear regulating integrated circuits IC4 and IC5.

Specification and performance (Bipolar version)

Input

220/240 V a.c. nominal (range 187 to 264 V a.c.)
110/120 V a.c. nominal (range 94 to 132 V a.c.)

Output

Total output power 100 W

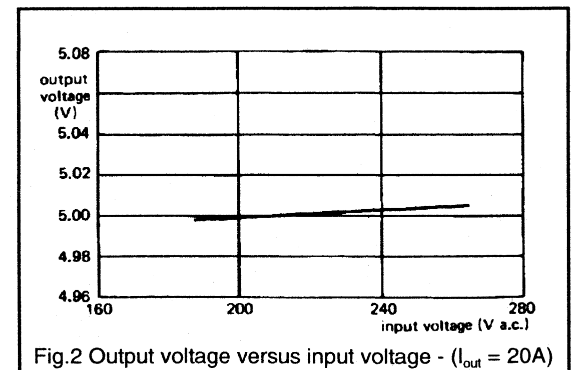


Fig.2 Output voltage versus input voltage - (I_{out} = 20A)

Fig.1 100W SMPS circuit diagram (50kHz Bipolar transistor version)

Main output

5V at 20A max output power - Adjustment range ±5%

Line regulation

The change in output voltage over the full input voltage range of 187 to 264 V is typically 0.2%; see Fig.2

Load regulation

The change in output voltage over the full load range of zero to 100 W is typically 0.4%; see Fig.3.

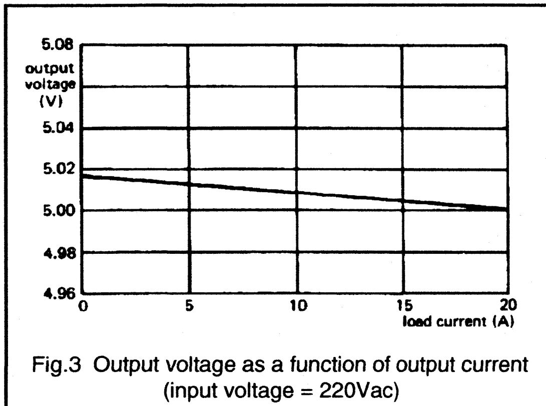


Fig.3 Output voltage as a function of output current (input voltage = 220Vac)

Auxiliary outputs

±12V at 0.1A
Regulation (worst-case condition of max change in input voltage and output load) < 0.4%

Ripple and Noise

0.2% r.m.s. 1.0% pk-pk (d.c. to 100MHz)

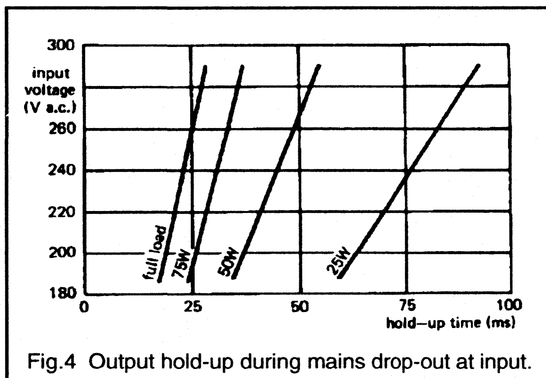


Fig.4 Output hold-up during mains drop-out at input.

Output hold-up

Both the main and auxiliary outputs will remain within specification for a missing half-cycle (18ms) at full load and minimum input voltage; See Fig.4

Isolation

Input to output ground 2kV r.m.s.
Output to ground 500V r.m.s.

Efficiency

The ratio of the d.c output power to the a.c input power is typically 71% at full load; See Fig.5.

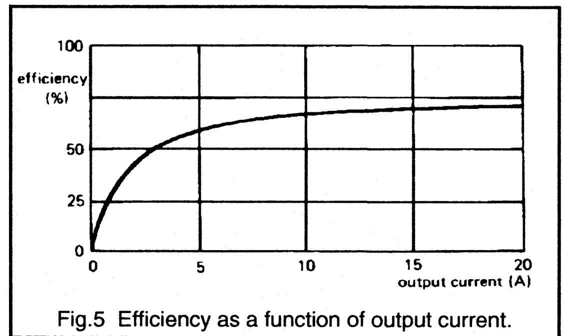


Fig.5 Efficiency as a function of output current.

Radio frequency interference

R.F.I. fed back to the mains meets VDE0875N and BS800.

Transient response

The response to a 50% change in load is less than 200mV and the output returns to the regulation band within 400µs: See Fig.6.

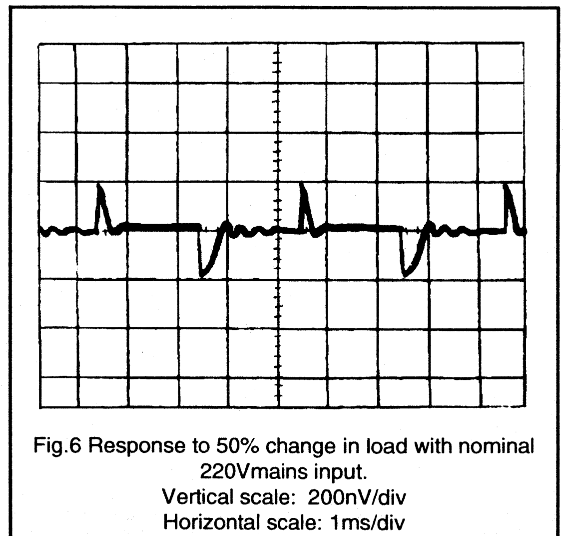


Fig.6 Response to 50% change in load with nominal 220Vmains input.
Vertical scale: 200nV/div
Horizontal scale: 1ms/div

Optimum drive of high voltage Bipolar transistor (H.V.T)

A feature of the high voltage Bipolar transistor is the very low conduction loss that can be obtained. This is made possible by the "conductivity modulation" process that takes place due to the influence of minority carriers in the collector region of the device. However, the presence of these carriers means that a stored charge will exist within the collector region (especially in high voltage types) which has the effect of producing relatively slow switching speeds. This will leads to significant switching losses, limiting the maximum frequency of operation to around 50kHz.

To effectively utilise the power switching H.V.T. the base drive must be optimised to produce the lowest switching losses possible. This is achieved by accurate control of the injection and more importantly the removal of the stored charge during the switching periods. This is fufilled by controlling the transistor base drive current. (The Bipolar transistor is a current-controlled device). The simple steps taken to achieve this are summarised as follows:-

(1) A fast turn-on "kick-up" pulse in the base current should be provided to minimise the turn-on time and associated switching loss.

(2) Provide the correct level of forward base current during conduction, based upon the high current gain of the transistor. This ensures the device is neither over-driven (which will cause a long turn-off current tail) or under-driven (coming out of saturation causing higher conduction loss). The Baker clamp arrangement used (see Fig.1) prevents transistor over-drive (hard saturation).

(3) The correct level of negative base drive current must be produced to remove the stored charge from the transistor at turn-off. The majority of this charge is removed during the transistor storage time t_s. This cannot be swept out too quickly, otherwise a "crowding effect" will taken place causing a turn-off current tail with very high switching loss. This accurate control of the charge is provided by a series inductor placed in the path of the negative base drive circuit. (For further information see sections 1.3.2. and 2.1.3).

BUT11 waveforms

These techniques have been applied in the BUT11 drive circuit shown in Fig.1, and the resulting base drive waveforms are given in Fig.7.

Optimised base drive minimises both turn-on and turn-off switching loss, limiting the power dissipation in both the transistor and snubber resistor allowing acceptable operation at 50kHz. This is outlined in Fig.8. which gives the BUT11 the collector current, I_C and collector-emitter voltage, V_{CE} waveforms.

The transistor $V_{CE(sat)}$ would normally be as low as 0.3V. However, the use of the Baker clamp limits it to about 1V. Even so this still yields a transistor conduction loss of only 0.76W for the full output load condition.

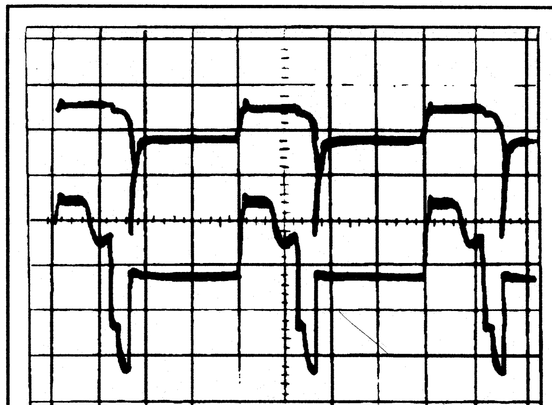


Fig.7 Base voltage V_B and base current I_B of BUT11 with nominal 220V input and full 5V, 20A output.
Upper trace V_B: 5V/div
Lower trace I_B: 0.2A/div
Horizontal scale: 5µs/div

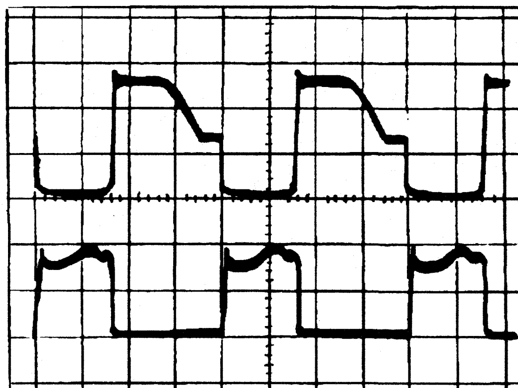


Fig.8 Collector-emitter voltage V_{CE} and collector current I_C for the BUT11 with nominal 220V mains input and full 5V, 20A output
Upper trace V_{CE}: 200V/div
Lower trace I_C: 1A/div
Horizontal scale: 5µs/div

50kHz Magnetics design

Output Transformer

For 50kHz operation the transformer was designed using an ETD39 core. The winding details are given in Fig.9 and listed as follows:-

Winding

1.	1/2 demag	42 turns 0.315mm dia. enamel copper wire (e.c.w.) (single layer).
2, 3	1/2 primary	42 turns 0.315mm e.c.w.(2 layers in parallel).
4, 5	r.f.i screens	each 1 turn 0.05 x 16.5mm copper strip.
6.	5V sec	6 turns 0.2 x 16.5mm copper strip.
7.	±12V sec	18 turns 0.355mm e.c.w. bifilar wound (1 wire each output).
8, 9	r.f.i screens	each 1 turn 0.05 x 16.55mm copper strip.
10, 11	1/2 prim	42 turns 0.315mm e.c.w (2 layer in parallel).
12.	1/2 demag	42 turns 0.315 e.c.w (single layer).
13.	primary drive	7 turns 0.2mm e.c.w.
-	interleaving	0.04mm film insulation.

Airgap 0.1mm total in centre pole.

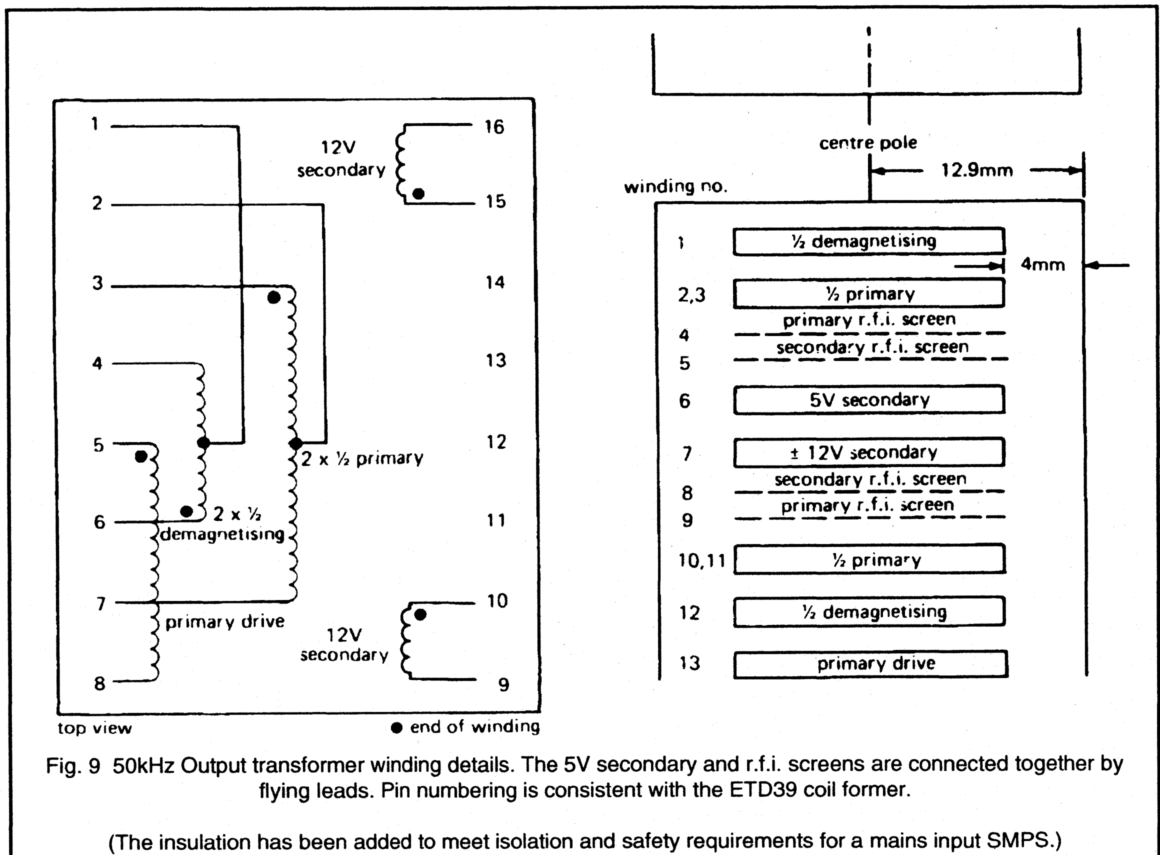


Fig. 9 50kHz Output transformer winding details. The 5V secondary and r.f.i. screens are connected together by flying leads. Pin numbering is consistent with the ETD39 coil former.

(The insulation has been added to meet isolation and safety requirements for a mains input SMPS.)

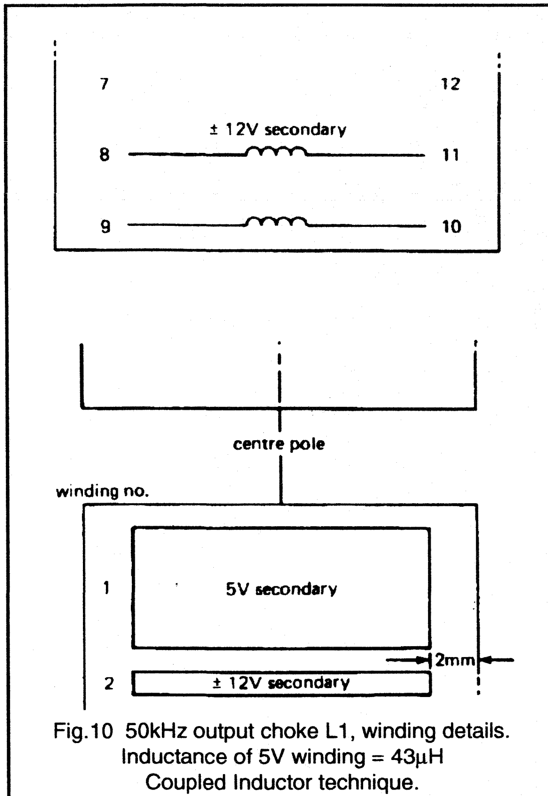


Fig.10 50kHz output choke L1, winding details.
Inductance of 5V winding = 43µH
Coupled Inductor technique.

50kHz output chokes

All of the output chokes have been wound on a single core i.e using the coupled inductor approach. This reduces overall volume of the supply and provides better dynamic cross-regulation between the outputs. The design of this choke, L1 is based upon 43µH for the main 5V output, using an ETD44 core which was suitable for 100W, 50kHz operation.

The winding details are shown in Fig.10 and are specified as follows :-

Windings

1. 19 turns 0.25 x 25mm copper strip.
2. 57 turns 0.4mm e.c.w. bifilar wound.

Airgap 2.5mm total in centre pole.

Note. Choke L3 was wound with 1 turn 0.4mm e.c.w.

100kHz MOSFET version

The circuit version of the 100 W forward converter based around the high voltage power MOSFET is shown in Fig.11. The operating frequency in this case has been doubled to 100kHz.

Feedback is again via opto-coupler IC1, the CNX83A which controls the output by changing the duty cycle of the drive waveform to the power MOSFET transistor, TR3 which is the BUK456-800A (available in TO-220 package or the fully isolated SOT-186 version). The transistor is driven by IC4 via R16 and operates within its SOAR without a snubber: see the waveforms of Fig.15. There is low auxiliary supply voltage protection and primary cycle by cycle current limiting which inhibit output drive pulses and protect the supply.

The power supply control and transistor drive circuitry (enclosed within the broken lines in Fig.11) have low current requirements (5mA). This allows dropper resistors R2 and R3 to provide the supply for these circuits directly from the d.c. link thereby removing the supply winding requirement from the transformer.

Specification and performance (MOSFET version)

The specification and performance of the 100kHz MOSFET version is the same as the earlier 50kHz Bipolar version with the exception of the following parameters:-

Output ripple and noise

< 10 mV r.m.s
< 40mV pk-pk (100MHz bandwidth) See Fig.12

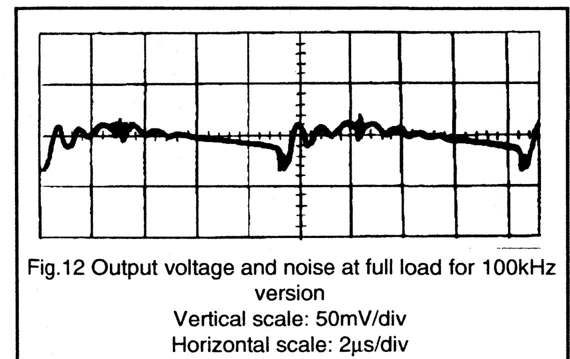


Fig.12 Output voltage and noise at full load for 100kHz version
Vertical scale: 50mV/div
Horizontal scale: 2µs/div

Transient response

The transient response has been improved to a 100mV line deviation returning to normal regulation limits within 100µs for a 10A change in load current.

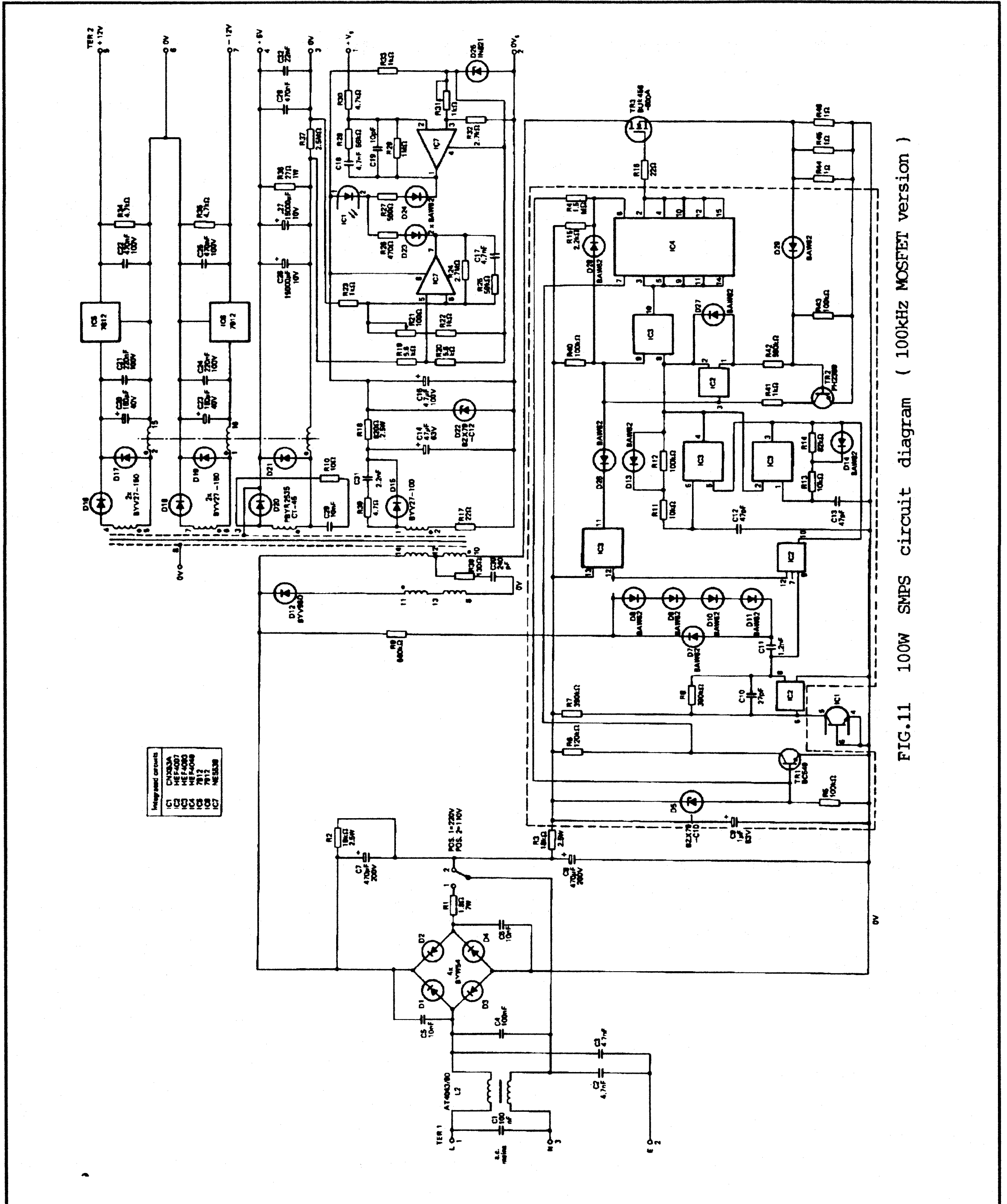


FIG.11 100W SMPS circuit diagram (100kHz MOSFET version)

Radio frequency interference

The 100kHz version meet BS800 and CISPRA recommendations; see Fig.13.

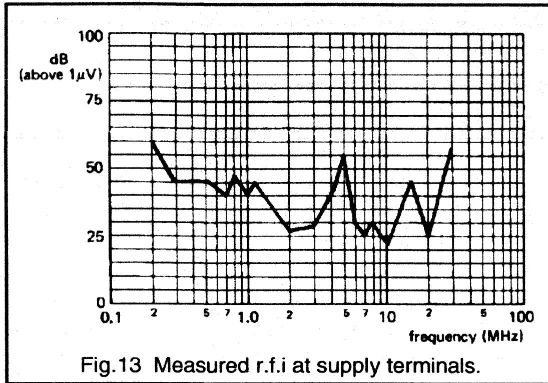


Fig.13 Measured r.f.i at supply terminals.

Efficiency

The overall efficiency has been improved by up to 5% compared to the Bipolar version, achieving 76% at full output load. This is mainly due to the more efficient switching characteristics of the MOSFET allowing the removal of the lossy snubber, reduced transistor drive power requirements and lower control circuit power requirements. Fig.14. shows the overall efficiency of the power supply against load current.

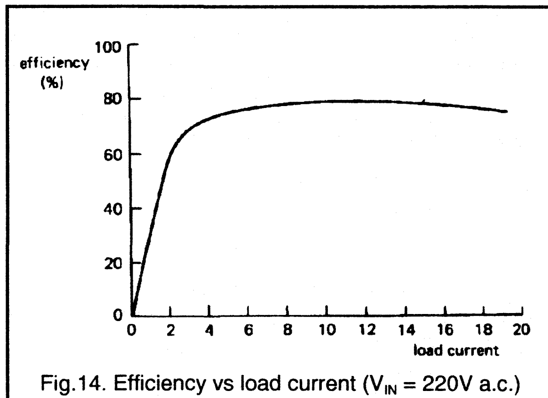


Fig.14. Efficiency vs load current (V_{IN} = 220V a.c.)

It should be noted that for the high current and low voltage (5V) main output, a large portion of the efficiency loss will be due solely to the output rectifiers forward voltage drop V_F. Therefore, these two output rectifiers are required to be low loss, very low V_F power Schottky diodes in order to keep overall converter efficiency as high as possible. In this case the Dual PBRYR2535CT-45 device was selected for the 5V output. This is available in the TO-220 package and will comfortably rectify an average output current well above the 20A required, providing a suitably sized heat-sink is added.

Mains isolation

The mains isolation conforms to IEC435.

The power MOSFET as a high frequency switch

Power MOSFET transistors are well known for their ease of drive and very fast switching characteristics. Since these are majority carrier devices, they are free from the charge storage effects which lessen the switching performance of the Bipolar products. Driving the MOSFET is far simpler and requires much less drive power than the equivalent Bipolar version.

The speed at which a MOSFET can be switched is determined by the rate at which its internal capacitances can be charged and discharged by the drive circuit. In practice these capacitances are very small (e.g the input capacitance C_{iss} for the BUK456-800A is quoted as 1000pF) allowing MOSFET rise and fall times in the tens of nano-seconds region. The MOSFET can conduct full current when the gate-source voltage V_{GS}, is typically 4V to 6V. However, further increases in V_{GS} are usually employed to reduce the device on-resistance and 8V to 10V is normally the final level applied to ensure a lower conduction loss.

With such fast switching times, the associated switching losses will be very low, giving the MOSFET the ability to operate as an extremely high frequency switch. Power switching in the MHz region can be obtained by using a MOSFET transistor.

One major disadvantage of the MOSFET is that it has a relatively high conduction loss in comparison with bipolar types. This is due to the absence of the minority carriers meaning no "conductivity modulation" takes place.

MOSFET on-resistance

The conduction loss is normally calculated by using the MOSFET "on-resistance", $R_{DS(on)}$, expressed in Ohms. The voltage developed across the device during conduction is an Ohmic drop and will rise as the drain current increases. Therefore, the conduction loss is strongly dependent upon the operating current. Furthermore, the value of the MOSFET $R_{DS(on)}$ is strongly dependent upon temperature, and increases as the junction temperature of the device rises during operation. Clearly, the MOSFET does not compare well to the Bipolar which has a stable low saturation voltage drop $V_{CE(sat)}$, and is relatively independent of operating current or temperature.

It should be noted that the $R_{DS(on)}$ of the MOSFET also increases as the breakdown voltage capability of the device is increased.

How fast should the MOSFET be switched?

Although very fast switching times are achievable with the power MOSFET, it is not always suitable or necessary to use the highest frequency possible. A major limiting factor in S.M.P.S. design is the magnetics. Present high frequency core loss for high grade ferrite core materials such as 3C85 limits the maximum operating frequency to about 200kHz, although new types such as 3F3 are now suitable for use at 500kHz.

There has always been a drive to use ever higher operating frequencies with the aim of reducing magnetics and filter component sizes. However, most S.M.P.S designs still operate below 300kHz, since these frequencies are quite adequate for most applications. There is no reason to go to higher frequencies unneccessarily, since very high frequency design is fraught with extra technical difficulties.

Furthermore, although the very fast MOSFET switching times reduce switching loss, the increased dI/dt and dV/dt rates will generate far worse oscillations in the circuit parasitics requiring lossy snubbers. The R.F.I. levels generated will also be far more severe, requiring additional filtering to bring the supply within specification. The golden rule in S.M.P.S. square wave switching design is to use the lowest operating frequency and switching times that the application will tolerate.

Estimating required switching times

In the 100kHz example presented here, the typical conduction time of the transistor will be approximately 3μs. A rule of thumb is to keep the sum of the turn-on and turn-off times below 10% of the conduction time. This ensures a wide duty cycle control range with acceptable levels of switching loss. Hence, the target here was to a produce switching times of the order of 100ns to 150ns.

Gate drive requirements

The capacitances of the power MOSFET are related to the overall chip size with the gate-source capacitance typically in the range 1nF to 2nF. However, these capacitances are very voltage dependent and are not suitable for estimating the amount of drive current required to obtain the desired switching times. A more accurate method is to use the information contained in the turn-on gate charge (Q_G) characteristic given in the data-sheets. The graph of Q_G for the BUK456-800A for a maximum d.c. rated drain current of 4A is shown in Fig.14.

The shape of this characteristic needs explaining. The initial slope shows the rise of V_{GS} to the device 4A threshold voltage V_{th}. This requires very little charge, and at the top point of this slope the MOSFET can then conduct full current. However, further gate charge is required while V_{DS} falls from its off-state high voltage to its low on-state level. This is the flat part of the characteristic and at the end of this region the MOSFET is fully switched on. (This is shown for a range of initial off state voltages). The second slope characterises any further increase in Q_G and V_{GS} that may be employed to minimise the device on-resistance.

Note. Since the turn-off mechanism involving the removal of gate charge is almost identical to the turn-on mechanism, the required turn-off gate charge can also estimated be from the turn-on gate charge plot.

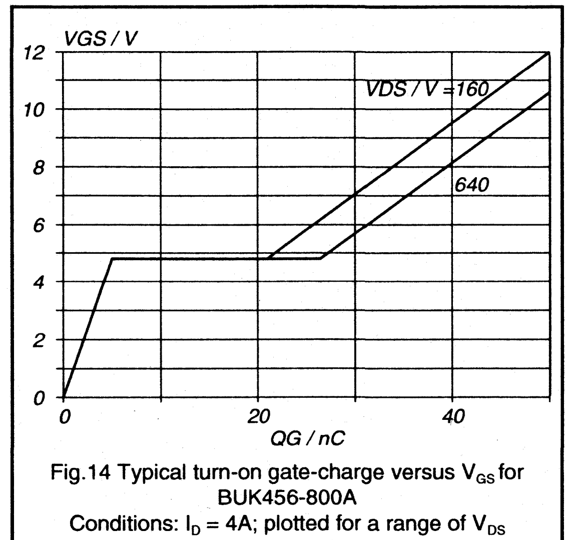


Fig.14 Typical turn-on gate-charge versus V_{GS} for BUK456-800A
Conditions: I_D = 4A; plotted for a range of V_{DS}

In this topology the typical d.c. link voltage is 280V, hence the MOSFET V_{DS} prior to turn-on will be 280V, doubling to 560V at turn-off. From Fig.14 for these two V_{DS} levels it can be estimated that the BUK456-800A will require 23nC to fully turn-on and 27nC to turn off. It should be noted that the this estimation of gate charge is for the 4A condition. In this present application the peak current is under 2A and in practice the actual Q_G required will be slightly less.

To a first approximation the gate current required can be estimated as follows:-

$$Q_G = I_G t_{sw}$$

Where t_{sw} is the applicable switching time. If an initial value of the turn-on and turn-off time is taken to be 125ns then the required gate current is given by:-

$$I_{G(on)} = \frac{23\text{nC}}{125\text{ns}} = 0.184\text{A}; \qquad I_{G(off)} = \frac{27\text{nC}}{125\text{ns}} = 0.216A$$

In the majority of MOSFET drive circuits the peak currents and resulting switching times are controlled by using a series gate resistor R_G. An initial estimation of the value of this resistor can be found as follows:-

$$R_G = \frac{V_{drive} - V_{th}}{I_{G(ave)}}$$

Where $I_{G(ave)}$ is the average value of the turn-on and turn-off peak gate current. In this example the gate driver I.C.4. consists of 5 parallel T.T.L. gates in order to provide high enough current sink and source capability. The driver supply voltage was approximately 10V, the MOSFET threshold voltage was 5V and the average peak gate current was 0.2A.

This gives a value for R_G of 25Ω. A value of 22Ω was selected, and the resulting gate drive waveforms for TR3 under these conditions at the full 100W output power are given in Fig.15

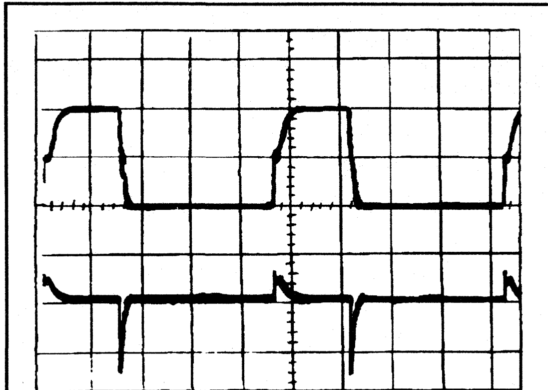


Fig.15 powerMOS TR3 gate drive waveforms.
Upper V_{GS}=5V/div; Lower I_G=0.2A/div
Horizontal 2µs/div

This shows a peak I_G of 0.17A at turn-on and 0.28A at turn-off. The magnitudes of the turn-on and turn-off peak gate currents in operation are slightly different to the calculated values. This is due to the effect of the internal impedance of the driver, where the impedance while sinking current is much lower than while sourcing, hence the discrepancy.

These drive conditions correspond to a turn-on time of 143ns and turn-off time of 97ns, which are reasonably close to the initial target values.

In this application, and for the majority of simple gate drive arrangements which contain a series gate resistor (see section 1.1.3) the total power dissipation of the gate drive circuit can be expressed by:-

$$P_G = Q_G \cdot V_{GS} \cdot f$$

Where Q_G is the peak gate charge and V_{GS} is the operating gate-source voltage. From Fig.14 taking Q_G to be 43nC for a V_{GS} of 10V gives a maximum gate drive power dissipation of only 43mW, which is very small and can be neglected.

MOSFET losses

Switching losses

The waveforms for the drain current and drain-source voltage at full output load for the drive conditions specified are given in Fig.16. In this case no transistor snubbing was required.

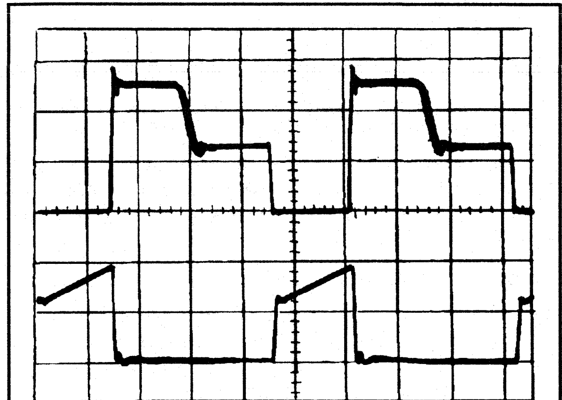


Fig.16 powerMOS drain-source voltage and drain current at full load.
Upper V_{DS}=200V/div; Lower I_D=1A/div
Horizontal scale 2µs/div

The waveforms of I_D and V_{DS} were found to cross at approximately half their maximum values for both turn on and turn-off. The switching loss can therefore, be approximated to two triangular cross-conduction pulses shown in Fig.17.

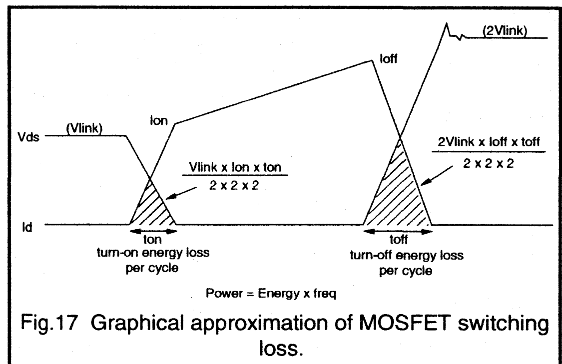


Fig.17 Graphical approximation of MOSFET switching loss.

Hence, the total switching loss can be expressed by the following simplified equation:-

$$P_{sw} = \frac{1}{8} f \left(I_{Don} V_{link} t_{on} + I_{Doff} 2V_{link} t_{off} \right)$$

Inserting the correct values for this example gives:-

$$P_{sw} = 0.125 \times 100k(1.3 \times 280 \times 147n + 1.95 \times 560 \times 97n)$$

$$= 0.67W + 1.06W = 1.73W$$

The MOSFET switching loss in this application is a very respectable 1.73W. It should be noted that a direct comparison with the switching loss of the earlier Bipolar version is not practical. It was necessary to use a snubber with the Bipolar in order to remove a large amount of the excessive switching loss generated by the device. Furthermore, the MOSFET switching frequency implemented was double that of the Bipolar version.

If a direct comparison were to be made under the same circuit conditions, the Bipolar switching loss would always be far in excess of the low values achievable with the MOSFET.

Conduction loss

The conduction loss for a power MOSFET is calculated by estimating $(I_{D(rms)})^2 R_{DS(on)}$. The drain current at full output load is as shown in Fig.16. and the r.m.s. value of the trapezoidal current waveforms found in the forward converter is given by:-

$$I_{rms} = \sqrt{D\left(\frac{I_{min}^2 + I_{min} I_{max} + I_{max}^2}{3}\right)} \qquad D = \frac{t_{ON}}{T}$$

At full load, these values can be seen to be I_{min}=1.25A; I_{max}=1.95A; D= 0.346. Substituting these values into the above equation gives an $I_{D(rms)}$ = 0.95A.

The typical $R_{DS(on)}$ value for the BUK456-800A is quoted as 2.7Ω. However, this is for a junction temperature of 25˚C. The value at higher operating junction temperatures can be calculated from the normalisation curve given in the data-sheets. If a more realistic operating temperature of 100˚C is assumed, the weighting factor is 1.75. Hence, the correct $R_{DS(on)}$ to use is 4.725Ω. Therefore, the conduction loss is given by:-

$$P_{cond} = (0.95)^2 4.723 = 4.26W$$

The conduction loss of 4.26W is over double the switching loss. However, this is typical for a high voltage MOSFET operated around this frequency. The MOSFET conduction loss is much higher than was previously obtained using the Bipolar transistor at 50kHz, as expected.

The total loss for the MOSFET device thus comes to 6W i.e. 6% of the total output power.

It should be remembered that this figure has been calculated for the full output load condition which will be a transient worst case condition. A more realistic typical dissipation of approximately 4W has been estimated for the half load condition, where the conduction loss is approximately halved. This 4W figure should be used when estimating the heat-sink requirement. In this case a relatively small heat-sink with a thermal co-efficient of around 10˚C/W would be adequate.

For more information on MOSFET switching refer to chapters 1.2.2. and 1.2.3. of this handbook.

100kHz magnetics design

Output transformer

Doubling the switching frequency to 100kHz has allowed the use of the smaller sized ETD34 core for the transformer. This transformer has been designed with a 0.1mm centre pole air gap. The winding details are shown in Fig.18 and listed as follows:-

Winding

2 to 1	Regln supply	
5 to 4	+12V sec	3 x 12 turns 0.4mm e.c.w. in 1 layer.
6 to 7	-12V sec	3 x 12 turns 0.4mm e.c.w. in 1 layer.
8	r.f.i. screen	1 turn 0.1 x 13mm copper strip.
10 to 12	1/2 prim	28 turns 0.355mm e.c.w. bifilar in two layers.
11 to 13	1/2 demagn	28 turns 0.355mm e.c.w. in 1 layer.
12 to 14	1/2 prim	28 turns 0.355mm e.c.w. bifilar in 2 layers.
13 to 8	1/2 demagn	28 turns 0.355mm e.c.w. in 1 layer.

Interleaving:- 1turn 0.04mm insulation between each layer except 3 turns between r.f.i. screens.

Output choke

Again the implementation of the higher frequency has allowed the use of the smaller sized ETD39 core for the coupled output inductor. A centre pole air-gap of 2mm was utilised. The winding details are shown in Fig.19 and are listed as follows:-

Winding

Copper strip	+5V	15 turns 0.3 x 21mm copper strip.
2 to 15	-12V	45 turns 0.4mm e.c.w in 1 layer.
1 to 16	+12V	45 turns 0.4mm e.c.w in 1 layer.

Interleave:- 1 layer 0.04mm insulation between each strip and winding.

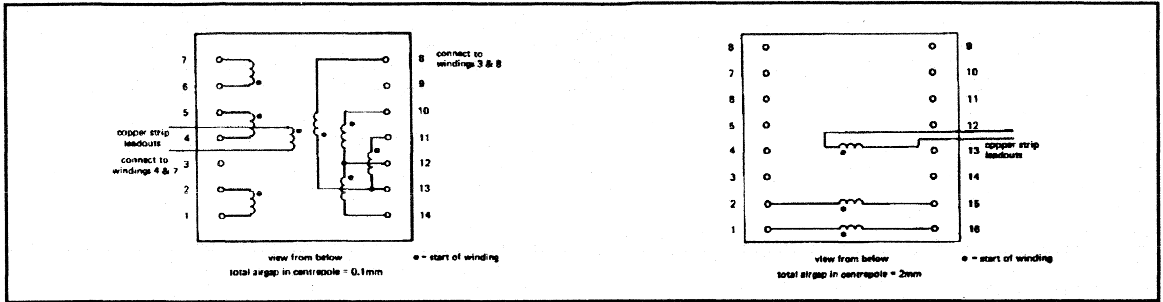


Fig.18 100kHz transformer construction.

Fig.19 100kHz inductor construction.

2.3.2 Flexible, Low Cost, Self-Oscillating Power Supply Using An ETD34 Two-Part Coil Former And 3C85 Ferrite.

This section describes a low-cost, flexible, full performance, Self Oscillating Power Supply (SOPS) using the flyback principle.

The circuit is based around an ETD34 transformer using a two-part coil former and 3C85 ferrite material. The feedback regulation is controlled from the secondary side by means of a small U10 transformer.

The circuit is described and the details of the magnetic design using the two-part coil former is given. The advantages of the two-part coil former are highlighted together with 3C85 material properties. Power supply performance of a 50W SMPS design example is given.

Introduction.

A recently developed low-cost full-performance switched-mode power supply design is presented, highlighting a new transformer concept using a novel ETD34 two-part coil former and 3C85 low-loss material. The SMPS is of the Self Oscillating Power Supply (SOPS) type and uses the flyback principle for minimum component count and ultra-low cost/watt.

Compliance with safety and isolation specifications has always been a headache for magnetics designers. Now, the introduction of the ETD34 two-part coil former solves the problem of the 4+4mm creepage and clearance distances, by increasing the available winding area and consequently decreasing copper losses. It also offers the advantage of a more flexible approach with the possibility of using a standard 'plug-in' primary and a customised secondary to meet any set of output requirements.

3C85 is a recently developed material superseding 3C8 and offers lower core loss, better quality control and higher frequency operation at no extra cost.

These products are illustrated in the following 50W SMPS design example, which is suitable for microcomputer applications.

SOPS

The principle of the Self-Oscillating Power Supply is shown in Fig.1 and is based on the flyback converter principle. Stabilisation of the output voltage against mains and load variation is achieved by varying the duty cycle of the powerMOS switching transistor. The on-time varies mainly with input voltage, whereas the off-time varies only with the load. This means that both the duty cycle and the frequency vary due to the control circuit. The switching frequency is therefore at a maximum for maximum input voltage and minimum load. Regulation is achieved by varying the point at which the POWERMOS transistor is switched off. A.C. magnetic coupling is used in preference to opto-couplers for long-term life stability and guaranteed creepage and clearance. This circuit has the inherent property of self limiting energy transfer, since the maximum energy $1/2LI^2$, is defined by the bipolar transistor V_{BE} threshold and the source resistance value.

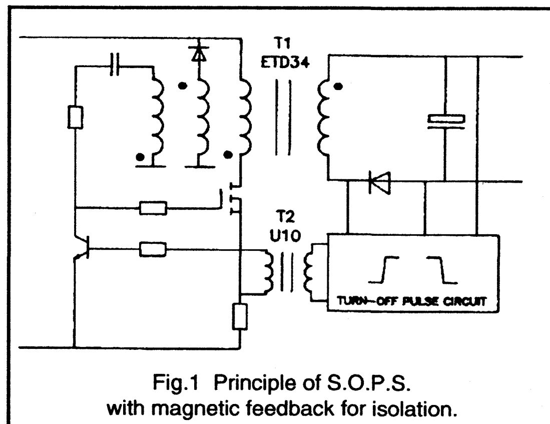


Fig.1 Principle of S.O.P.S. with magnetic feedback for isolation.

The Transformer

The transformer uses the versatile ETD system. This is the range of four IEC standardised cores based on an E-core shape with a round centre pole. This permits easy winding especially for copper foil and standard wire. The ETD system includes coil formers into which the cores are clip assembled. The coil formers are designed for automatic winding and comply with all the standard safety specifications.

The two-part coil former was especially designed for the ETD34, and is shown in Fig.2. There is 25% more winding area compared to the standard coil former yet full safety isolation is provided so that the creepage and clearance specifications are fully met. The inner part is a "click" fit into the outer part, such that the former is mechanically stable even with the cores removed. This two-part construction leads to a very versatile winding approach where standard primaries can be wound and assembled, yet still retaining the flexibility for various secondaries to be added for different requirements.

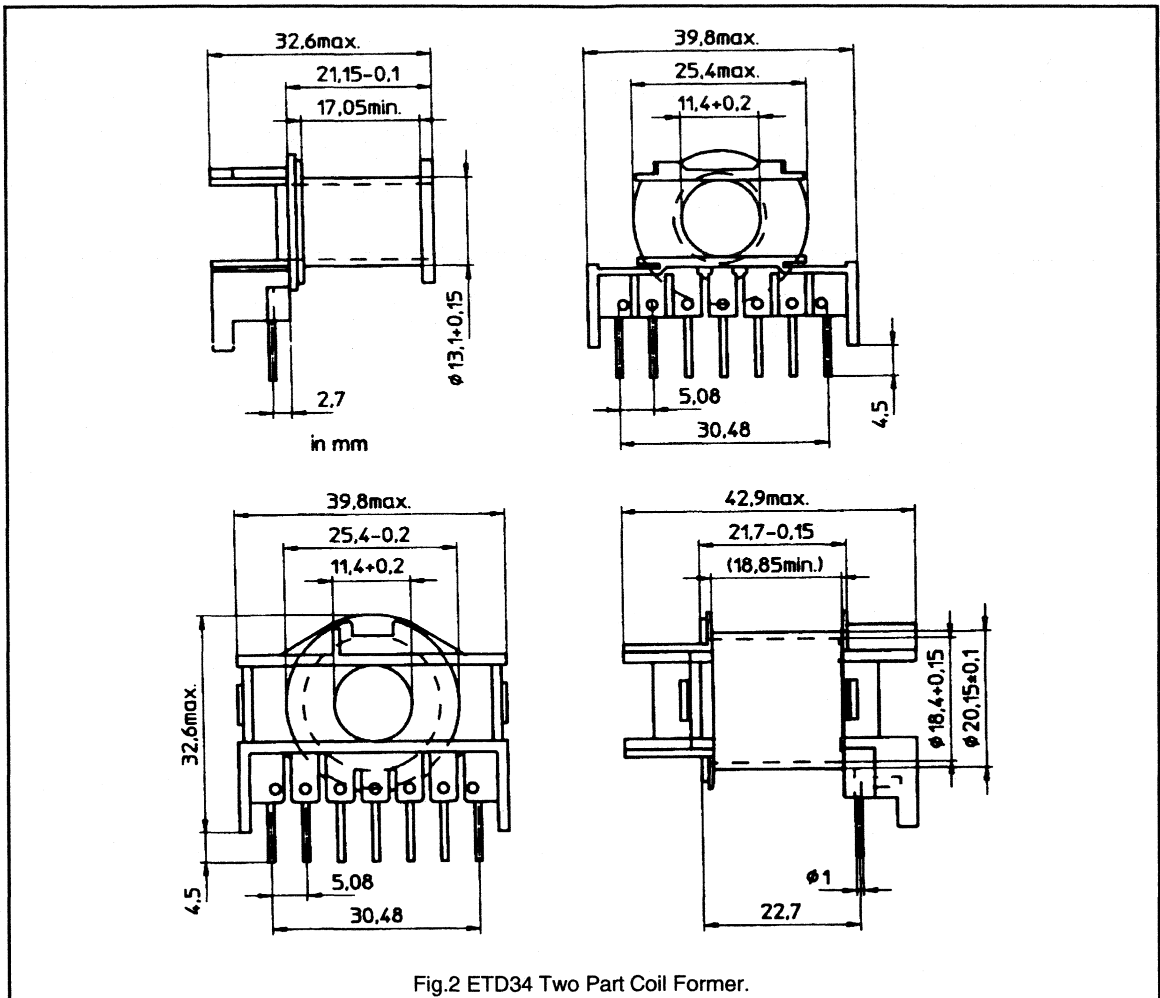


Fig.2 ETD34 Two Part Coil Former.

Leakage inductance is always a problem with flyback transformers, but using this special construction the increase in leakage can be almost offset by the greater winding area of the two-part coil former when compared to the standard product with 4 + 4mm creepage and clearance. Fig.3. shows standard and two part transformer cross-sections, where the leakage inductance is not more than 20% greater for the two-part coil former for this 50W design.

The transformer details for the 50W microcomputer power supply design example are shown in Fig.4. The primary side consists of three windings:- a feedback winding of 5 turns, the main primary winding and a bifilar voltage clamp winding of 92 turns. This is achieved with 4 layers to fill the inner coil space area. The secondaries consist of a 5V winding of 3 turns and the $\pm$12V windings of 7 turns each. As there are so few turns, the winding area is most effectively filled with stranded wire, copper strip or parallel windings, and these are therefore all possible choices.

In addition to the improved windings possibilities with the two-part coil former, the ETD core material has been enhanced. The quality of the 3C85 material is much improved compared to the older 3C8 type. Fig.5 compares curves of core loss versus frequency for 3C85 against 3C8. The 30% improvement in 3C85 has been due to refining the material composition and tighter process quality control.

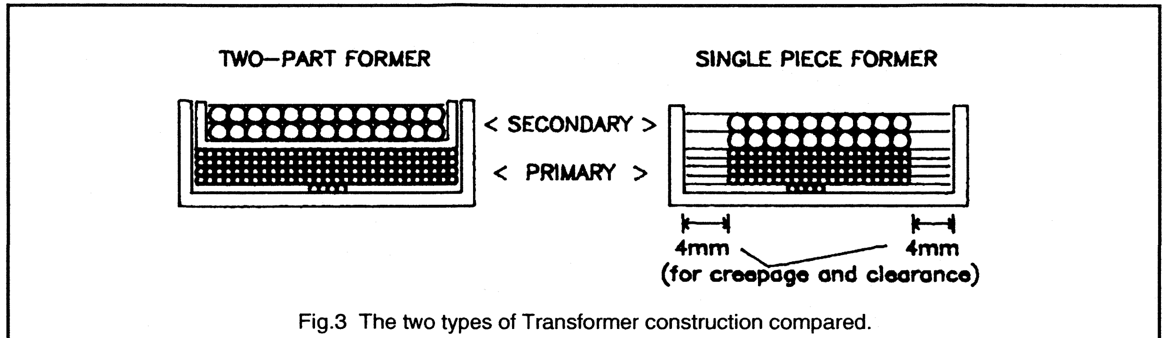


Fig.3 The two types of Transformer construction compared.

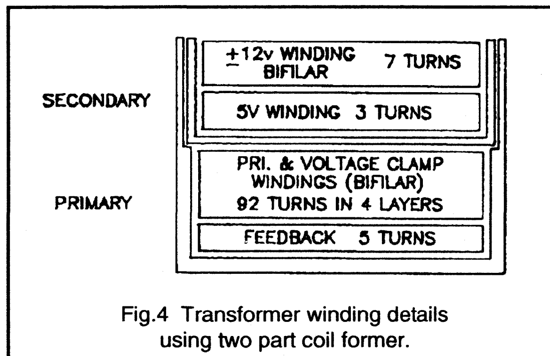


Fig.4 Transformer winding details using two part coil former.

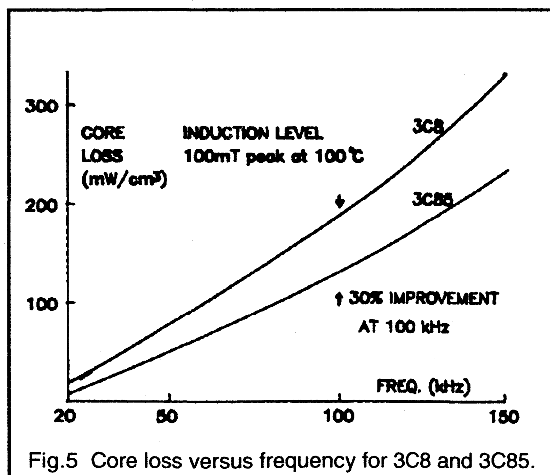


Fig.5 Core loss versus frequency for 3C8 and 3C85.

Application and Operation of SOPS

The SOPS circuit is ideally suited for microcomputer systems, where full performance at low cost is required. The 50W output power is split between a regulated 5V output at 5A for the logic, a +12V output at 1.8A and a -12V output at 0.2A for the peripherals. The circuit diagram of the power supply is shown in Fig.6. The operating frequency varies from 250kHz at open circuit to 35kHz at full load. The circuit works as follows:-

The mains input is filtered (L1), rectified (D1-D4) and smoothed (C7) to provide a d.c. rail. This supply rail utilises a single electrolytic capacitor which is a low profile , low cost, snap-fit 055 type.

The main switching transistor, Q1, is a TO-220 powerMOS device, the BUK456-800A. Starting current is provided via R1 to Q1 to start the self-oscillating operation. Feedback current is provided by a small winding on the transformer (T1), via C8 to maintain bias. Duty cycle control is via R5 and T2, with final control being achieved with R5, T2 and Q2. The triangular transformer magnetising current is seen across R5 as a voltage ramp, see Fig.7. This is fed to the base of Q2, via a small U10 transformer, T2. When the voltage becomes greater than the V_{BE} of the transistor, Q2 is turned on, causing the gate of Q1 to be taken to the negative rail, so terminating the magnetisation of the transformer T1. The output voltage is controlled by feeding back a turn-off pulse by means of T2, thus causing Q2 to turn on earlier.

A voltage clamp winding is bifilar wound with the primary to limit voltage overshoots on the drain of Q1 at turn-off, thus ensuring that the transistor operates within its voltage rating.

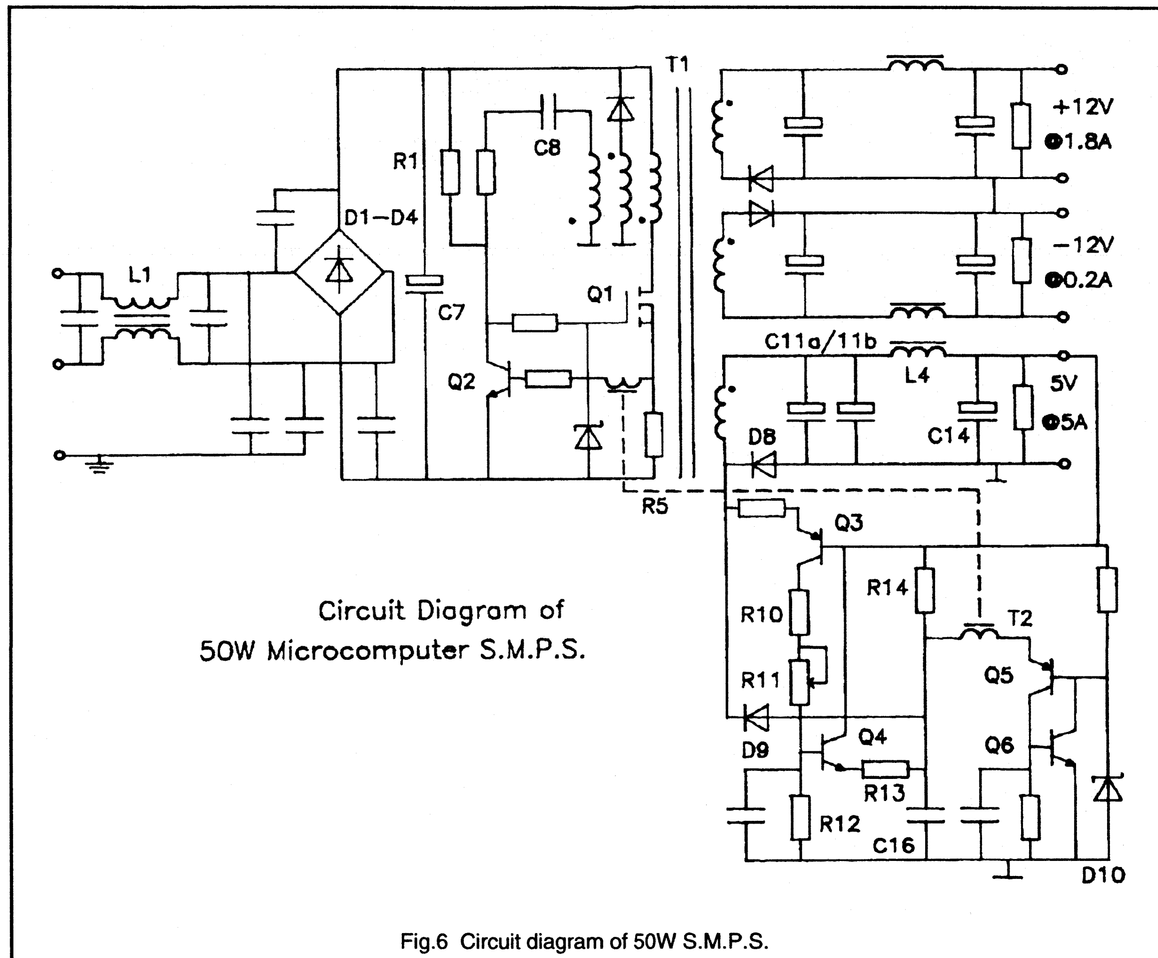


Fig.6 Circuit diagram of 50W S.M.P.S.

Maximum throughput power is determined by the value of R5, the higher it's resistance value, the lower the maximum power. The same drive and control circuit can be used for different throughput powers, ETD core sizes and powerMOS transistors.

The 5V secondary uses a single plastic TO-220 Schottky diode, the PBYR1635 shown as D8. The output filter is a pi type giving acceptable output ripple voltage together with good transient response. Two electrolytic capacitors are used in parallel, C11a/C11b (to accommodate the ripple current inherent in flyback systems), together with a small inductor wound on a mushroom core, L4, and a second capacitor, C14.

The turn-off pulse is created, cycle-by-cycle, by charging a capacitor from the output and comparing it with a reference, D10 and by using the transition signal to feedback a turn-off pulse via transformer T2. A potential divider is present across the output 5V rail, consisting of R10, R11 and R12, via Q3. The potential divider controls the base voltage of the transistor Q4, which charges capacitor C16 via R13. The voltage on C16 ramps up to a voltage equal to that on the base of the transistor less the V_{BE}, causing Q4 to switch off. The capacitor continues to charge more slowly via resistor R14, i.e. a ramp and pedestal (see Fig.8), until the voltage on the emitter of Q5 is equal to the voltage determined by the band-gap reference D10 (2.45V) plus the V_{BE} drop of Q5. When this voltage is reached Q5 switches on, causing Q6 to switch on, pulling Q5 on harder. The edge produced is transmitted across T2 and adds to the voltage on the base of Q2. Transistor Q3 is there to maintain the voltage level at the end of the 'on' period of

the waveform to prevent premature switching. Capacitor C16 is reset by diode D9 on the edge of the switching waveform of the schottky diode, D8.

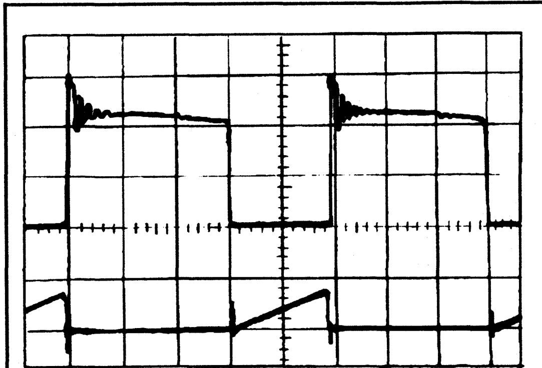


Fig.7 BUK456-800A powerMOS transistor switching waveforms.
Top trace - Drain voltage V_{DS} 200V/div
Bottom trace - Source current I_S 1A peak (across R5)
Timebase - 5µs/div

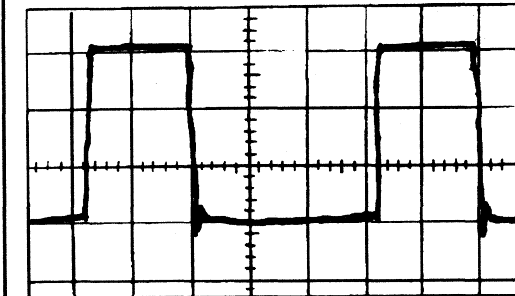


Fig.8 Ramp and pedestal control waveforms across C16 = 1V/div, 5µs/div

Performance

The performance of the supply is as follows: the 5V output has load regulation of 1.2% from 0.5A to 5A load current. The line regulation is 0.5% for 187V to 264V a.c. mains input voltage.

The 12V secondaries are unregulated, and therefore have an inferior regulation compared to the 5V output. Each rail has a load regulation of 6% from open-circuit to full load: this is adequate for typical microcomputer peripheral requirements.

The efficiency of the power supply is typically 80%. The ripple and noise on all outputs is less than 75mV peak to peak. The radio frequency interference is less than 50dB (above 1µV) from 150kHz to 30MHz and complies with VDEO875 and BS800, based on a 150Ω V network. See Fig.9. The transient response of the 5V output due to a 2A to 5A step load change gives a deviation of 100mV.

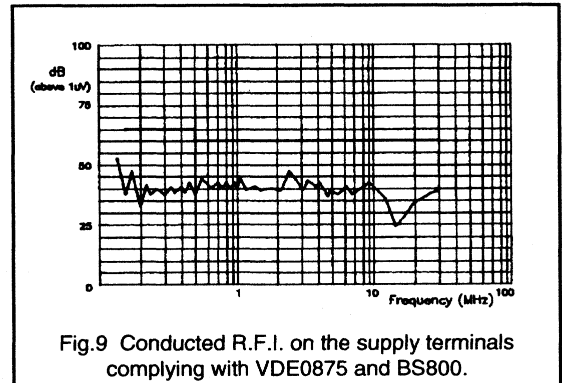


Fig.9 Conducted R.F.I. on the supply terminals complying with VDE0875 and BS800.

Conclusion

A novel Self Oscillating Power Supply has been introduced featuring two recently developed products, increasing the cost effectiveness and efficiency of low-power SMPS:-

The new ETD34 two-part coil transformer featuring:

* isolation problems solved
* standard 'plug-in' primaries
* suitable for automatic winding
* ETD system compatible.

The 3C85 ferrite material offers:

* 30% lower loss than 3C8
* comparable price with 3C8
* high frequency operation, up to 150kHz
* improved quality

2.3.3 A 100 kHz SMPS Using An Emitter Driven Darlington Transistor.

A major limitation of the bipolar high voltage transistor is it's switching speed. Under normal base drive conditions, the need for rapid charge extraction during turn-off results in high negative base currents as well as long storage times. Hence switching frequencies are typically limited to less than 30kHz. It is however possible to overcome these problems, and quite dramatically increase the useable switching frequency. This is achieved by abandoning conventional base drive techniques and using an emitter drive (or cascode switch) configuration. This section describes some aspects of emitter drive and presents a 100kHz SMPS example using a Darlington transistor. The experiences and new insights gained during the design of the converter are also outlined.

Basics of emitter drive

The general principle of emitter drive is shown in Fig.1. T1 is a low voltage PowerMOS (or bipolar transistor) and consequently can easily be directly driven by an IC. T1 interrupts the emitter current of the high voltage transistor T2, and so the combination of the two provides high voltage switching with the easier driving of a low voltage transistor. Note that there is no negative voltage rail, which is often present in S.M.P.S drive circuits.
When T1 is turned-on by the drive circuit, capacitor C discharges via the base of T2 and a high turn-on base current will flow into T2. Care should be taken in choosing a value for C: too high a value may result in severe overdrive with bad turn-off conditions.

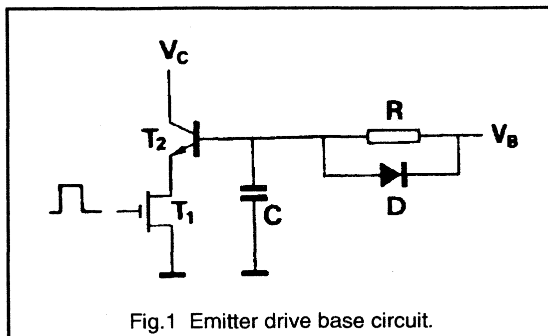


Fig.1 Emitter drive base circuit.

During the transistor on-state, a positive base current is fed from the voltage source V_B via resistor, R. When T1 is turned-off, the emitter current of T2 is interrupted. The negative base current of T2 thus, equals the collector current, ensuring a short storage time. This negative base current charges the capacitor again, but the voltage is limited (via D) to $V_B + V_D$ volts.

An important factor to consider is that the turn-off mechanism within the high voltage transistor T2, differs significantly for base drive and emitter drive (see chapter 3). As a consequence, the Reverse Bias Safe Operating Area (SOAR) of emitter drive is drastically improved in comparison with base drive. As a practical rule one may say that the RBSOAR of an emitter driven high voltage transistor is square, and is essentially extended to the point I_{Csat} / V_{CESmax}. For base drive this is approximately the point I_{Csat} / V_{CEOmax}. In high voltage transistors (HVTs) V_{CEOmax} is typically half the V_{CESmax} value.

To summarise, the advantages of emitter drive are:-

- fast turn on.
- short storage time.
- wide RB SOAR.
- simple drive circuit without negative voltage source.

Switching phenomena of base and emitter drive

Reference [2] describes in detail the internal behaviour of carriers inside a high voltage transistor when base drive is used. In the on-state, just before turn-off, three charges in the transistor are recognised: the base charge, Q_B, which is essential for transistor operation, the collector charge, Q_C, which yields a low resistive collector area providing a low V_{CEsat}, and the diode charge Q_D in the neutral diode, which is present in hard saturation. In the case of base drive it is shown that first, the diode charge is removed, then the base and collector charges decrease, starting from the edges of the active emitter.

At the end of the storage time, the last remnants of the base charge are removed, resulting in the first part of the fall time. The removal of the collector charge, which is trapped in the collector area, is responsible for the current tail found in HVTs (see Fig.2).

This model has been derived from waveforms observed in practical circuits. Furthermore, laser absorption measurements have been carried out at the Philips Research Laboratories on a circuit using conventional base drive, and the results of these measurements are in full agreement with the above [3]. For emitter drive, these measurements have yet to be done.

When using emitter drive, the turn-off behaviour is similar to the recovery of a power diode. As a consequence, the charge removal will be rather homogeneous over the chip. As in the case of base drive, for emitter drive the diode

charge will be the first to be removed, but at the same time collector and base charge are already contributing to the negative base current. During the turn-off the charge will move up in the direction of the base contact. At the end of the storage time the total charge remaining is insufficient to maintain the collector current, hence the voltage rises rapidly, thereby sweeping out the rest of the carriers. The total rest charge is generally higher compared to base drive and thus, the fall time will be worse.

Fig.2 gives the various stages of turn-off for both base- and emitter drive. From this illustration it follows that for base drive, a current-concentration is a logical consequence of this way of driving, whilst for emitter drive the turn-off mechanism is more a bulk effect taking place all over the crystal. As a result there is a big difference in the Reverse Bias SOAR for the two ways of driving: emitter drive extends the RB SOAR up to V_{CESmax}.

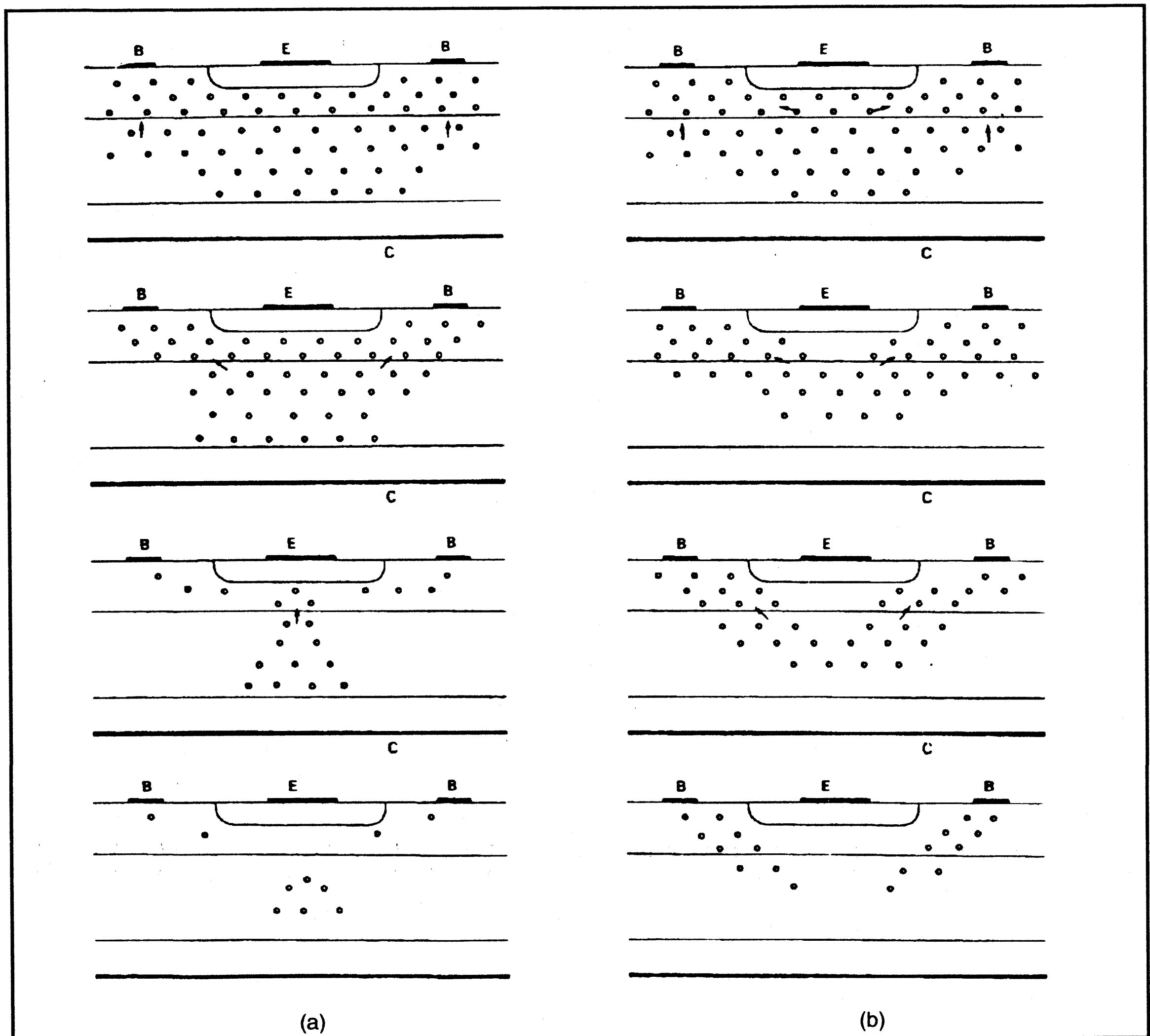


Fig.2 Internal transistor carrier behaviour at turn-off for (a) base drive (b) emitter drive.

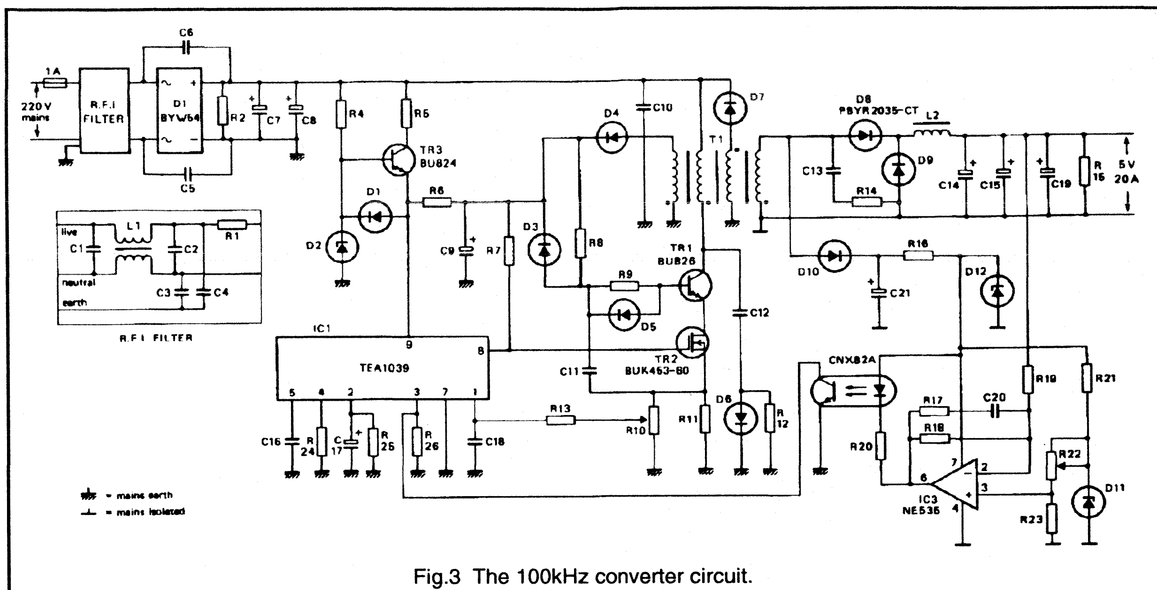


Fig.3 The 100kHz converter circuit.

A 100 KHz emitter-driven converter

Reference [1] describes a forward converter with an emitter switched BU826 Darlington. In this particular example, the low voltage switch in the BU826 emitter is a Bipolar transistor. Operating at 50KHz, it is a good example for showing the benefits of emitter drive.

If one takes a closer look at the advantages of emitter drive, operation at frequencies higher than 40kHz reveals this configuration to be even more favourable.

When discussing high frequency S.M.P.S it is often stated that only PowerMOS is suitable for this application, however, bipolar switches with modern technologies (like generation III transistors) can also be an excellent choice for 100KHz switchers.

To study the possibilities of bipolar switching at 100KHz it was decided to construct a forward converter which was similar to the previous version outlined in [1]. As a bonus, one might then benefit from the smaller and cheaper components required at the higher frequency. The finalised circuit is shown in Fig.3.

One can easily recognise the standard forward converter configuration, with the demagnetising winding, output choke and diodes.

At switch-on of the power supply, Darlington T3 conducts and delivers an initial current for starting up. IC1 is a 9-pin SIL SMPS driver IC containing the blocks shown in Fig.4.

This IC, the TEA1039 contains a power stage capable of driving up to 1Amp. It can also be used with frequency or duty cycle modulation, determined by the voltage on pin 6. Pins 4 and 5 determine the oscillation frequency, which also depends upon the modulator section. The state of the modulator is determined by the error input, the maximum f_{osc} or duty cycle input and the overload protection input. The required external reference and error amplifier are usually found at the secondary side so, the signal is fed back to the error input pin 3 via an optocoupler to keep the isolation intact.

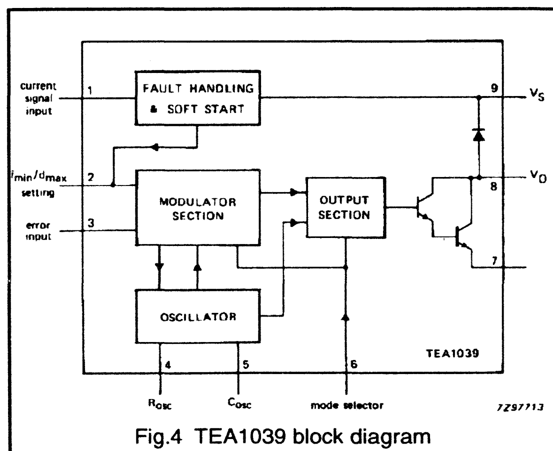


Fig.4 TEA1039 block diagram

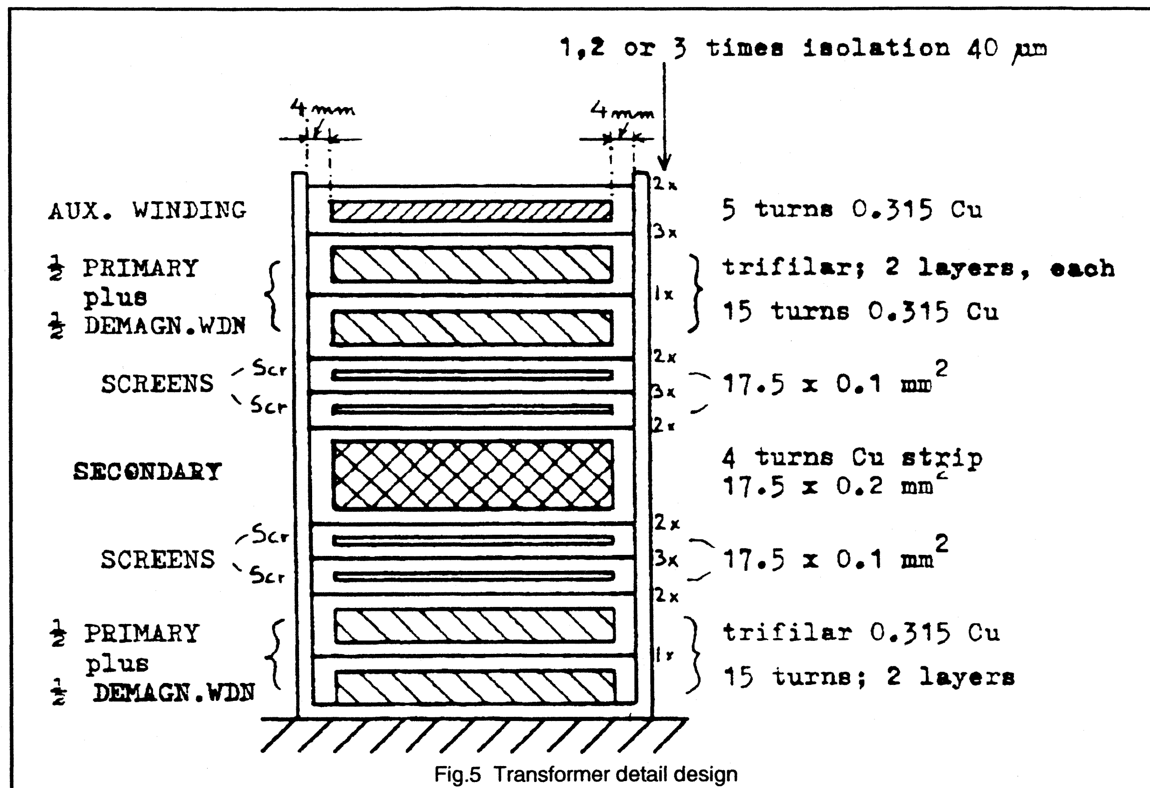


Fig.5 Transformer detail design

Once the power supply is fully working, a winding on the transformer delivers a positive voltage via D4 to C9, which feeds the powerswitch. This then supplies the driver IC via R6, ALSO shutting off the BU824 at the same time.

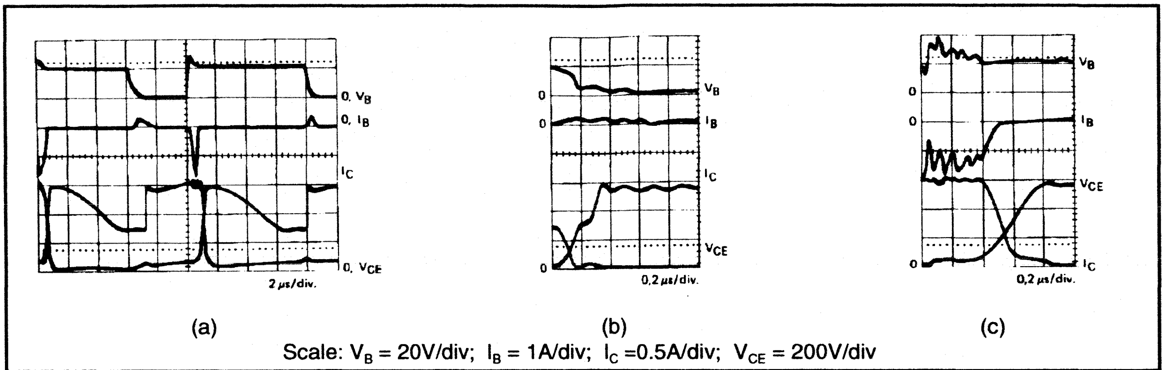
The TEA1039 directly drives the low voltage PowerMOS BUK453-60A, which is connected to the emitter of the high voltage Darlington BU826. On can easily reecognise the basic emitter drive configuration outlined in Fig.1. To avoid the effects of the turn-on peak current delivered by C11, this capacitor is connected to R10 and R11 rather than ground. Fast peak current monitoring is provided via R13 and C18 to pin 1 of the TEA1039.

The extra components R9 and D5 are needed to limit positive base drive, $+I_B$ to its maximum rated value.

In order to achieve optimum utilisation of the transformer an eloquent design was required. To reduce copper losses, the secondary winding was made of a copper strip and sandwiched between two primary halves. The demagnetising winding, consisting of two wires in parallel, was wound simultaneously with the primary. A number of screens were added between the windings, aimed at reducing RFI. A detailed drawing of the design is given in Fig.5. Modern ETD cores were used for both the transformer (ETD39) and the choke (ETD34).

Measurements done on the converter

The waveforms for the BU826 output transistor are given in Fig.6. The global I_C, V_{CE}, I_B and V_B waveforms are easily recognised in Fig.6(a), while Figs.6(b) and 6(c) give clearer details of the turn-on and the turn-off.



(a) (b) (c)

Scale: V_B = 20V/div; I_B = 1A/div; I_C =0.5A/div; V_{CE} = 200V/div

Fig.6 Waveforms for 100kHz emitter driven Darlington.

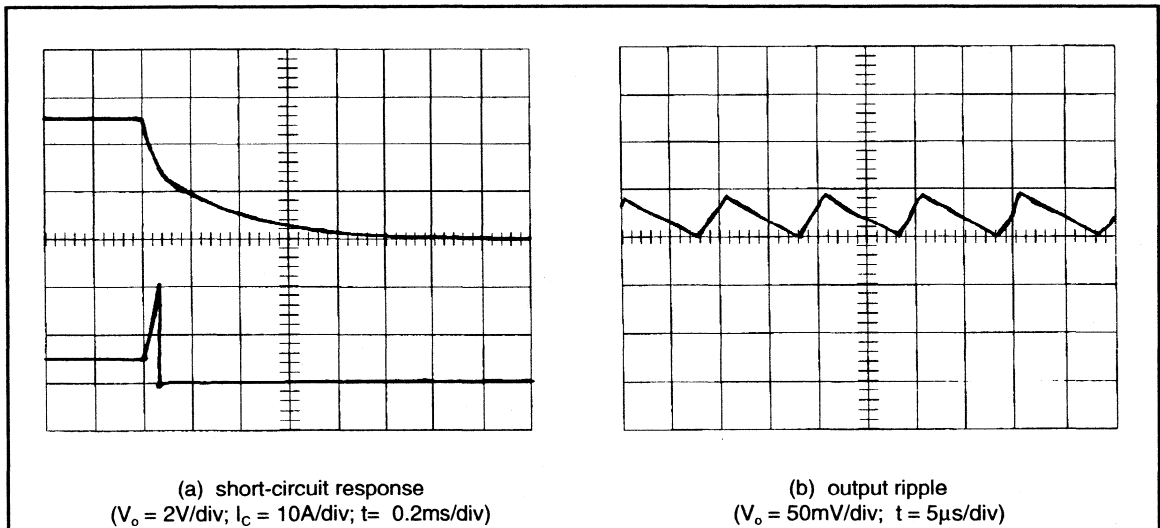
At an ambient temperature of 25˚C, a 40˚C rise in temperature of the semiconductors and magnetic components was observed.

Some performance characteristics of the supply were measured, and the major parameters are outlined in Figs.7, 8 and 9.

Fig.8 shows the short-circuit response of the supply and the ripple voltage of the output. Close inspection reveals the following:-

- excellent short circuit proof (Fig.7(a))

- low output ripple < 45mV (Fig.7(b))



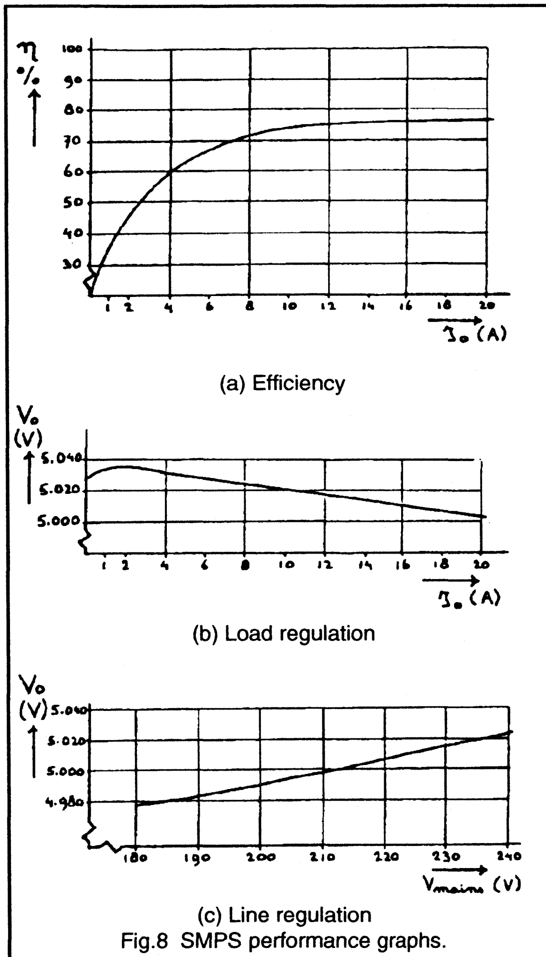
(a) short-circuit response
(V_o = 2V/div; I_C = 10A/div; t= 0.2ms/div)

(b) output ripple
(V_o = 50mV/div; t = 5µs/div)

Fig.7 Aspects of SMPS performance.

Fig.8 gives graphs of the important supply specifications of efficiency and load and line regulation, and close inspection reveals:-

- an efficiency of 76% at loads more than 10A (Fig.8(a))
- a load regulation better than 0.6% (Fig.8(b))
- a line regulation better than 0.9% (Fig.8(c))



(a) Efficiency

(b) Load regulation

(c) Line regulation

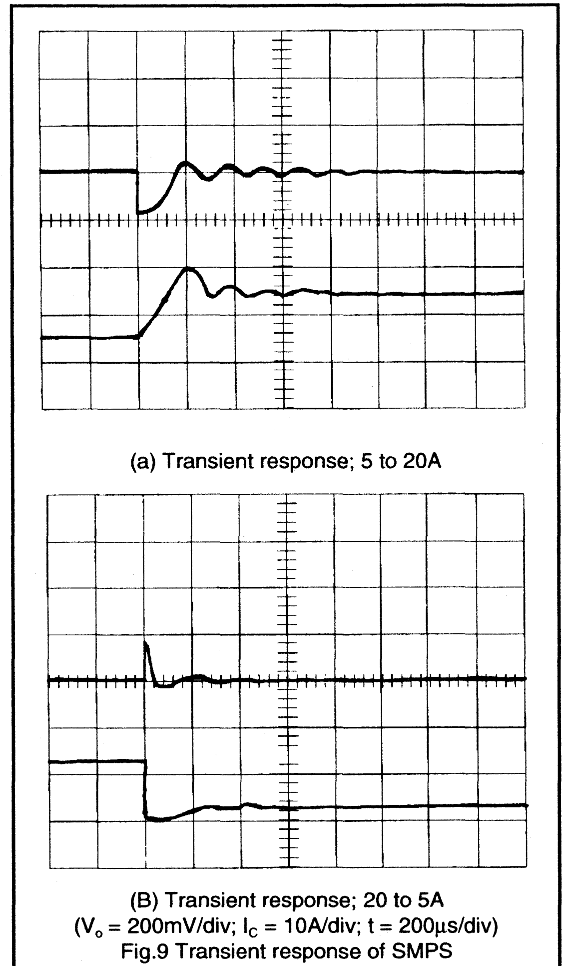
Fig.8 SMPS performance graphs.

The transient response time of the supply (from 5A to 20A or from 20A to 5A) is about 200μs, and the output voltage transient is 0.2V max. These responses are shown in the waveforms of Fig.9

Conclusions

Emitter-switching is a worthwhile design alternative, as it results in fast turn-on, short storage time and a wide RBSOAR.

These properties turn out to be especially advantageous at higher frequencies, and it is believed that at around the 100kHz level, emitter drive is an essential tool when using bipolar switches.



(a) Transient response; 5 to 20A

(B) Transient response; 20 to 5A

(V_o = 200mV/div; I_C = 10A/div; t = 200μs/div)

Fig.9 Transient response of SMPS

A practical design using a modern-technology monolithic Darlington the BU826, emitter driven by a PowerMOS BUK453-60A was presented. It shows that operating frequencies of 100 kHz are of practical use in present days designs using bipolar transistors. The presented converter showed that very good performance that can be obtained by using modern-technology components.

Acknowledgements

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(International Product Marketing ICs, Nijmegen) and especially Ger van Dijk whose help in the magnetics design was appreciated.

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[2] Tinus v.d. Wouw, "Switching phenomena and base drive design", Proceedings of Power conversion International 1981, Munchen.

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Magnetics Design

2.4.1. Improved ferrite materials and core outlines for high frequency power supplies

Increasing switching frequency reduces the size of magnetic components. The current trend is to promote SMPS miniaturisation by using this method. The maximum switching frequency used to be limited by the performance of available semiconductors. Nowadays however, Power MOSFETs are capable of square-wave switching at 1MHz and beyond. The ESL of the output capacitor had until recently limited any major size reduction in output filter above 100kHz. The advent of multi-layer ceramic capacitor stacks of up to 100µF removed this obstacle. This allowed the operating frequency to be raised significantly, providing a dramatically reduction in the size of the output filter (by an order of magnitude). The transformer has now become the largest single component in the power stage, and reducing its size is very important. The transformer frequency dependent core losses are now found to be a major contributing factor in limiting the operating frequency of the supply.

Part 1 of this section highlights the improvements in ferrite material properties for higher frequency operation. The standard 3C8 with its much improved version the 3C85 are discussed. However, the section concentrates on the new high frequency power ferrite, 3F3. This material features very low switching losses at higher frequencies, allowing the process of miniaturisation to be advanced yet further.

The popular ETD system shown in Fig.1 is also outlined, and used as an example to compare the losses obtained with the above three materials

In Part 2, the new EFD (Efficient Flat Design) core shape is introduced. These cores have been specifically designed for applications where a very low build height is important, such as the on-card d.c.- d.c. converters used in distributed power systems.

Circuit topologies suitable for high frequency applications are considered in the final part. Optimum winding designs for the high frequency transformer, which maximise the throughput power of the material are described.

PART 1: Improved magnetic materials

The ETD core system

The very widely used ETD core shape is shown in Fig.1, which also outlines and the method of coil-former assembly. The ETD range meets IEC standardisation, and is based on an E-core shape with a round centre pole. This permits easy winding especially for copper foil and stranded wire. The ETD system includes coil-formers into which the cores are clipped for quick, simple and reliable assembly. The coil-formers are designed for automatic winding and enable conformance with all standard safety specifications including UL.

ETD cores are suitable for a wide range of transformer and inductor designs, and are very commonly featured in off-line power supply transformers, because the ease of winding allows insulation and creepage specifications to be met.

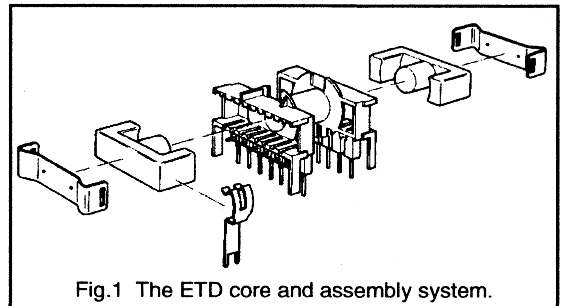


Fig.1 The ETD core and assembly system.

Core materials

Three types of ferrite core material are compared. The standard 3C8 which is applicable for 50kHz use, the popular 3C85 which is usable at up to 200kHz, and the new high frequency core material 3F3, which has been optimised for use from 200kHz upwards.

The throughput power of a ferrite transformer is, neglecting core losses, directly proportional to (amongst other things) the operating frequency and the cross-sectional area of the core. Hence for a given core, an increase in the operating frequency raises the throughput power, or for a given power requirement, raising the frequency allows smaller cores and higher power densities. This is expressed by the following equation:-

$$P_{th} = W_d \times C_d \times f \times B$$

Where W_d is the winding parameter, C_d is the core design parameter, f is the switching frequency and B is the induction (flux density) in Tesla.

Unfortunately, the core losses are also frequency dependent, and increasing frequency can substantially increase the core losses. Thus an increase in the core volume is required to maintain the desired power throughput without over-heating the core. This means the transformer bulk in a higher frequency supply could limit the size reduction target.

The new 3F3 material with low-loss characteristics at high frequencies will reduce this problem, allowing new levels miniaturisation to be obtained. An example of the practical size (and weight) reduction possible by moving to higher operating frequencies is given in Fig.2. In comparison with the 50kHz examples, there is a significant reduction in transformer size when switched at 500kHz, and an even more impressive shrinking of the output inductor when operated at 1MHz.

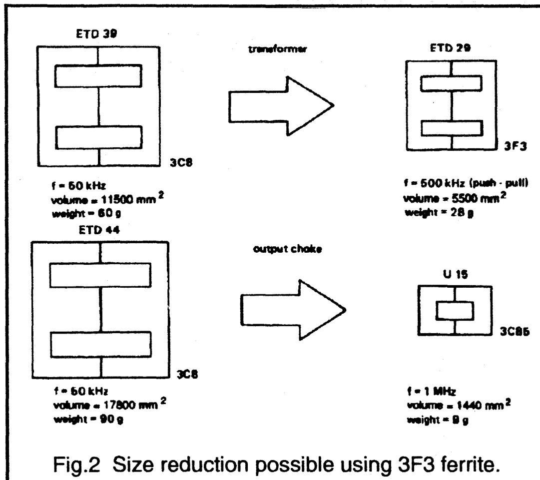


Fig.2 Size reduction possible using 3F3 ferrite.

Note. The size of the output capacitor and inductor required to filter the high frequency output ripple components is greatly reduced - up to 90% smaller, resulting in excellent volume savings and very low ripple outputs.

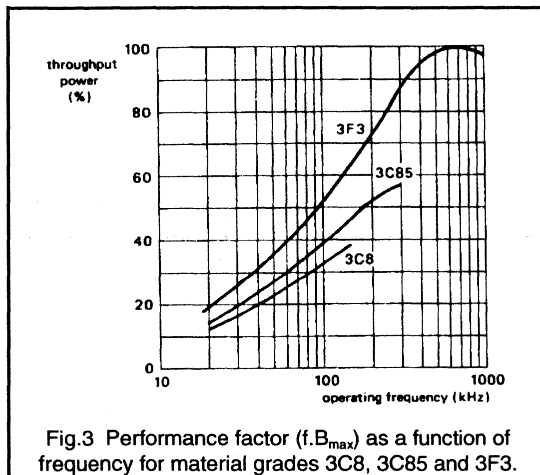


Fig.3 Performance factor ($f.B_{max}$) as a function of frequency for material grades 3C8, 3C85 and 3F3.

The performance factor ($f.B_{max}$) is a measure of the power throughput that a ferrite core can handle at a loss of 200mW/cm^3. This level is considered acceptable for a well designed medium size transformer. The performance factors for the three different material grades 3C8, 3C85 and 3F3 are shown in Fig.3. For frequencies below 100kHz (the approximate transition frequency, f_t) the power throughput is limited by core saturation and there is not much difference between the grades. However for frequencies above 100kHz, core loss is the limitation, which reduces the allowable throughput power level by overheating the core. Therefore, in order to utilise higher frequencies to increase throughput power or reduce core size, it is important that the core losses must first be minimised.

Reducing the losses

There are three main identifiable types of ferrite material losses, namely, hysteresis, eddy current and residual.

Hysterisis loss

This occurs because the induced flux, B lags the driving field H. The B/H graph is a closed loop and hysterisis loss per cycle is proportional to the area of the loop. This loss is expressed as:-

$$P_{hyst} = C_a \times f^x \times B_{pk}{}^y$$

Where C_a is a constant, B_{pk} is the peak flux density, f is the frequency with x and y experimentally derived values.

Eddy current loss

This loss is caused by energy from the magnetic flux, B setting up small currents in the ferrite which causes heat dissipation. The energy lost is represented by:-

$$P_{ec} = \frac{C_b \times f^2 \times B_{pk}^2 \times A_e}{\sigma}$$

C_b is a constant, A_e is the effective cross-sectional core area and σ is the material resistivity.

Residual/Resonant loss

Residual losses are due to the reversal of the orientation of magnetic domains in the material at high frequencies. When the driving frequency is in resonance with the natural frequency at which the magnetic domains flip, there is a large peak in the power absorption. This gives:-

$$P_{res} = C_c \times f \times B_{pk}^2 \times \frac{\tan\delta}{\delta}$$

where

$$\tan\delta = loss\ angle = \frac{\mu''}{\mu'} \qquad \mu = \mu' + j\mu''$$

Comparison of different materials

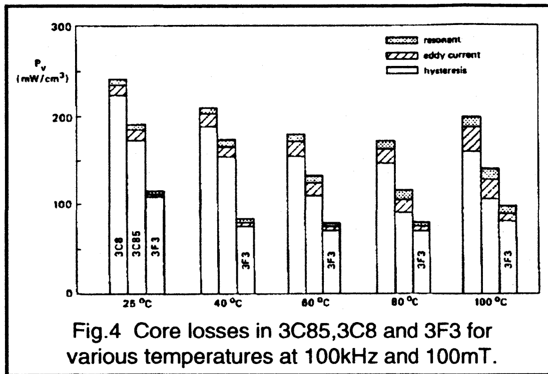


Fig.4 Core losses in 3C85,3C8 and 3F3 for various temperatures at 100kHz and 100mT.

These losses (in mW/cm^3) are now presented for the three material grades in a partitioned form. These are given under various operating of temperature for two different operating conditions. Fig.4 shows performance at 100kHz and a peak flux density of 100mT, which is typical for the 3C8 and 3C85 materials. The hysteresis loss is clearly dominant at this frequency. Inspection reveals a reasonable loss reduction when comparing 3C85 to the cheaper 3C8 grade. More significantly however, even at this lower frequency the new 3F3 grade can be seen to offer substantial loss reduction compared to 3C85 (especially at lower operating temperatures).

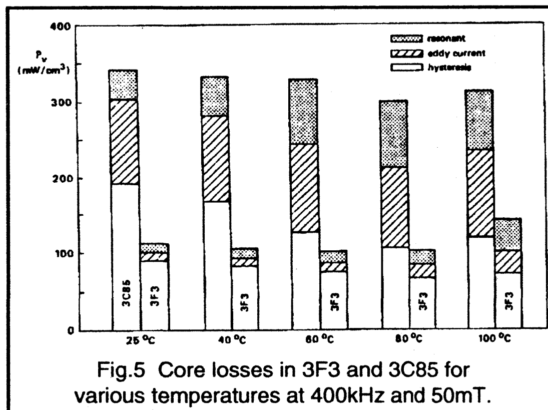


Fig.5 Core losses in 3F3 and 3C85 for various temperatures at 400kHz and 50mT.

At higher operating frequencies well above 100kHz, eddy currents and residual losses are far more dominant. Fig.5 gives the values for 400kHz and 50mT high frequency operation. This shows the superiority of the 3F3 material, offering significant reductions (60% vs 3C85) in all magnitudes, particularly in the eddy currents and residual losses.

Fig.6 gives a comparison of the peak operating flux density versus frequency at a core loss of 200mW/cm^3 for each grade. This shows that the maximum allowable operating frequency for 3F3 is always higher than for the other two types, hence, making it much more suitable for miniaturisation purposes. For example, at 100mT, 3F3 can operate at 280kHz, compared to 170kHz for 3C85 and 100kHz for 3C8.

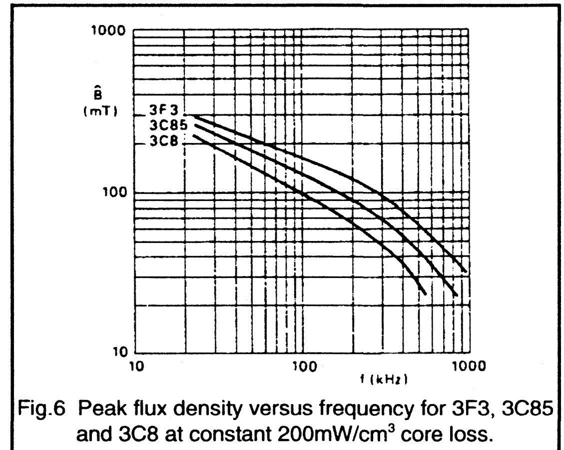


Fig.6 Peak flux density versus frequency for 3F3, 3C85 and 3C8 at constant 200mW/cm^3 core loss.

Fig.7 compares the three types of core material in terms of complex permeabilities μ' and μ" over the frequency range 1 to 10 MHz, at very low flux density levels of < 0.1 mT. It can be seen that the resonant loss peaks at a higher frequency for 3F3, producing much lower high frequency residual losses right up to 1MHz.

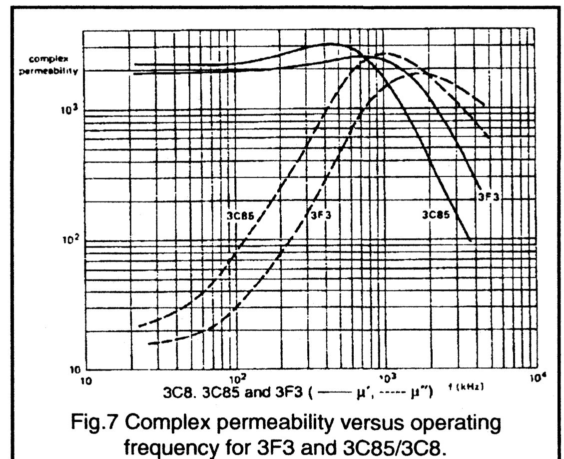


Fig.7 Complex permeability versus operating frequency for 3F3 and 3C85/3C8.

Material	3C8		3C85			3F3		
B_{sat} (mT) at f = 25kHz H = 250A/m	≥ 320		≥ 320			≥ 320		
Core type	A_L ± 25% nH/N²	P_V Watts	A_L ± 25% nH/N²	P_V Watts	P_V Watts	A_L ± 25% nH/N²	P_V Watts	P_V Watts
f	10kHz	25kHz	10kHz	25kHz	100kHz	10kHz	100kHz	400kHz
B	0.1mT	200mT	0.1mT	200mT	100mT	0.1mT	100mT	50mT
ETD29	-	-	2100	≤ 0.8	≤ 1.0	1900	≤ 0.6	≤ 1.0
ETD34	2500	≤ 1.6	2500	≤ 1.1	≤ 1.3	2300	≤ 0.85	≤ 1.5
ETD39	2800	≤ 2.2	2800	≤ 1.6	≤ 1.9	2600	≤ 1.3	≤ 2.3
ETD44	3500	≤ 3.6	3500	≤ 2.5	≤ 3.0	3200	≤ 2.0	≤ 3.7
ETD49	4000	≤ 4.6	4000	≤ 3.4	≤ 4.0	3600	≤ 2.6	≤ 5.2

Table 1. Comparison of material properties for the ETD range

Comparison of material grade properties for the ETD range

The following values shown in Table 1 are for a core set under power conditions at an operating temperature of 100˚C.

3F3 offers a major improvement over existing ferrites for SMPS transformers. With reduced losses across the entire frequency range (but most markedly at 400kHz and higher) 3F3 enables significant reductions in core volume while still maintaining the desired power throughput.

As well as the ETD range, 3F3 is also available in the following shapes:-

- RM core
- P core
- EP core
- EF core
- E core
- ring core
- new EFD core

The new EFD core system which also offers size reduction capabilities shall now be described.

PART 2: The EFD core (Economic flat design)

The newly developed EFD power transformer core system shown in Fig.8 offers a further significant advance in circuit miniaturisation. Their low build height and high throughput power density make them ideally suited to applications where space is a premium.

One such application is with distributed power systems, which is becoming an increasingly popular method of power conversion, especially in the telecommunication and EDP market. Such power-systems convert a mains voltage into an unregulated voltage of about 44 to 80V d.c. This is then fed to individual sub-units, where d.c.- d.c. converters produce the required stabilised voltages. These converters are usually mounted on PCBs which in modern systems, are stacked close together to save space. The d.c.- d.c. converter, therefore, has to be designed with a very low build height.

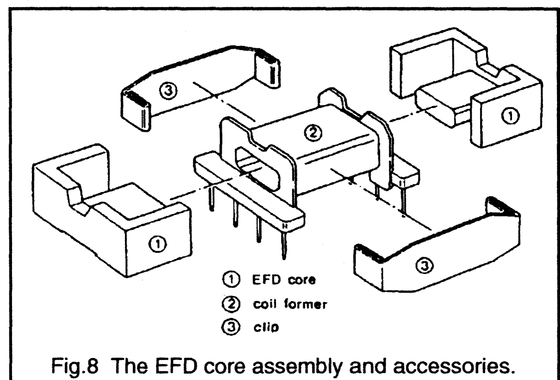


Fig.8 The EFD core assembly and accessories.

The low-profile design

The EFD core offers significant reduction in transformer core height. The ETD core combine extreme flatness with a very high throughput power-density. The range consists

of four core assemblies complemented by a complete range of accessories. It is planned that the EFD outline will become a new European standard in d.c. - d.c. power transformer design.

The four core assemblies have a maximum finished height of 8mm, 10mm or 12.5mm. The type numbers are:-

- 8mm height - EFD 15/8/5
- 10mm height - EFD 20/10/7
- 12.5mm height - EFD 25/13/9 and EFD 30/15/9

Fig.9 shows that the EFD range has a lower build height than any other existing low profile design with the same magnetic volume.

Integrated product design

Because there is no room in a closely packed PCB for heavily built coil formers, they must be as small and light as possible. For this reason high quality thermo-setting plastics are used, This ensures that the connecting pins in the base remain positioned correctly.

To ensure suitability for winding equipment the connecting pins have been designed with a square base, saving time in wire terminating. To allow thick wire or copper foil windings to be easily lead out, both core and coil former have a cut-out at the top (see Fig.8).

To increase efficiency and reduce size, the ferrite core has been designed with the centre pole symmetrically positioned within the wound coil former. This is clearly shown in the cross-sectional view in Fig.10.

Because of this, the full winding area can be used, resulting in an extremely flat design which is ideally suited for surface-mounting technology (SMT). SMT designs are already under consideration.

Maximising throughput power-density

Besides their extreme flatness, the most important feature of the EFD transformer is the very high throughput power density. This is especially true when the core is manufactured from the high-frequency low loss 3F3 material, which was described in the previous section. Combining EFD with 3F3 can provide throughput power densities (in terms of transformer volume) between 10 and 20 W/cm^3. Furthermore, with a usable frequency range from the 100kHz to 1MHz, the EFD transformer will cover most applications.

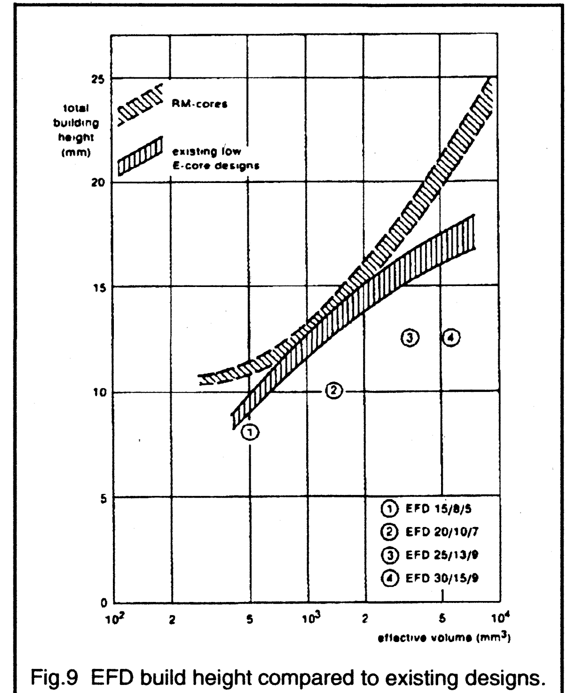


Fig.9 EFD build height compared to existing designs.

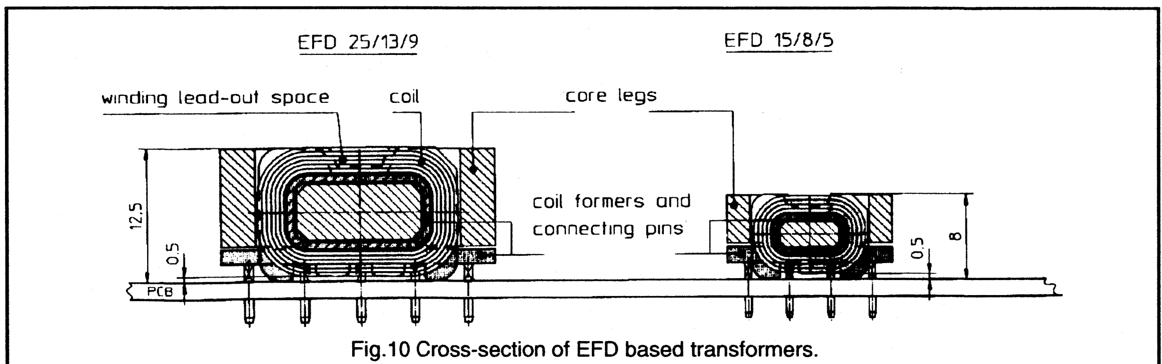


Fig.10 Cross-section of EFD based transformers.

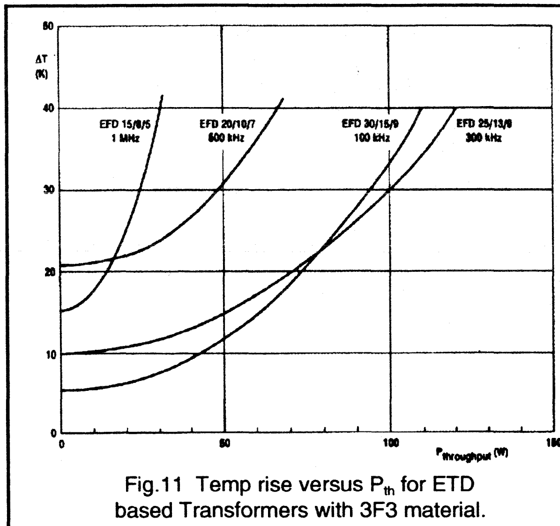


Fig.11 Temp rise versus P_{th} for ETD based Transformers with 3F3 material.

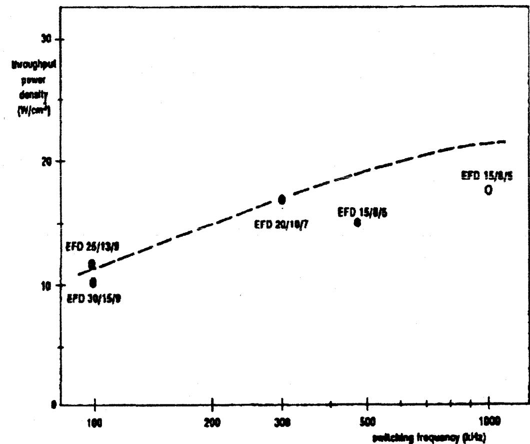


Fig.12 P_{th} for forward mode transformers based on EFD core with 3F3 material.

As described earlier, high frequency transformer design (above 100kHz) is mainly limited by the temperature rise, caused by heat dissipation from the high frequency core losses as well as the power dissipation in the windings themselves. So the extent of transformer miniaturisation at high frequencies is limited by this rise in temperature (The curie temperature of a typical power ferrite material is around 200˚C). As a general rule, maximum transformer efficiency is reached when about 40% of the loss is in the ferrite core, and 60% in the windings. The temperature rise for a range of throughput powers for transformers based on the EFD range in 3F3 material is shown in Fig.11

In order to optimise upon the core dimensions and winding area, a sophisticated computer aided design (CAD) model of a d.c. - d.c. forward mode converter was used. This predicted the temperature rise of the transformer as a function of throughput power. The following parameters were assumed:-

Ferrite core - 3F3.

V_{in} = 44V to 80V; V_{out} = 5V, +12V and -12V.

T_{amb} = 60˚C; T_{rise} = 40˚C.

Primary - Cu wire; Secondary - Cu foil.

(Split sandwiched winding with 2 screens).

The CAD program was used to find an optimised design for the EFD transformer at well chosen frequency bands. The dotted line in Fig.12 indicates the theoretical result derived from the CAD model. This shows in practice how well the EFD range approximates to the ideal model. The open circle for EFD 15/8/5 in Fig.12 indicates the maximum optimal switching frequency.

From these results the range was grouped, depending upon core size into their most optimal frequency bands.

- 100 to 300kHz - EFD 30/15/9 and EFD 25/13/9.
- 300 to 500kHz - EFD 20/10/7.
- 500kHz to 1MHz - EFD 15/8/5.

These are the recommended frequency ranges for each EFD type. The transformers can operate outsides these ranges, but at a reduced efficiency, since the ratio of their core to winding areas would be less than ideal. Table 2 lists the power throughput at certain frequencies for each EFD core.

Core type	100 kHz	300kHz	500kHz	1MHz
EFD 30/15/9	90 - 100 W	110-140W	--	--
EFD 25/13/9	70 - 85 W	90 - 120 W	--	--
EFD 20/10/7	--	50 - 65 W	55 - 70 W	--
EFD 15/8/5	--	--	20 - 30 W	25 - 35 W

Table 2 Power handling capacity for EFD range.

Valid for single-ended forward d.c. - d.c. converter (V_{in} = 60V; V_{out} = 5V)

Typical EFD throughput power curves given in Fig.13 show the performance of the low loss 3F3 material as well as 3C85. These results were confirmed from measurements taken during tests on EFD cores in a transformer testing set up. As expected these show that, especially above 300kHz, the 3F3 (compared to 3C85) significantly improves throughput power.

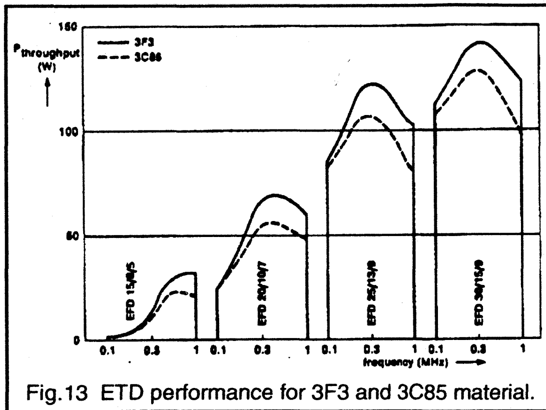


Fig.13 ETD performance for 3F3 and 3C85 material.

PART 3: Applications

Circuit (transformer) configurations

Forward, flyback and push-pull circuit configurations have been used successfully for many different SMPS applications. This includes mains-isolated square-wave switching over the frequency range 20-100kHz, and with output powers up to 200W. Recent transformer designs has been developed to minimise the effects of leakage inductance and stray capacitance upon these circuits. The influences of the transformer characteristics on the choice of circuit configuration for higher switching frequency applications are now discussed.

The flyback converter

The flyback converter shown in Fig.14 has leakage inductance between the primary and secondary windings which delays the transfer of power when the primary power transistor turns off. For the example waveforms shown in Fig.14, the delay lasts for 600ns. During this time, power is returned to the d.c. supply. The circulating power increases with the switching frequency, and in this case would produce 50W at 1MHz. This tends to limit the maximum operating frequency for flyback converters.

The forward converter

The power transistor in the forward converter shown in Fig.15 normally has a snubber network (and stray circuit capacitance) which protects the transistor at turn-off. This is necessary because the energy stored in the leakage inductance between the primary and secondary windings would produce a large voltage spike at transistor turn-off.

At transistor turn-on the energy stored in the capacitance is discharged and dissipated. For the example waveforms given in Fig.15, this would be 7.5W at a switching frequency of 1MHz. Furthermore, as in the flyback converter, the circulating magnetising power can also be as high as 50W at 1MHz, hence reducing the efficiency of the transformer. These characteristics limit the maximum frequency at which forward converters can be usefully applied.

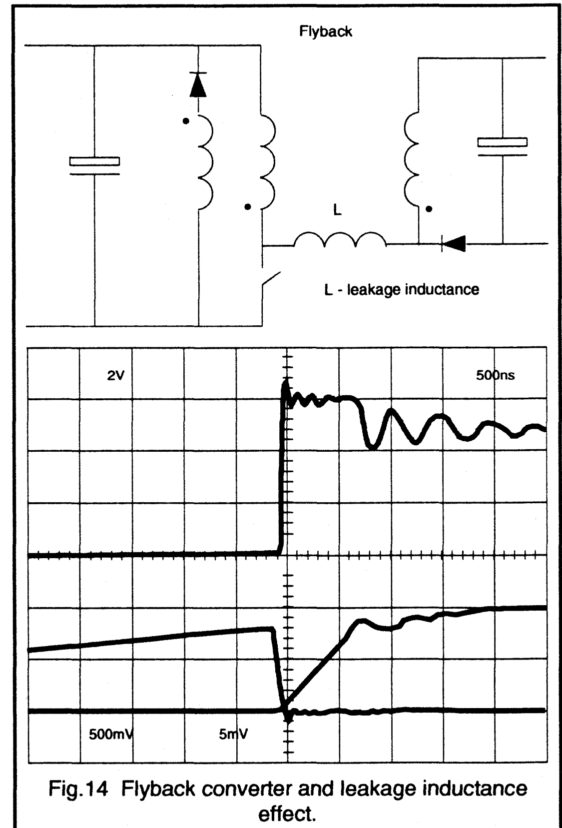


Fig.14 Flyback converter and leakage inductance effect.

Centre-tapped push-pull converter

The centre-tapped push-pull circuit configuration given in Fig.16 uses magnetic B/H loop symmetry when driving the transformer. Therefore, when either transistor is turned off, the magnetising current is circulated around the secondary diodes, thereby reducing energy recovery problems or the need for voltage clamping.

However, the transformer must be correctly "flux balanced" by monitoring the current in the transistors to prevent transformer saturation and subsequent transistor failure.

The drain current and voltage waveforms resulting from two examples of push-pull transformer winding construction are also shown in Fig.16 . In Fig.16(b) (most serious case) the leakage inductance has distorted the waveforms. In Fig.16(c) it is the circuit capacitance which produces the distortion. These distortions mean that the transistor current

sense waveforms must be adequately filtered, so that the control circuit can vary mark/space correctly and prevent transformer saturation.

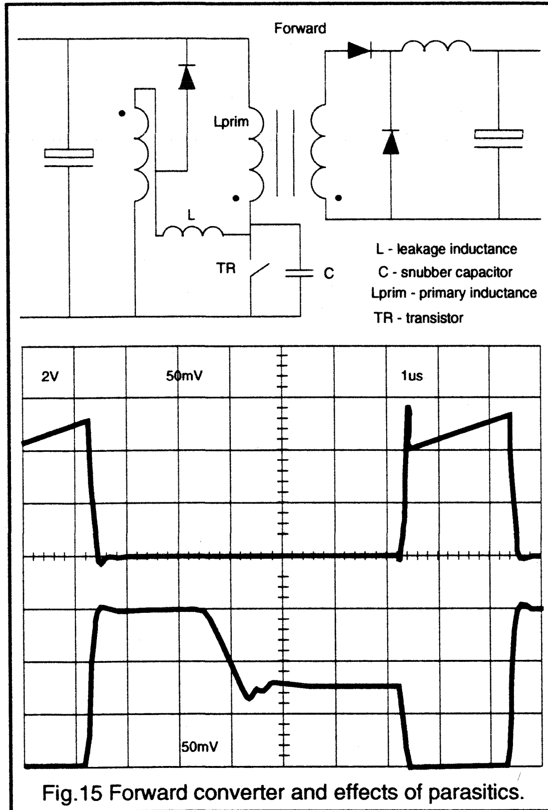
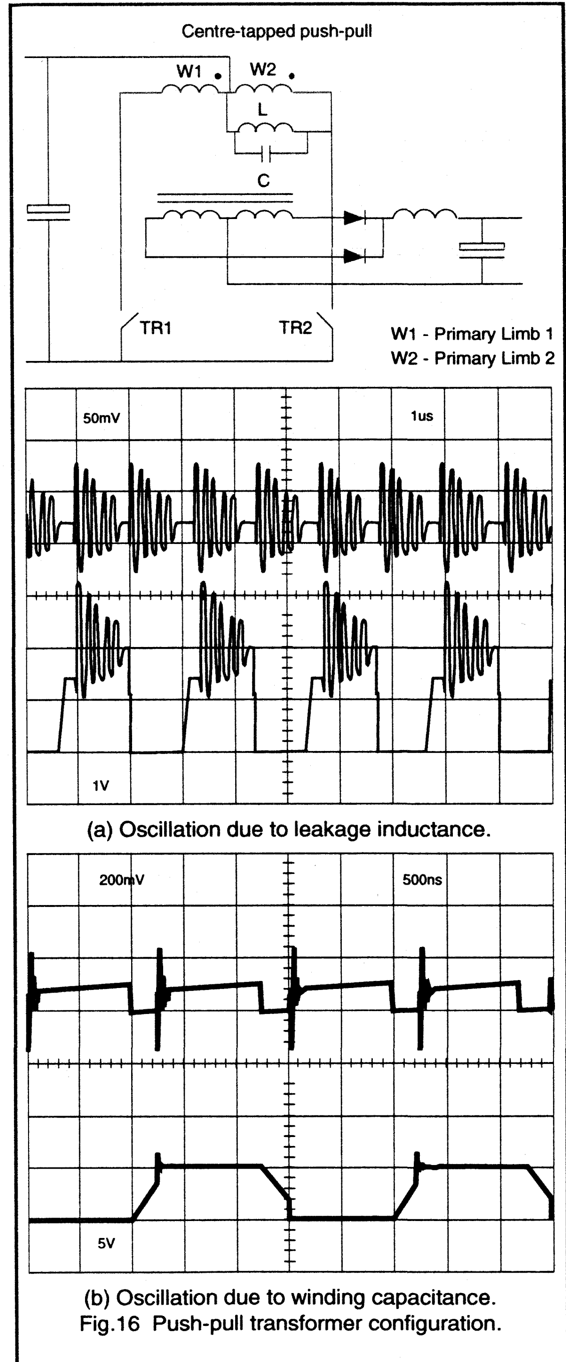


Fig.15 Forward converter and effects of parasitics.

As the switching frequency is increased, the accuracy of the current balancing information is reduced by the action of the filtering and there maybe a point at which this becomes unacceptable. The filter itself, is also dissipative and will also produce a high frequency loss.

The half-bridge converter

The half-bridge push-pull transformer shown in Fig.17 is inherently self-balancing. Standard winding methods for transformer construction using this configuration are possible at frequencies up to around 1MHz. Fig.17 also gives waveforms example for the half-bridge transformer. This design allows the most flexibility when choosing a particular switching frequency.



(a) Oscillation due to leakage inductance.

(b) Oscillation due to winding capacitance.

Fig.16 Push-pull transformer configuration.

Switching frequency

When designing a transformer and calculating the core loss, the exponent for frequency in the hysteresis loss equation is assumed to be constant at all frequencies. Only the fundamental is considered significant compared to all other harmonics of the square wave. This is a reasonable approximation to make from 20kHz to 100kHz because the contribution of eddy losses and resonant losses to the overall core loss is negligible (see Fig.4).

As the frequency increases to 1MHz and beyond, the resonant and eddy current losses contribute proportionally more to the overall core loss. This means that the harmonics of a 1MHz square wave have more significance in determining the core-loss than those at 100kHz. When the mark/space is reduced, the harmonics increase, and the loss will increase proportionally. This effectively limits the upper frequency of a fixed frequency square-wave, mark/space controlled power supply. However, as outlined new materials such as 3F3 have been specially developed to keep these high frequency transformer losses as low as possible.

Transformer construction

In the half-bridge push-pull configuration of Fig.17, during the period that the two primary transistors are off, there is zero volts across the secondary winding. Therefore, the secondary diodes are both conducting and share the choke current. The primary side should also have zero volts across it, but it rings because of the stray capacitance and leakage inductance between the primary and the secondary windings (see waveform of Fig.17). At 500kHz, using an ETD29 or an EFD20 core, for example, a 1+1 copper strip secondary winding is suitable for providing an output of 5V. This is preferable to using more turns for the secondary winding because the leakage inductance and the amplitude of the ringing during the period that the MOSFETs are off is minimised. Reducing the ringing is of vital importance for the following reasons:-

1. It prevents the anti-parallel diode inherent in the upper MOSFET switch from conducting when the lower transistor is turned on. This will increase the MOSFET dV/dt rating typically by a factor 10, allowing the switching speed to be maximised and the switching losses to be reduced.

2. For low voltage outputs, the ringing will only be slightly reduced by the 1+1 construction. However, the core losses increase significantly at the actual frequency of the ringing (5-10MHz). Hence, any reduction in the ringing amplitude will be beneficial to core loss.

To further optimise the operation of the transformer, and reduce the ringing, the output clamping diodes should be operated with the minimum of secondary leakage inductance and mounted physically close to the transformer.

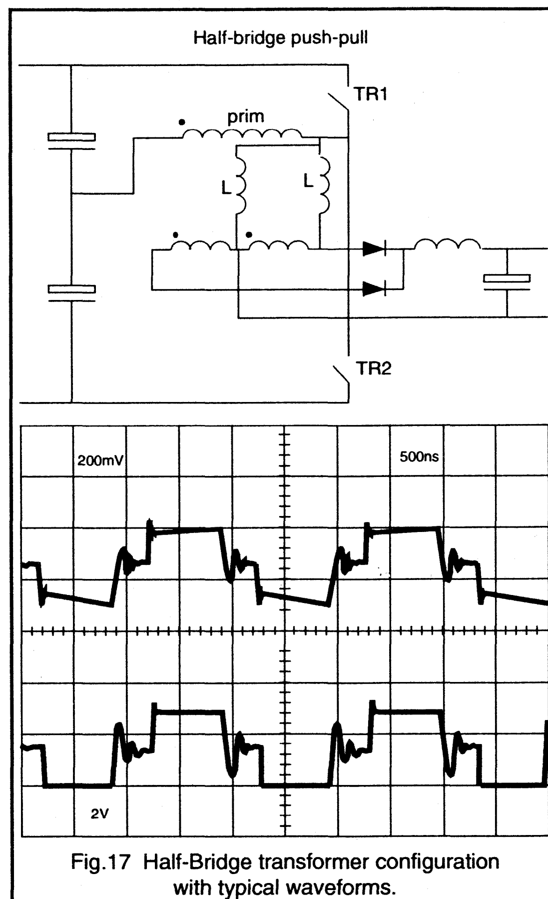


Fig.17 Half-Bridge transformer configuration with typical waveforms.

Conclusions

To advance the trend towards SMPS miniaturisation, low-loss ferrites for high frequency have been specially developed. A new ferrite material has been presented, the 3F3, which offers excellent high-frequency, low loss characteristics.

A wide range of power ferrites materials are now available which offer performance/cost optimisation for each application. The particular SMPS application slots for the three ferrites discussed in this paper are summarised as follows:-

- 3C8 for low-cost 20-100kHz frequency range.
- 3C85 for high performance 20-150kHz.
- 3F3 for miniaturised high performance power supplies in the frequency range above 150kHz.

A new type of power core shape, the EFD was also introduced. The use of the EFD core also allows further SMPS miniaturisation by providing extremely low build heights in conjunction with very high throughput power densities. Optimum use of the EFD design can be made if the 3F3 material grade is selected. The EFD system is intended for applications with very low height restrictions, and is ideal for use in the d.c. - d.c. converter designs found in modern distributed power systems.

Different transformer winding configurations were also described (particularly for mains isolated SMPS.) It was found that to obtain the greatest size reduction using the new 3F3 material at very high frequencies, the following application ideas are useful:-

- Use the half-bridge push-pull circuit configuration.
- Minimize the transformer leakage inductance by careful winding construction.
- Minimise the lead-lengths from the transformer to rectifier diodes.

Resonant Power Supplies

2.5.1. An Introduction To Resonant Power Supplies

Whilst many application requirements can be satisfied by the use of conventional switching topologies, their shortcomings, particularly the switching losses in high power / high frequency circuits, are becoming a serious limitation. Some of the problems can be overcome by the use of resonant, or quasi-resonant, converters.

A resonant converter is a switching converter in which the natural resonance between inductors and capacitors is used to shape the current and voltage waveforms.

There are many ways in which inductors, capacitors and switches can be combined to form resonant circuits. Each of the configurations will have advantages and disadvantages in terms of stress placed on the circuit components.

To reduce switching loss, a resonant converter which allows the switching to be performed at zero current and low dI/dt is needed. A range of such circuits can be produced by taking any of the standard converter topologies and replacing the conventional switch with a resonant switch.

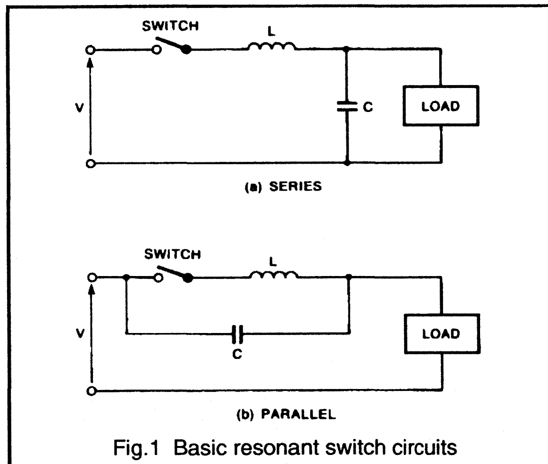


Fig.1 Basic resonant switch circuits

Resonant switch

A resonant switch consists of an active element (the switch) plus an additional inductor, L, and capacitor, C. The values of L and C are chosen so that, during the on time of the switch, the resonant action between them dominates. This ensures that the current through the switch, instead of just increasing linearly and having to be turned off, forms a sinusoid which rises to a peak and falls to zero again.

Two basic resonant switch configurations are shown in Fig.1. Before the switch is closed, C is in a state where it has a small negative charge. With the switch closed, C is discharged into L and then recharged positively. During the recharging extra energy is drawn from the supply to replace that delivered to the load during the previous cylce. With C charged positively, the switch is opened. The energy in C is now transfered to the load, either directly or via the main inductor of the converter. In the process of this transfer, C becomes negatively charged.

Figure 2 shows the three basic SMPS topologies - buck, boost and buck / boost - with both conventional (a) and resonant (b) switches. It should be noted that parasitic inductance and capacitance could form part, or even all, of the components of the resonant network.

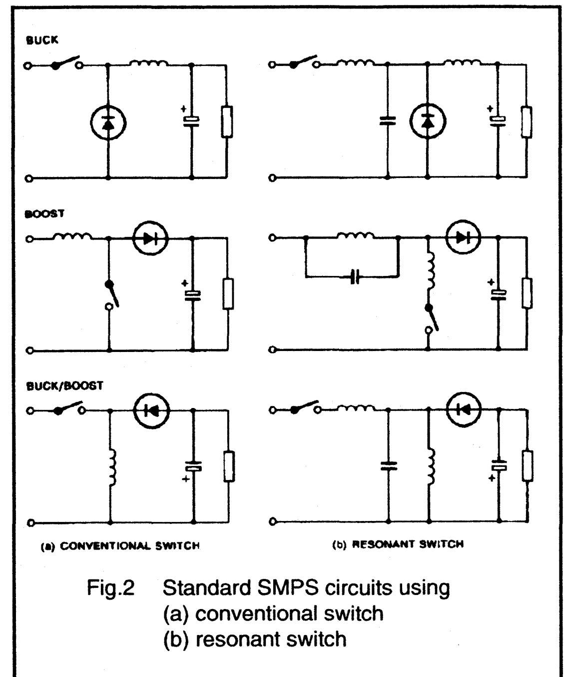


Fig.2 Standard SMPS circuits using
(a) conventional switch
(b) resonant switch

Flyback converter

To show how the resonant switch circuit reduces switching loss we will now consider the operation of the flyback converter, firstly with a conventional switch and then with a resonant switch.

Conventional switch

The basic flyback converter circuit is shown in Fig.3(a). If the transformer is assumed to have negligible leakage inductance it can be replaced by a single equivalent inductor Lm and the circuit becomes as shown in Fig.3(b), which is the same as a buck-boost converter shown in Fig.2.

Before the switch S is closed, a current Io will be flowing in the loop formed by Lm, diode D and the output smoothing capacitor Co. When S closes, voltage Es reverse biases the diode, which switches off and blocks the flow of Io. A current Is then flows via S and Lm. The only limitations on the initial rate of change of current are the stray inductance in the circuit and the switching speed of S. This means that switching current Is rises very quickly, leading to large turn-on losses in S and D.

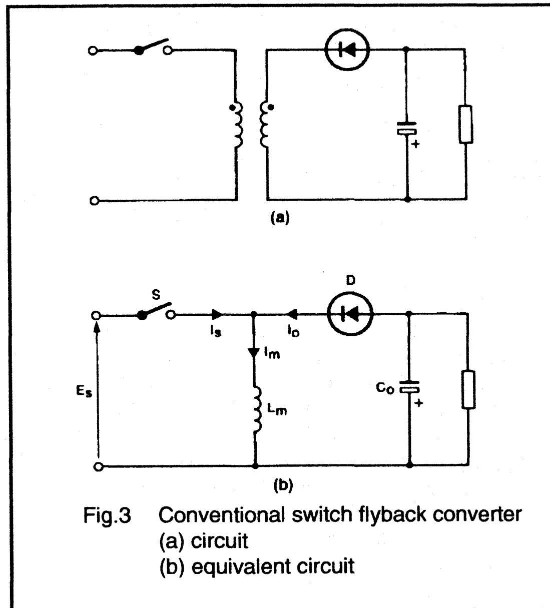


Fig.3 Conventional switch flyback converter
(a) circuit
(b) equivalent circuit

The current Is rises linearly from Io until the switch is forced to reopen. The diode is then no longer reverse biased and the current switches back from Is to Io via D, with Co then acting as a voltage source. The losses in this switching will also be very high due to the high level of Is and the rapid application of the off-state voltage. Io now falls linearly, delivering a charging current to Co, until the switch closes again.

Figure 4 shows the current waveforms for Io and Is and the current in inductor Lm.

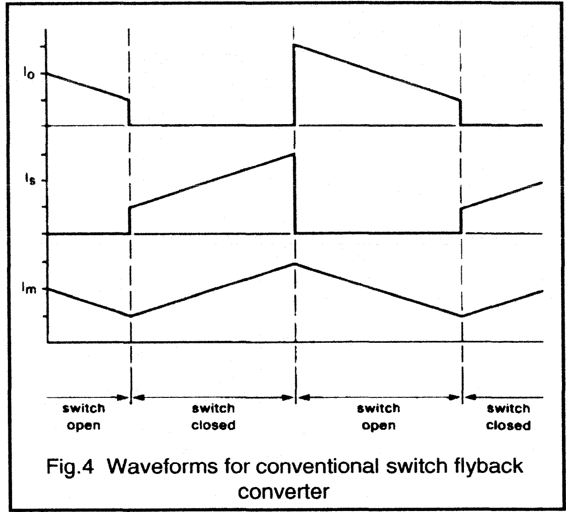


Fig.4 Waveforms for conventional switch flyback converter

Resonant switch

The resonant switch flyback converter circuit is shown in Fig.5(a). The equivalent circuit (Fig.5 (b)) is the same as that for the conventional switch except for the addition of the inductor La and capacitor Ca whose values are very much less than those of Lm and Co respectively.

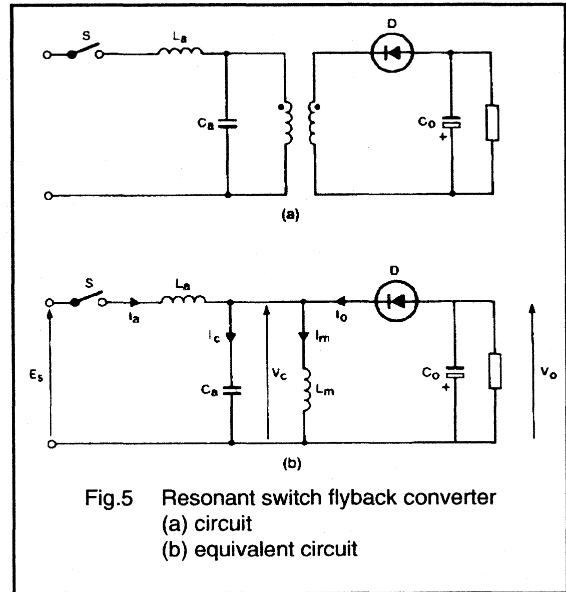


Fig.5 Resonant switch flyback converter
(a) circuit
(b) equivalent circuit

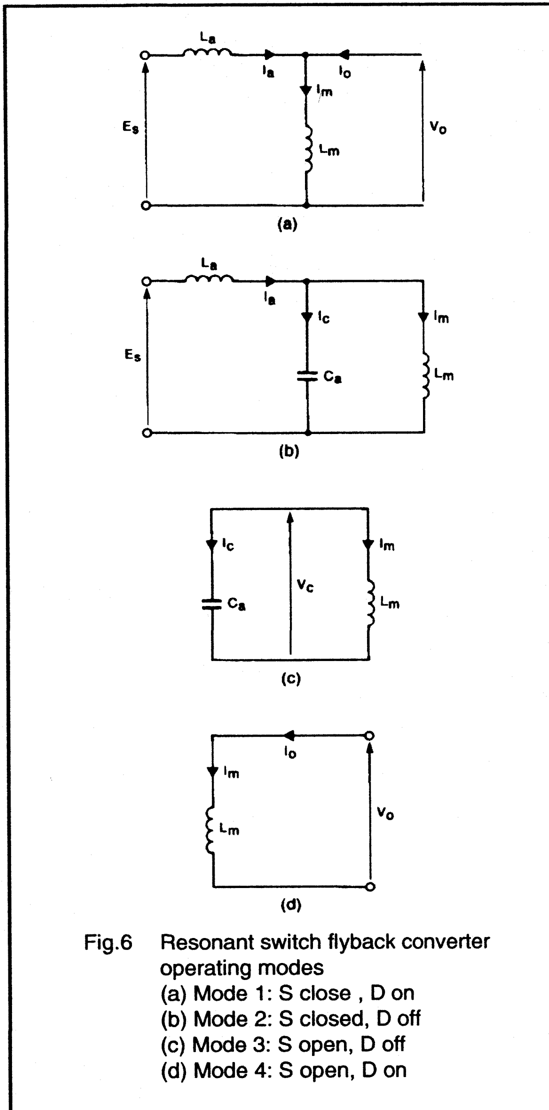


Fig.6 Resonant switch flyback converter operating modes
(a) Mode 1: S close , D on
(b) Mode 2: S closed, D off
(c) Mode 3: S open, D off
(d) Mode 4: S open, D on

If it is assumed that the switch is closed before the current in Lm has fallen to zero, then the initial equivalent circuit will be as shown in Fig.6(a). The rate of rise of current in S is determined by the value of La which, although small, is much larger than the stray inductance that limits current rise in a conventional switch. Turn-on losses are thus significantly reduced. Co, being much larger than Ca, acts as a voltage source (Vo) preventing current from flowing into Ca and maintaining a constant rate of change of current in Lm. Ia will increase linearly until it equals Im at which time Io is zero and diode D turns off.

With D turned off, the equivalent circuit becomes as shown in Fig.6(b). The resonant circuit, La, Ca and Lm, causes Ia to increase sinusoidally to a peak and then fall back to zero. S can then be opened again with very low losses.

With the switch open, the circuit is as shown in Fig.6(c). The resonant action between Ca and Lm causes energy to be transferred from the capacitor to the inductor. Vc will fall, passing through zero as Im reaches a peak, and then will increase in the opposite direction until it exceeds Vo. At which point D becomes forward biased, so it will turn on.

As D turns on (Fig.6(d)) the voltage across Ca becomes clamped and Im now flows into Co. Im falls linearly until the switch is closed again and the cycle repeats.

Voltage and current waveforms for a complete cycle of operation are shown in Fig.7.

From the description of operation it can be seen that the reduced switching losses result from:

- La acting as a di/dt limiter at switch on
- The resonant circuit La, Lm and Ca ensuring that the current is zero at turn-off

These factors combine to allow the switching devices to be operated at higher frequencies and power levels than was previously possible.

Circuit design

Correct operation of a resonant switch converter depends on the choice of suitable values for the inductors and capacitors. It is not possible to determine these values directly but they can be selected using simple computer models. An example of a model for a resonant switch flyback converter is given below to demonstrate the basic technique that can be used to analyse many different types of resonant circuits. Writing the final computer program will be a simple task for anyone with proramming experience and the model will run relatively quickly on even small personnel computers.

Circuit analysis

Here we analyse the operation of a resonant flyback converter circuit in mathemtical terms, assuming ideal circuit components.

In the equivalent circuit of the flyback converter, Fig.5(b), there are two switching elements S and D and the circuit has four possible modes of operation:

Mode 1	S closed	D on
Mode 2	S closed	D off
Mode 3	S open	D off
Mode 4	S open	D on

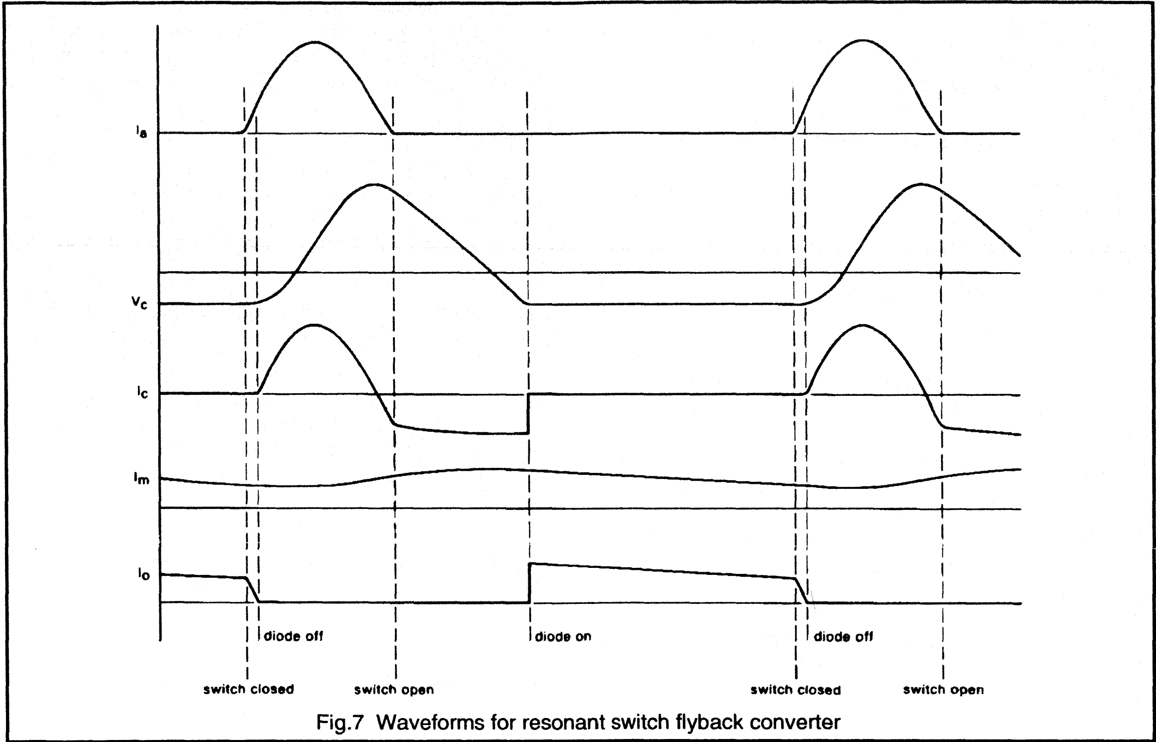


Fig.7 Waveforms for resonant switch flyback converter

Using Laplace analysis of the equivalent circuit for each operating mode, equations can be written for Ia, Ic, Im, Io and Vc.

J and U are the values of, Im and Vc respectively at the start of each operating mode i.e. when t = 0.

Mode 1

Figure 6(a) shows the equivalent circuit when S is closed and D is on. The large output capacitor Co as shown acts as voltage source (Vo).

The equations are:

$$Ia = \frac{Es - U}{La}$$

$$Im = \frac{U}{Lm}.t + J$$

$$Ic = 0$$

$$Vc = U$$

$$Io = Im - Ia$$

Mode 2

Figure 6(b) shows the equivalent circuit when S is closed and D is off.

The equations are:

$$Ia = J + A1.t + \frac{A2 - A1}{\omega 1}.\sin(\omega 1.t)$$

$$Im = J + A1.t + \frac{A3 - A1}{\omega 1}.\sin(\omega 1.t)$$

$$Ic = Ia - Im$$

$$Vc = U + \left(\frac{Lm.(Es - U) - La.U}{La + Lm}\right).(1 - \cos(\omega 1.t))$$

$$Io = 0$$

where,

$$A1 = \frac{Es}{La + Lm}$$

$$A2 = \frac{Es - U}{La}$$

$$A3 = \frac{U}{Lm}$$

$$\omega 1 = \sqrt{\left(\frac{La + Lm}{Lm.Ca.La}\right)}$$

Mode 3

Figure 6(c) shows the equivalent circuit when S is open and D is off.

The equations are:

$$Ia = 0$$

$$Im = J.\cos(\omega 2.t) + \frac{U}{Lm.\omega 2}.\sin(\omega 2.t)$$

$$Ic = -Im$$

$$Vc = U.\cos(\omega 2.t) + \frac{J}{Ca.\omega 2}.\sin(\omega 2.t)$$

$$Io = 0$$

where,

$$\omega 2 = \sqrt{\left(\frac{1}{Lm.Ca}\right)}$$

Mode 4

Figure 6(d) shows the equivalent circuit when S is open and D is on.

The equations are

$$Ia = 0$$

$$Im = J + \frac{U}{Lm}.t$$

$$Ic = 0$$

$$Vc = U$$

$$Io = Im$$

Computer simulation

Using the previous equations, it is possible to write a computer program which will simulate the operation of the circuit.

If S is closed before Im falls to zero, then during a complete cycle each of the operating modes occurs only once, in the sequence mode 1 to mode 4.

The first function of the program is to determine the duration of each mode.

Mode 1

The time between the switch turning on and the current Ia reach Im is given by:

$$T1 = \frac{J1.Lm.La}{Lm.(Es - Vo) - U1.La}$$

J1, the initial value of Im chosen by the designer, determines the average output current. U1 is the initial value of Vc. If Im is greater than zero, D will still be on so Vc and therefore U1 will equal Vo.

Mode 2

The duration, T2, of the second mode cannot be found directly and must be determined by numerical methods. T2 ends when Ia falls back to zero, so by successive approximation of t in the mode 2 equation for Ia, it is possible to find T2.

J and U at the start of mode 2, i.e., J2 and U2, are found by solving the mode 1 equations for Im and Vc respectivley at t = T1.

For any given set of circuit values there is a value of J1 above which Ia will not reach zero. This condition has to be detected by the program. Decreasing the value of La or increasing the value of Lm or Ca will allow Ia to reach zero.

Mode 3

Mode 3 operation ends when Vc = Vo. The duration, T3, is given by:

$$T3 = \frac{1}{\omega}2.\left\{\cos^{-1}\left(\frac{Vo}{\sqrt{U3^2 + A4^2}}\right) - \tan^{-1}\left(\frac{A4}{U3}\right)\right\}$$

where,

$$A4 = \frac{J3}{Ca.\omega 2}$$

and J3 and U3 are the values of Im and Vc respectively at the start of mode 3.

Mode 4

If the circuit operation is stable then the value of Im, when S is again closed, will equal J1 and the duration of the mode will be

$$T4 = \frac{Lm.(J4 - J1)}{U4}$$

Where J4 and U4 are the values of Im and Vc at the start of mode 4.

Calculation of Io and Vs

Having found the durations of the four modes, the average output current in D can be calculated, from:

$$Io(av) = \frac{T4.(J4 + J1) + T1.J1}{2.(T1 + T2 + T3 + T4)}$$

Peak, RMS and average values of the current in S (Ia) can be determined by numerical analysis during modes 1 and 2. The voltage across S is given by

$V_S = E_S - V_C$

These values will be needed when the components S and D are chosen.

Conclusions

Resonant combinations of inductors and capacitors can be used to shape the current and voltage waveforms in switching converters. This shaping can be used to:

- reduce RFI and EMI,
- eliminate the effects of parasitic inductance and capacitance,
- introduce a degree of self limiting under fault conditions,
- reduce switching losses.

The resonant switch configuration is one way of reducing switching losses in the main active device. It can be adapted for use in all the standard square wave circuit topologies and with all device types.

Although the analysis of resonant circuits is more complex than the analysis of square wave circuits, it is still straightforward if the operation of the circuit is broken down into its different modes. Such an analysis will yield a set of equations which can be combined into a computer program, to produce a model of the system which can be run relatively quickly on even small computers.

2.5.2. Resonant Power Supply Converters - The Solution For Mains Pollution Problems

Many switch mode power supplies which operate directly from the mains supply, use an electrolytic buffer capacitor, after the bridge rectifier, to smooth the 100/120 Hz ripple on the DC supply to the switching circuit. This capacitive input filter causes mains pollution by introducing harmonic currents and therefore cannot be used in supplies with output powers above 165W. (TV, IEC norm 555-2, part 2: Harmonics, sub clause 4.2).

The smoothing capacitor can be charged only when the mains voltage is greater than the DC voltage. Therefore the input current will take the form of high amplitude, short duration pulses. For comparison, the load current for a 220W resistive load (an RMS current of 1A for 220V mains/line) and the load current for a 220W rectifier with capacitive input buffer are shown in Fig. 1.

The peak value of the current with the capacitor load is 5 times higher than for the resistive load, while the RMS current is doubled. It is understandable that the electricity supply authorities do not like this kind of load, because it results in high levels of harmonic current and a power factor below 0.5. It is, therefore, necessary to find alternative methods of generating a smooth DC voltage from the mains.

The PRE-CONVERTER switched mode supply is one possible solution. Such a converter can operate from the unsmoothed rectified mains/line voltage and can produce a DC voltage with only a small 100/120 Hz ripple. By adding a HF transformer it is possible to produce any value of DC voltage and provide isolation if necessary.

By proper frequency modulation of the pre-converter, the input current can be made sinusoidal and in-phase with the voltage. The mains/line now 'sees' a resistive load, the harmonic distortion will be reduced to very low levels and the power factor will be close to 1.

A pre-converter has to be able to operate from input voltages between zero (at the zero crossings) and the peak value of mains/line voltage and still give a constant output voltage. The SMPS converter that can fulfil these conditions is the 'flyback' or 'ringing' choke converter. This SMPS converter has the boost and buck properties needed by a pre-converter. However, the possibility of stability problems under 'no load' operation and its moderate conversion efficiency, means that this converter is not the most attractive solution for this application.

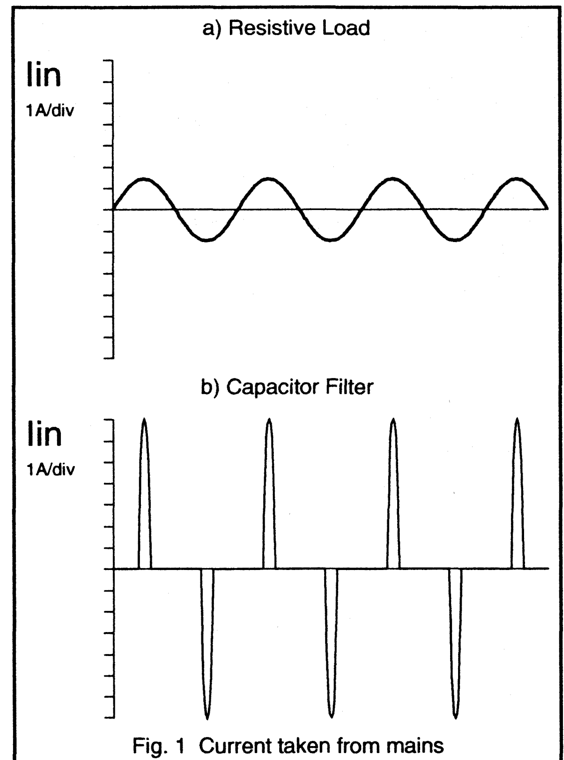


Fig. 1 Current taken from mains

The RESONANT POWER SUPPLY (RPS) has the right properties for pre-converter systems. The boost and buck properties of a resonant L-C circuit around its resonant frequency are well known. In principle any current can be boosted up to any voltage for a PARALLEL RESONANT L-C circuit. Furthermore, the current and voltage wave forms in a resonant converter are more or less sinusoidal, resulting in a good conversion efficiency and there are no stability problems at no load operating conditions.

Resonant pre-converter circuits

There are two basic resonant power supply (RPS) principles that can be considered, namely:

- The SERIES RESONANT POWER SUPPLY (SRPS), where a series resonant L-C circuit determines the no load operation cycle time. The output power increases with increasing operation cycle time (thus with decreasing operation frequency).

- The PARALLEL RESONANT POWER SUPPLY (PRPS), where a parallel resonant L-C circuit determines the no load operation cycle time. The output power increases with decreasing operation cycle time (thus with increasing operation frequency).

The basic SRPS converter circuit

A basic SRPS converter topology is shown in Fig. 2. For simplicity in the following description, the input voltage Ep is taken to be constant - 310 VDC for the 220VAC mains/line. If the circuit is to appear as a 'resistive' load to the mains, then the output power of the pre-converter has to be proportional to the square of the instantaneous value of Ep. This means that the peak output power of the circuit must be equal to twice the average output power. So a 250W pre-converter has to be delivering 500W when Ep is at its peak.

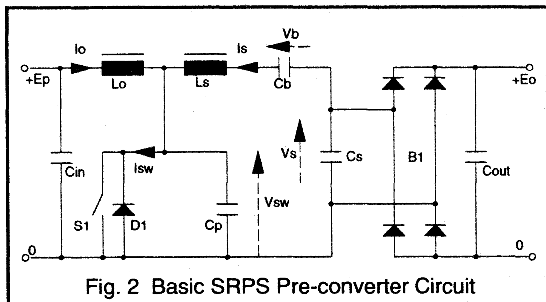


Fig. 2 Basic SRPS Pre-converter Circuit

In Fig. 2, the semiconductor switch S1 has an anti-parallel diode D1 to avoid a negative voltages across S1. Principally, a diode in series with S1 also gives a suitable SRPS pre-converter, but it slightly increases the positive peak voltage on S1 without giving an advantage over the circuit with anti-parallel diode. The lower value of the RMS current in S1 and thus the reduction in its on-state losses is completely cancelled by increased turn-on losses in this device.

Furthermore, stability problems can occur under no load conditions for the circuit with series diode (infinitely small current pulses in S1). The circuit with anti-parallel diode has no infinitely short current pulses under no load conditions, because the positive current in S1 will be preceded by the negative current in D1. As a result, no nett DC current is supplied to the circuit at finite pulse widths.

The input inductance Lo forms the connection between the input voltage and the switch voltage Vsw. A 'SERIES' resonant L-C circuit, consisting of the capacitor Cp (when both S1 and D1 are OFF), the inductance Ls, the DC voltage blocking capacitor Cb and the capacitor Cs (when B1 is OFF), determines the no load operation frequency. The influence of the input inductance Lo can be neglected if its value is several times that of Ls.

A practical SRPS pre-converter for 250W nett output power (500W peak power conversion) can have component values shown in Table 1.

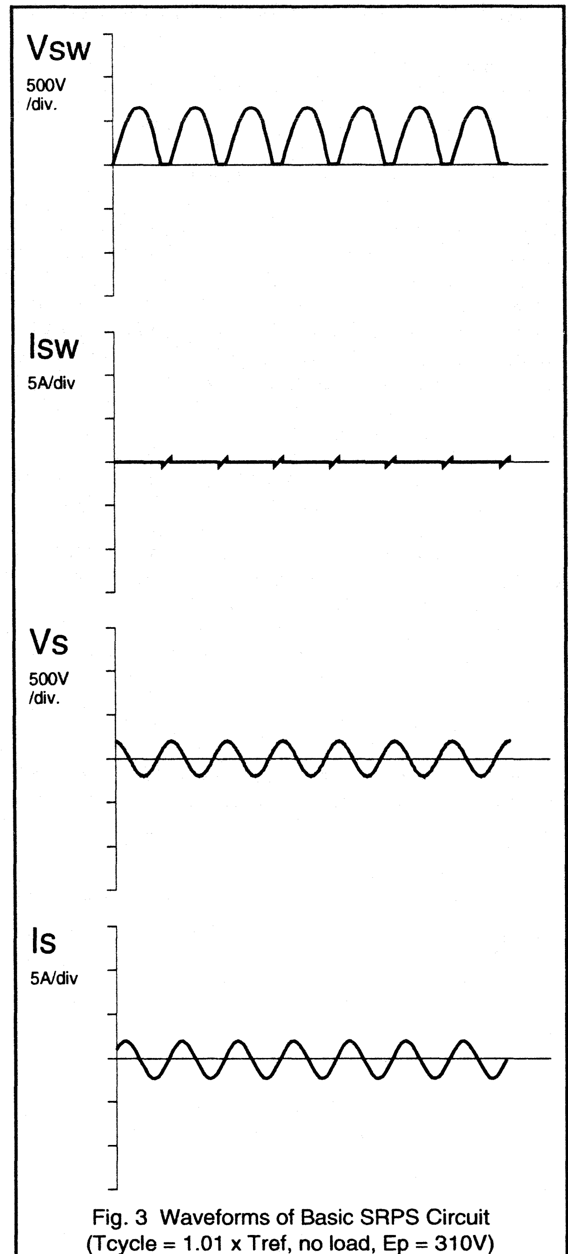


Fig. 3 Waveforms of Basic SRPS Circuit
(Tcycle = 1.01 x Tref, no load, Ep = 310V)

Capacitor Cp changes the voltage waveform across switch S1/D1 from the rectangular shape associated with SMPS converters, to the sinusoidal shape of an SRPS converter.

Lo	4 mH	8 x Ls
Cp	16 nF	Cs / 1.5
Ls	500 µH	
Cs	24 nF	
Cb	360 nF	15 x Cs
Tref	13.3 µs	minimum cycle time

Table 1 Component Values for SRPS circuit

The output rectifier bridge B1 has been connected in parallel with the output capacitor Cs. The whole converter also can be viewed as a parametric amplifier, where the switch S1 or the diode D1 modulate the value of Cp between Cp and infinity, while the output bridge B1 has similar influence on the value of the capacitor Cs. Heavier load means longer conduction of S1/D1 and of B1, so that some automatic frequency adaptation of the SRPS circuit takes place at operation frequencies below the no load resonant frequency. The output power of the SRPS increases with decreasing operation frequency.

Fig. 3 shows time plots of some of the voltages and currents of the basic SRPS circuit for the minimum ON time of S1/D1.

Under no load operation, the voltage Vsw is a pure sine wave superimposed on the input voltage with an amplitude equal to this voltage. The operation cycle time is approximately equal to the series resonant circuit cycle time, Tref, for no load conditions. The voltage Vsw and Vs and the current Is are sine waves with a low harmonic distortion. The input current Io is a low amplitude sine wave and it has no DC component for zero load.

In order to give an impression of the boosting properties of the SRPS converter, the no load voltages and currents for an operation cycle time of 1.25 x Tref are plotted in Fig. 4.

Fig. 3 gives the minimum 'ON' time condition for the S1/D1 switch and thus the minimum output voltage amplitude for a given input voltage. The minimum ratio of the amplitude of Vs and the input voltage Ep, with the component values given earlier, has been found to be:

$$\frac{Vs}{Ep} = 0.7$$

It will be obvious, that the value of the output voltage Eo has to be in excess of the minimum amplitude of Vs. Thus:

$$Eo > 0.7 \times Ep$$

A practical value of Eo has to be about 10% in excess of this minimum value in order to deal with tolerances in component values, thus:

$$Eo > 0.8 \times Ep$$

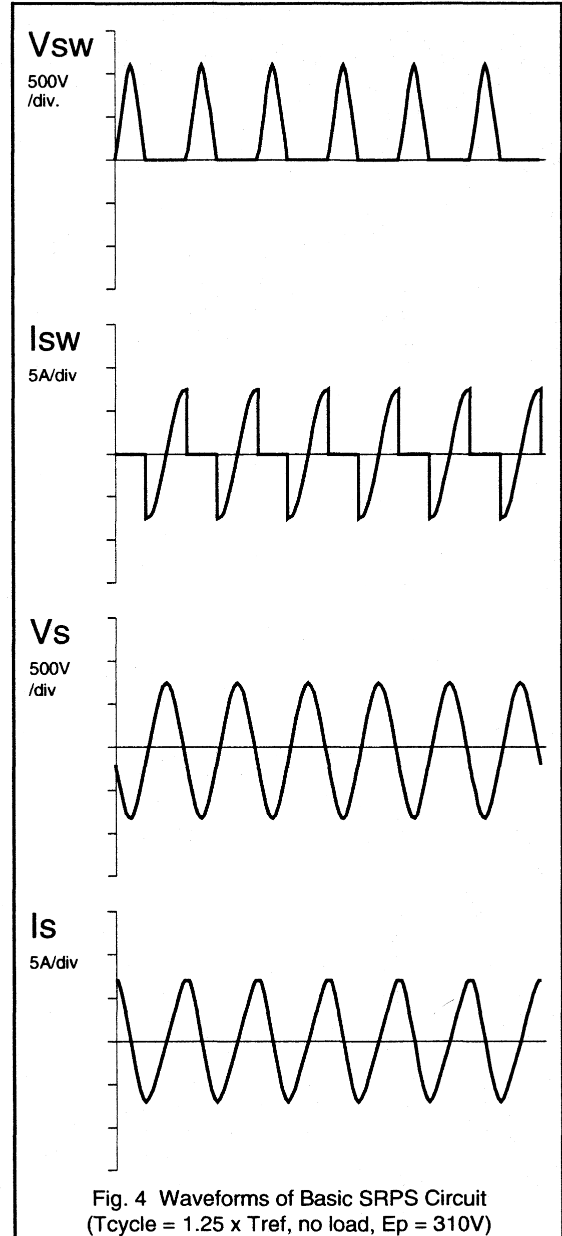


Fig. 4 Waveforms of Basic SRPS Circuit
(Tcycle = 1.25 x Tref, no load, Ep = 310V)

To realise the situation shown in Fig. 4, the output voltage Eo has to be increased considerably for no load operation for the same Ep or Ep can be decreased considerably for the same Eo. In fact, the relation between Eo and Ep in this figure is found to be:

$$Eo > 2.7 \times Ep$$

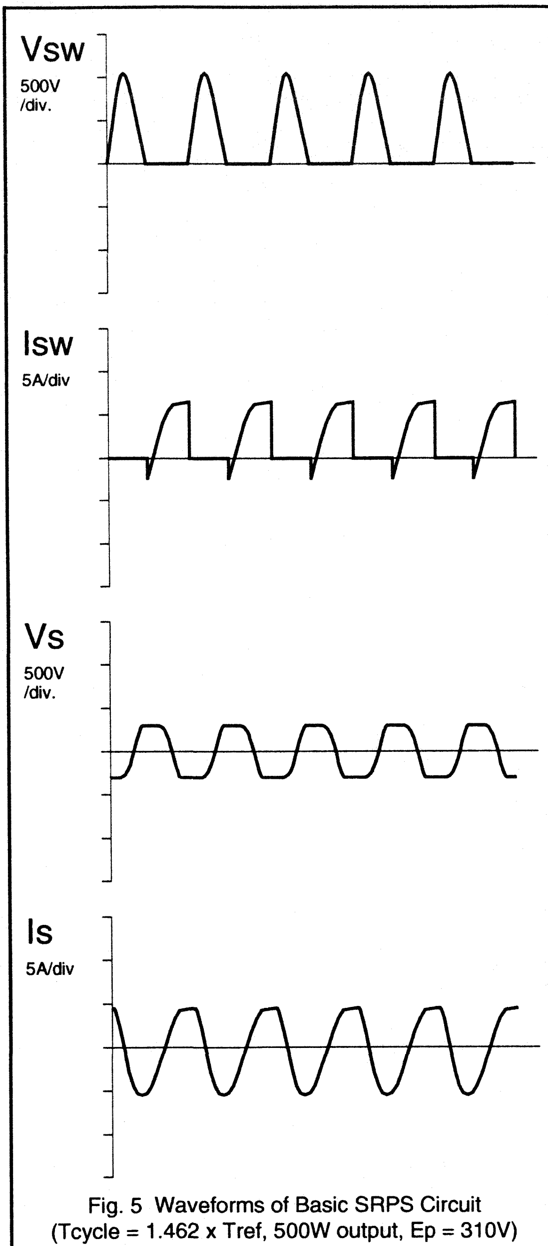


Fig. 5 Waveforms of Basic SRPS Circuit (Tcycle = 1.462 x Tref, 500W output, Ep = 310V)

Finally, Fig. 5 shows the voltages and currents for full load (Pout = 500W) at Ep = 310V and Eo = 300V. The input current Io is not shown but is a DC current of 1.6A with a small ripple current. The cycle time has been increased to 1.45 x Tref to get the 500W output power, giving an operating frequency of about 50 kHz.

It should be noted that S1 has to switch 'OFF' a high current at a relatively high dV/dt, resulting in significant turn-off losses. These losses are the main reason to prefer PRPS over SRPS for pre-converter applications.

The basic PRPS converter circuit

A basic PRPS converter topology is shown in Fig. 6. Just as for the basic SRPS pre-converter, we will assume a DC supply voltage Ep of 310 Vdc and a peak output power of 500W, i.e. a nett output power of 250W average.

The topology of Fig. 6 (PRPS) is almost identical to the topology of Fig. 2 (SRPS), except for the following points:

- Diode D1 is now in series with the switch S1 instead of in anti-parallel.
- Capacitor Cp has been omitted.

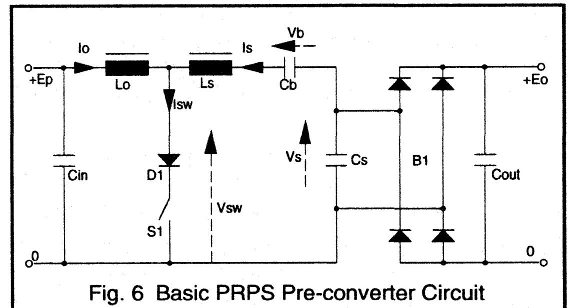


Fig. 6 Basic PRPS Pre-converter Circuit

The value of the two inductors Lo and Ls remain the same as they were in the SRPS, but the values of Cb and Cs are changed to obtain proper PRPS circuit operation. Having D1 in series with S1 does not lead to 'no-load' stability problems because, in the PRPS circuit, both the amplitude and the duration of the S1 current pulse are reduced as the output power decreases.

The input inductance Lo again forms the connection between the input voltage Ep and the switch voltage Vsw (across D1 and S1 in series). A 'PARALLEL' resonant L-C circuit, consisting of the series connection of Lo and Ls, the DC voltage blocking capacitor Cb and the capacitor Cs (both the switch S1 and the diode bridge B1 OFF) now determines the no load operation frequency. The value of the input capacitor Cin is chosen to be sufficiently large with respect to Cs to be neglected with respect to the no load operation frequency.

A practical PRPS pre-converter for 250W nett output power (500W peak power) can have component values as shown in Table 2.

Lo	4 mH	8 x Ls
Ls	500 µH	
Cs	24 nF	
Cb	48 nF	2 x Cs

Table 2 Component Values for PRPS circuit

To be able to put a full wave rectifier across capacitor Cs, the DC voltage blocking capacitor Cb cannot have a value of several times Cs. Therefore, a value of only twice Cs has been chosen for Cb. This ratio gives good practical results in combination with an output voltage, Eo, of 450V.

The parallel L-C circuit consists of series combinations of Lo and Ls and Cb and Cs. The output rectifier bridge now modulates the value of the capacitor between 2/3 Cs and 2 Cs (Cb and Cs in series and Cb only). It should be noted that the resonant frequencies of the two states differ by a factor of $\sqrt{3}$.

The switch S1 modulates the inductance value of the parallel L-C circuit between Lo + Ls and Ls. This is combined with a change in input voltage from zero (S1 ON) and Ep (S1 OFF). Again, the PRPS can be seen as a parametric amplifier, but now with both inductance and capacitance modulation.

In contrast with the SRPS circuit, the output power of a PRPS converter will increase with increasing operation frequency, thus with decreasing operation cycle time.

Under no load conditions and maximum operation cycle time, the output voltage and current will be near sinusoidal and wiil have their minimum no load values. This minimum output voltage can be calculated from

$$Vs > Ep.\frac{(Lo+Lp)}{Lo}.\frac{Cb}{(Cb+Cs)}$$

Substituting the values for Lo, Ls, Cb and Cs in the formula gives

$$Vs > 0.75 \times Ep$$

An output voltage choice of Eo = 450 V for Ep = 375 V will, therefore, be amply sufficient.

The voltage Vsw, the current Isw, the output voltage Vs and the current Is for the maximum operation cycle time, i.e. about equal to Tref, are shown in Fig. 7.

To get an impression of the boosting properties of the PRPS circuit, the no load voltages and currents are shown, for an operation cycle time Tcycle = 0.975 x Tref, in Fig. 8. It can be seen that the output voltage has been increased by a factor 2.5 with only a very small decrease of operation cycle time.

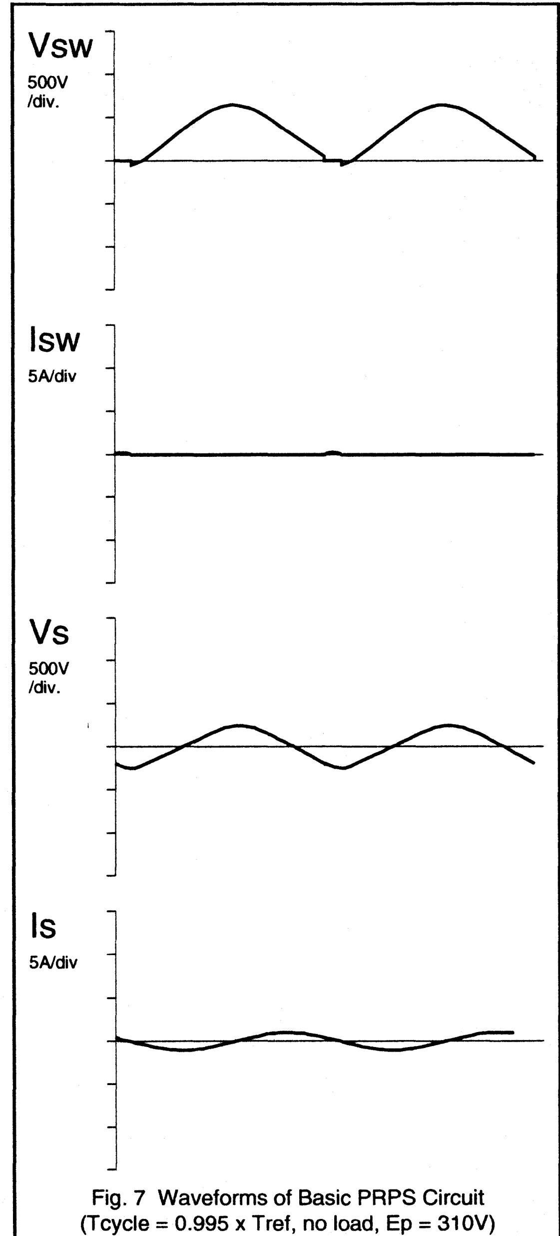


Fig. 7 Waveforms of Basic PRPS Circuit (Tcycle = 0.995 x Tref, no load, Ep = 310V)

Finally, the full load voltages and currents are shown in Fig. 9 (output power 500W at Eo = 450V and Ep = 310V). It should be noted that the operation cycle time has been decreased to .5694 x Tref.

The significant feature of the PRPS circuit is that the current in the main switching device S1 is brought down to zero by the circuit and not by the device itself. Device S1 can now be turned off without loss. The negative voltage which causes the current to fall, is supported by diode D1, which needs to be a fast recovery type like the BYR79. The reverse recovery loss in D1 is small because the resonant action of the circuit make the rate of fall of current relatively slow - up to two orders of magnitude slower than in a standard SMPS.

SRPS and PRPS compared

A pre-conditioner can be implemented using either an SRPS or PRPS topology. The capacitor and inductor values are roughly the same, as are the peak values of voltage and current. The main difference between the circuits is in the switching requirements of S1 and D1.

In the SRPS, the turn on loss of S1 is very low - the voltage across S1 is zero and the current rises relatively slowly. However the turn off loss is large - S1 has to turn off a large current and, although the dVsw/dt is moderated by Cp it is still relatively fast. On the other hand, the turn off loss in D1 is negligible - no voltage is applied to the diode until S1 is turned off giving plenty of time for reverse recovery - but the turn on loss may be significant because the dIsw/dt is un-restrained.

In the PRPS circuit, however, the turn off loss in S1 is close to zero but the recovery loss in D1 is not negligible - Isw falls through zero and the negative voltage appears across the diode. S1 is turned on from a high voltage so there will be some loss in both S1 and D1 even though the rate of rise of current is moderated by Ls.

It is generally true that reducing turn off loss produces a bigger cost/performance benefit than reducing turn on loss. It is also true that losses in diodes are usually much lower than in their associated switching device. Since the PRPS configuration reduces turn off loss in S1 to zero it appears that PRPS is a better choice than SRPS as a resonant pre-converter.

Therefore, the remainder of this paper will concentrate on PRPS circuits.

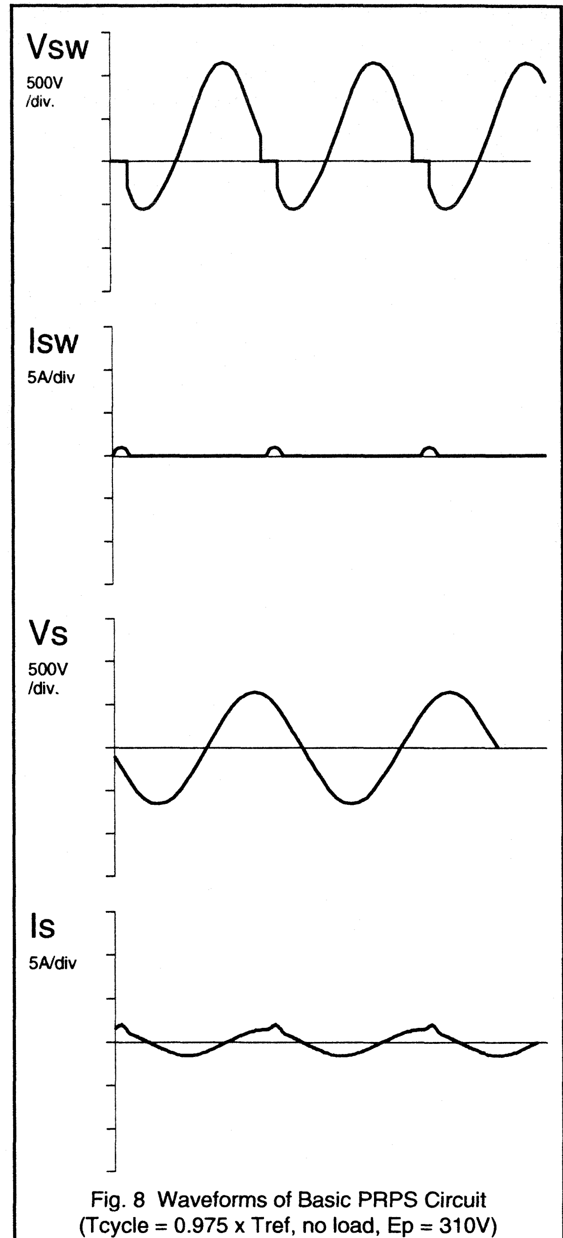


Fig. 8 Waveforms of Basic PRPS Circuit
(Tcycle = 0.975 x Tref, no load, Ep = 310V)

PRPS transformer for >1kW

The practical PRPS circuits in this paper all use a transformer with a built-in leakage inductance to give mains isolation and inductance Ls. The inexpensive U-64 core, used in large quantities in the line deflection and EHT circuits in colour TV sets, can be used successfully as the transformer core in PRPS converters with a nett output power in excess of 1000W.

Fig. 10 illustrates a PRPS transformer constructed with a pair of U-64 cores. Both the primary and secondary windings are split into two halves. Each leg of the U-core is fitted with a two-chamber coil former with a primary and a secondary winding. To achieve a reasonable 'leakage

inductance' Ls, the primary and secondary coils are crossed. Thus each U-core has one primary and one secondary coil.

A pre-converter transformer with this arrangement offers several advantages over the 'standard' SMPS transformer using E-cores.

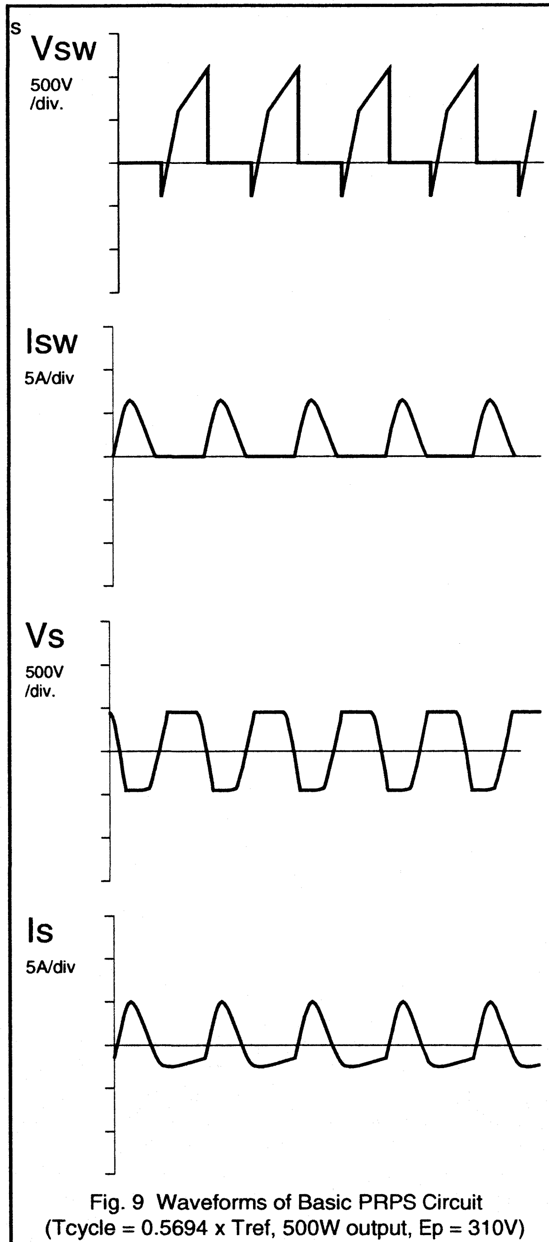


Fig. 9 Waveforms of Basic PRPS Circuit
(Tcycle = 0.5694 x Tref, 500W output, Ep = 310V)

- It will be easier to meet the mains isolation requirements, particularly with respect to creepage distances.

- The thermal properties will be much better because the winding is distributed over both core legs.

- The mean length of a turn is less than with a single core leg, reducing copper loss.

- The two leg arrangement will need only 70% of the turns of the one leg design. This is because of the active (magnetic) fluxing of both legs.

- It is a simpler and hence less expensive transformer to wind.

One disadvantage of this arrangement is that the windings are not layered. This means that 'skin effect' will have to be overcome by using Litz wire for both the primary and secondary windings.

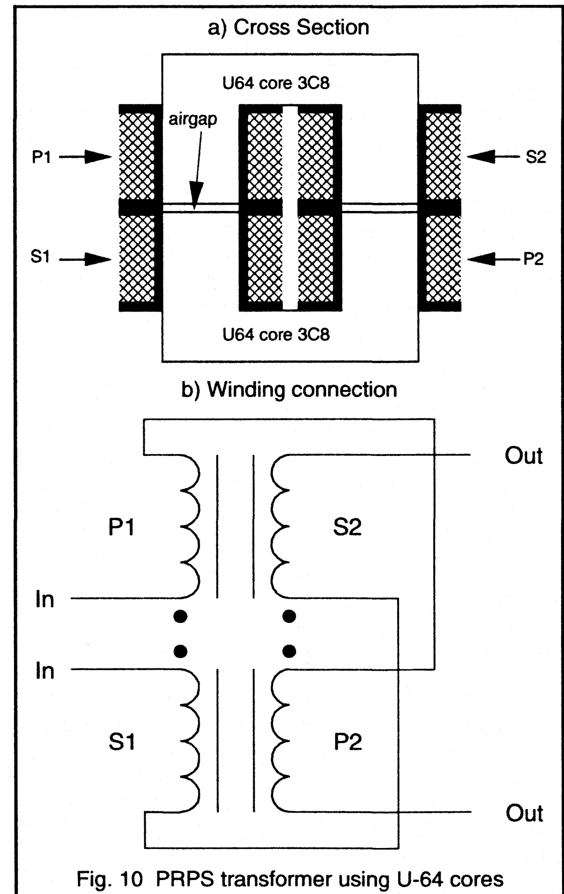


Fig. 10 PRPS transformer using U-64 cores

The equivalent electrical circuit diagram of the PRPS transformer is given in Fig. 11. It is the well known 'Tee' circuit with primary winding(s) leakage inductance Llp, a magnetisation inductance Lm and secondary winding(s) leakage inductance Lls, followed by an 'ideal' transformer for the output voltage transformation.

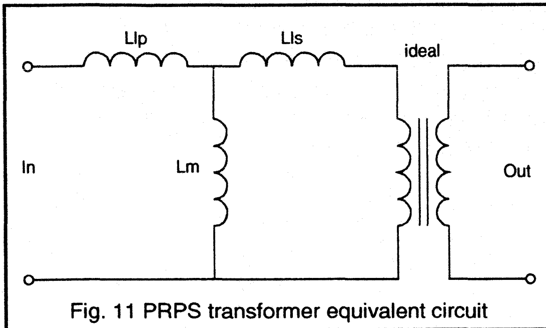


Fig. 11 PRPS transformer equivalent circuit

The primary and secondary leakage inductance is determined by the transformer construction and, in particular, by the positioning of the windings. In the symmetrical arrangement of Fig. 10, the values of Llp and Lls will be equal. Llp and Lls are also proportional to the square of the number of primary turns as is Lm. However, Lm is also strongly dependent on the width of the 'airgap' between the two U-cores. The airgap can be adjusted to give a value of Lm between 2 and 100 times Llp+Lls.

The transformer can be characterised by two inductance measurements:

- Lx, the measured primary inductance with the secondary winding(s) shorted.

- Ly, the measured primary inductance with the secondary winding(s) open circuit

It can be seen from the equivalent circuit diagram that,

$$Lx = Llp + \frac{Lm.Lls}{Lm + Lls}$$

$$Ly = Llp + Lm$$

If the transformer is assumed to be symmetrical then,

$$Llp = Lls$$

rearranging gives,

$$Llp = Ly - \sqrt{Ly^2 - Lx.Ly}$$

$$Lm = \sqrt{Ly^2 - Lx.Ly}$$

If the airgap is <50μm then Lm will be at least 100 times the value of Llp or Lls. In this case,

$$Lx \approx Llp + Lls$$

and

$$Ly \approx Lm$$

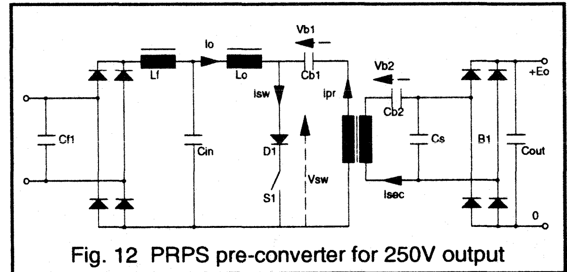


Fig. 12 PRPS pre-converter for 250V output

A PRPS pre-converter transformer for 1250W nett output has been constructed to the arrangement shown in Fig. 10. It had a primary consisting of two 36 turn windings connected in series, wound using 600 x 0.07mm Litz wire. The number of turns on the secondary varied depending on the required output voltage. Measurements of this transformer gave the following values for Lx and Ly.

Lx = 200 μH

Ly = 1600 μH (Note that this value is strongly influenced by the size of the airgap)

PRPS pre-converter for high output voltages

The circuit shown in Fig. 12 is a PRPS pre-converter using the type of transformer mentioned earlier. This circuit is intended to deliver 1250W at a relatively high voltage - in this case 250V. To achieve an final output voltage of 250V with an effective output voltage, Eo, of 450V means having a transformer with a turns ratio of 8:5.

Cf1	2μF	2 x 1μF
Cin	2μF	2 x 1μF
Cb1	0.2μF	2 x 0.1μF
Cb2	1.36μF	2 x 0.68μF
Cs	0.3μF	2 x 0.15μF
Lf	1600μH	
Lo	1600μH	
Lx	200μH	
Ly	1600μH	

Table 3 Component Values for High Output Voltage PRPS circuit

The transformer has replaced the inductance Ls in the basic circuit diagram of Fig. 6. The DC voltage blocking capacitor Cb has been split up into a primary blocking capacitor Cb1 and a secondary blocking capacitor Cb2. There will, therefore, be no DC current in Tr1 so in principle the transformer does not need an air gap. However, experience

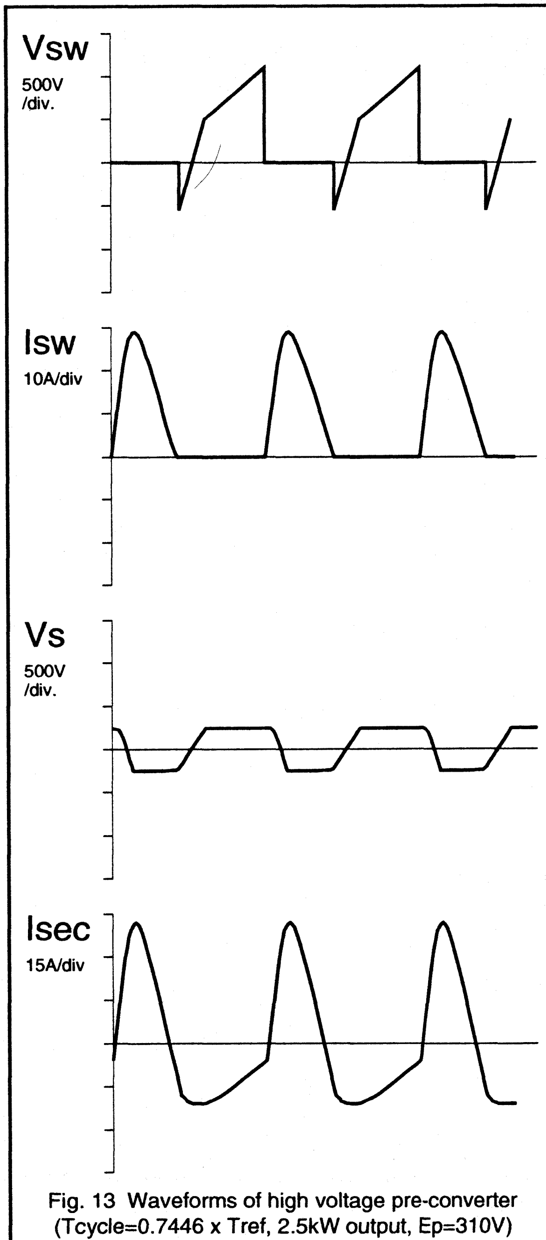


Fig. 13 Waveforms of high voltage pre-converter (Tcycle=0.7446 x Tref, 2.5kW output, Ep=310V)

has shown that a limited value of magnetisation inductance improves the operation of the circuit, so an airgap has been included which keeps the Ly value, of Tr1, equal to Lo.

The pre-converter circuit has been com~leted by the addition of capacitor Cf1, rectifier bridge an~ ~er inductor Lf (an iron cored choke). The combination of Cf1, Lf, Cin and Lo prevents a significant switching frequency signal appearing at the mains terminals.

The component values shown in table 3 are used in the circuit of Fig. 12. With these values the no load reference cycle time will be 49.7 µs. Therefore, the no load operating frequency is just over 20 kHz.

Figs. 13 and 14 show the waveforms associated with the circuit when the input voltage is 310 V and the circuit is delivering 2.5 kW

Ep	Pout (PRPS)	Pout (R load)	% Deviation
310.0	2501	2501	0.0%
308.3	2476	2474	0.1%
303.2	2389	2392	-0.1%
294.8	2249	2262	-0.6%
283.2	2068	2087	-0.9%
268.5	1857	1876	-1.0%
250.8	1621	1637	-1.0%
230.4	1375	1382	-0.5%
207.4	1128	1119	0.8%
182.2	890	864	3.0%
155.0	668	625	6.8%
126.1	472	414	14.1%
95.8	305	239	27.7%
64.5	171	108	57.9%
32.4	70	27	156.2%

Table 4 Output power of PRPS pre-converter.

Of particular interest is Io because it can be easily measured with a low value resistor. This current will be used to control power output of the PRPS pre-converter. Io will be compared with a reference, Ioref, which will be proportional to input voltage Ep. The comparison of Io and Ioref should be done at the right time, namely during the period when Io has a negative slope. The switch S1 is turned ON as soon as the value of Io drops below Ioref.

The computed values of Pout for 15 values of Ep which would be achieved using this control strategy are given in Table 4. As a comparison the output power for a resistive load is also shown in Table 4.

It can be seen from Table 4, that the PRPS output power closely matches the power of a purely resistive load except for Ep values near the zero crossings of the mains/line voltage.

Of course, an average output power control loop (with a time constant far in excess of the 10 (8.3) ms cycle time of a half mains/line period) is required to determine the

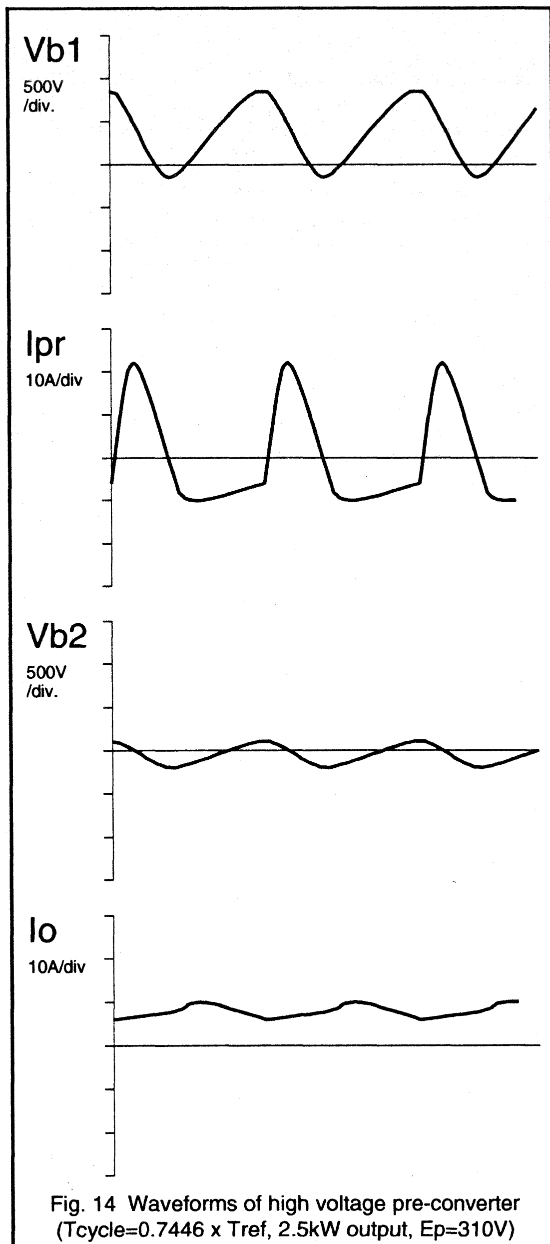


Fig. 14 Waveforms of high voltage pre-converter (Tcycle=0.7446 x Tref, 2.5kW output, Ep=310V)

proportionality constant between the mains/line voltage and Ioref for the mains/line voltage variations and for the output power control.

It can also be concluded, from table 4, that the PRPS circuit can indeed fulfil the pre-converter action successfully, i.e. a resistive load for the mains voltage can be easily achieved, thus no mains distortion and a power factor >0.99 is possible.

The circuit shown in Fig. 12 is only suitable for high output voltages. At low output voltages (below 100V for output powers in excess of 1000W), the secondary blocking capacitor Cb2 has to have a high value and pass a large current and is, therefore, an expensive component. If a low output voltage pre-converter is required, then an alternative arrangement is needed.

PRPS pre-converter for low output voltages

The high cost of Cb2, in a low output voltage PRPS pre-converter, could be avoided if it could be eliminated from the circuit. The problem is that removing Cb2 allows a DC current to flow in the transformer. The resulting flux can be handled by increasing the airgap between the cores of the transformer. This will have the additional effect of reducing Ly from 1600 µH to 800 µH. This change has been incorporated in the circuit shown in Fig. 15, which is intended to deliver 1200W at 60V.

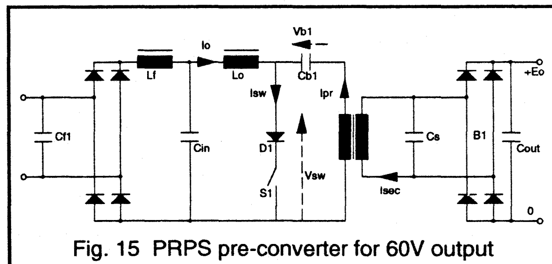


Fig. 15 PRPS pre-converter for 60V output

To get 1200W nett from a transformer of the type shown in Fig. 10 it is necessary to change the number of primary turns Np and thus decrease the value of Lx. Suitable values would be:

Np (primary turns)	2 x 28	(600 x .07 mm Litz wire)
Ns (secondary turns)	2 x 4	(flat Litz wire 7 mm2)

The air gap in the transformer should be adjusted to give an Lx of 125 µH.

Suitable values for the other components are given in table 5. The reference cycle time, Tref, with these values will be 39 µs.

The inductance Lo can be made with either a pair of U-64 cores - with the winding distributed over both legs- or with a pair of E-cores.

Cf1	2μF	2 x 1μF
Cin	2μF	2 x 1μF
Cb1	0.15μF	
Cs	3.75μF	5 x 0.75μF
Lf	1600μH	
Lo	1600μH	

Table 5 Component Values for Low Output Voltage PRPS circuit

In practice, PRPS pre-converters produce about 150W for each Amp(rms) flowing in the primary winding. So for a 1200W converter:

Ipr = 8A
Isec = 56A (at 60V and 20A)

The voltage and current wave forms for the circuit of Fig. 15 are similar to those shown in Figs. 13 and 14, except for the amplitudes in the secondary side.

This configuration of PRPS pre-converter is viable for output voltages as low as 40 V. Below this, however, the value and current rating of Cs becomes excessive and it is likely that alternative configurations would be more cost effective.

Control circuit for PRPS converters

Figure 16 shows a simple control circuit for PRPS converters. In is constructed from MOS ICs and standard comparators. The analogue control section for the output power stabilisation is not shown because it will, in principle, be no different than for an SMPS converter.

The PRPS control circuit comprises of a dual sawtooth oscillator whose frequency can be adjusted by applying a voltage to X1. The output of this oscillator is fed to the clock pulse input of a divide-by-8 counter. The highest oscillator frequency needs to be just over 8x the highest expected operating frequency of the PRPS power section.

The oscillator can be stopped by applying a hold up signal (low) to G1. This hold-up input is used to modulate the cycle time of the control circuit. As soon as this 'hold up' signal is removed (high), a pulse will sent to the divide-by-8 circuit which then advances one position.

The counter has 8 outputs, Q0-Q7. Output Q0 will go high either synchronously following Q7 or asynchronously with a high on pin15. Output Q0 sets a flip-flop consisting of a 2 and a 3 input NOR-gate. The output terminal X8 then goes high to indicate that the main switching device S1 should turn on.

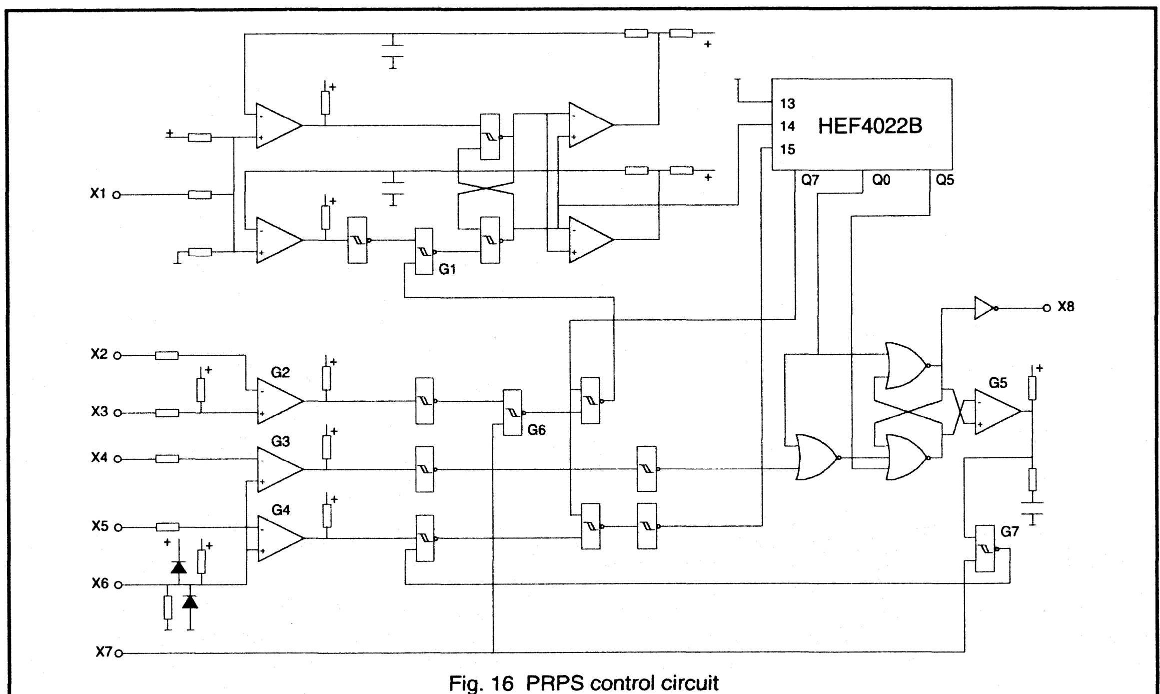


Fig. 16 PRPS control circuit

The Q7 output is used to enable both the 'hold-up' signal for the oscillator and the reset input for the divide-by-8, i.e. both the 'hold-up' and the reset only can be active if there is a '1' at Q7. The output flip-flop is reset either by the negative voltage across S1-D1 - via comparator G3 - or by the sixth position, Q5, of the counter. To prevent the possibility of immediate reset of the flip-flop, the indication of negative voltage across S1-D1 is blanked out while Q0 is high.

The voltage across S1-D1 is connected to terminal X6 via a high value resistor (220 kΩ). X4 is connected to the negative supply line of the power circuit. Comparator G3 then gives logical information about the polarity of the voltage across S1-D1.

Information about the amplitude of this voltage is obtained via comparator G4. A reference voltage, proportional to the mains voltage, is connected to X5. If the attenuated S1-D1 voltage falls below this reference, and Q7 is high, the counter will be reset and S1 will be turned ON. This is an emergency measure in case the normal current control loop via the comparator G2 fails to disable the 'hold up' signal. This could occur if there were a false current reference signal at X2.

The best strategy for the control of a PRPS pre-converter is by comparing the current, Io, in the input inductor, Lo, with a mains proportional reference current. In Fig. 16 a signal, proportional to Io, is connected to X3 and the reference signal to X2. As soon as Io falls below the reference value the 'hold-up' signal is removed, the counter is advanced from Q7 to Q0 and S1 is turned ON.

A '1' at input X7 allows the control circuit to run, whereas a '0' will cause the PRPS to switch OFF in a controlled manner. When X7 goes high, the output of NAND gate G7 goes low. This signal is used to reset the counter which takes Q0 high, turns on S1 and starts the operating cycle. The output of G5, which was pulled high while the circuit was stopped, is now driven low and is kept low by the RC network as long as S1 continues to be switched. This 'low' keeps the output of G7 high and allows the correct signal to be fed from G4 to the counter reset. The high on X7 also enables G6 and lets the information from G2 - the 'current' comparator - through to the 'hold up' circuit.

If X7 is taken low then G6 is disabled and the signal which would start the next switching cycle is not allowed to get through. The counter will continue to run until Q7 goes high at which time the circuit will be 'held up' and the operating cycle will be halted.

The cycle time will be adjusted by changing the reference value at X2. This signal will be a series of half sinewaves whose peak value is proportional to the power that the pre-converter needs to deliver to the keep the output voltage at the required level. This control strategy has been tested on various PRPS circuits and fulfils all the requirements properly.

Modelling PRPS pre-converters

There are no equations which summarise the overall behaviour of a PRPS pre-converter circuit. Determining factors like the throughput power of the circuit and the peak voltages and currents, means developing a computer model. In this model the operation of the circuit is broken down into its separate modes and the appropriate equations derived for each of them.

The circuit of Fig. 6 has, basically, two switches which determine its mode of operation. The first is the combination of S1 and D1 - this is the controllable switch - and the second is the bridge rectifier B1.

Therefore the circuit has four different modes of operation. For all these modes, the time functions for the currents and voltages can be derived by circuit analysis. The four modes are given below:

Mode	S1-D1	Bridge
I	ON	ON
II	ON	OFF
III	OFF	OFF
IV	OFF	ON

Table 6 PRPS Operating Modes

Using Laplace transformation it is possible to derive the time functions for currents Io and Is, for the circuit in each of its 4 modes. This method allows the initial values of the currents and voltages to be easily introduced into the equations. The initial conditions of Io, Is, Vb1 and Vs will be indicated by Jo, Js, Ub1 and Us respectively.

Mode I

We will start with the derivation of the time functions for the operation of the PRPS circuit in mode I (S1-D1 ON and B1 ON). The initial conditions are:

$$Io = Jo$$

$$Is = Js = -Jo$$

$$Vb1 = Ub1$$

$$Vs = Us = Eo$$

Calculation starts at t = 0 with the switching ON of S1-D1, while B1 is already conducting, i.e. $Jo > 0$. The following Laplace equations are then valid:

$$\frac{Ep}{s} + Lo.Jo = Io.s.Lo$$

$$\frac{Ub1+Us}{s}+Ls.Js=Is.\left(s.Ls+\frac{1}{s.Cb1}\right)$$

Note: B1 is conducting, so $Vs = Us = Eo$, i.e. Cs is infinitely large and has no influence on Is.

If we define the following:

$$\omega=\sqrt{\frac{1}{Ls.Cb1}}$$

$$F1=Jo$$

$$F2=\frac{Ep}{Lo}$$

$$G1=Js$$

$$G2=\frac{Ub1+Us}{Ls}$$

The Laplace equations for Io and Is can then be written as:

$$Io=\frac{F1}{s}+\frac{F2}{s^2}$$

$$Is=\frac{G1.s}{s^2+\omega^2}+\frac{G2}{s^2+\omega^2}$$

The inverse Laplace transformation of these two equations gives the following time functions:

$$Io=F1+F2.t$$

$$Is=G1.\cos(\omega.t)+\frac{G2}{\omega}.\sin(\omega.t)$$

To calculate the input power and the voltage Vb1 and Vs, these time functions can be integrated to give Ioint and Isint, thus:

$$Ioint=F1.t+\frac{F2}{2}.t^2$$

$$Isint=\frac{G1}{\omega}.\sin(\omega.t)+\frac{G2}{\omega^2}.(1-\cos(\omega.t))$$

The input power during the validity of mode I (i.e. during a time interval of length T1) is equal to:

$$Pin(T1)=\frac{Ep.Ioint}{T1}$$

The voltages Vb1 and Vs are equal to:

$$Vb1=Ub1-\frac{Isint}{Cb1}$$

$$Vs=Us=Eo$$

In the computer program, these formulae will be stored in a subroutine called sub1.

Mode II

The initial conditions for mode II operation (S1-D1 ON and B1 OFF) are:

$$Io=Jo$$

$$Is=Js$$

$$Vb1=Ub1$$

$Vs=Us$ (either +Eo or -Eo)

The Laplace equations for Io and Is are now:

$$\frac{Ep}{s}+Lo.Jo=Io.s.Lo$$

$$(Ub1+Us).s+Ls.Js=Is.\left(s.Ls+\frac{Cb1+Cs}{s.Cb1.Cs}\right)$$

Define:

$$\omega=\sqrt{\frac{Cb1+Cs}{Ls.Cb1.Cs}}$$

$$F1=Jo$$

$$F2=\frac{Ep}{Lo}$$

$$G1=Js$$

$$G2=\frac{Ub1+Us}{Ls}$$

The Laplace functions for Io and Is are now identical to those for mode I, so the time functions are:.

$$Io=F1+F2.t$$

$$Is=G1.\cos(\omega.t)+\frac{G2}{\omega}.\sin(\omega.t)$$

$$Ioint=F1.t+\frac{F2}{2}.t^2$$

$$Isint=\frac{G1}{\omega}.\sin(\omega.t)+\frac{G2}{\omega^2}.(1-\cos(\omega.t))$$

$$Pin(T2)=\frac{Ep.Ioint}{T2}$$

$$Vb1=Ub1-\frac{Isint}{Cb1}$$

$$Vs=Us-\frac{Isint}{Cs}$$

In the computer program, these formulae will be stored in a subroutine called sub2.

Mode III

The initial conditions for mode III operation (S1-D1 OFF and B1 OFF) are:

$Io = Jo$

$Is = Js = -Jo$

$Vb1 = Ub1$

$Vs = Us$

The correct Laplace equation for Is ($Io = -Is$) can be expressed by the relationship:

$$\frac{Ub1 + Us - Ep}{s} + (Lo + Ls).Js = Is.\left(s.(Lo + Ls) + \frac{Cb1 + Cs}{s.Cb1.Cs}\right)$$

Define:

$$\omega = \sqrt{\frac{Cb1 + Cs}{(Lo + Ls).Cb1.Cs}}$$

$G1 = Js$

$$G2 = \frac{Ub1 + Us - Ep}{Lo + Ls}$$

The time functions can then be expressed by:

$$Is = G1.\cos(\omega.t) + \frac{G2}{\omega}.\sin(\omega.t)$$

$Io = -Is$

$$Isint = \frac{G1}{\omega}.\sin(\omega.t) + \frac{G2}{\omega^2}(1 - \cos(\omega.t))$$

$Ioint = Isint$

$$Pin(T3) = \frac{Ep.Ioint}{T3}$$

$$Vb1 = Ub1 - \frac{Isint}{Cb1}$$

$$Vs = Us - \frac{Isint}{Cs}$$

In the computer program, these formulae will be stored in a subroutine called sub3.

Mode IV

The initial conditions for the mode IV operation (S1-D1 OFF and B1 ON) are given below:

$Io = Jo$

$Is = Js = -Jo$

$Vb1 = Ub1$

$Vs = Us = Eo$

The Laplace equation for current Is is now:

$$\frac{Ub1 + Us - Ep}{s} + (Lo + Ls).Js = Is.\left(s.(Lo + Ls) + \frac{1}{(s.Cb1)}\right)$$

Define:

$$\omega = \sqrt{\frac{1}{(Lo + Ls).Cb1}}$$

$G1 = Js$

$$G2 = \frac{Ub1 + Us - Ep}{Lo + Ls}$$

The time functions are given by,

$$Is = G1.\cos(\omega.t) + \frac{G2}{\omega}.\sin(\omega.t)$$

$Io = -Is$

$$Isint = \frac{G1}{\omega}.\sin(\omega.t) + \frac{G2}{\omega^2}(1 - \cos(\omega.t))$$

$Ioint = Isint$

$$Pin(T4) = \frac{Ep.Ioint}{T4}$$

$$Vb1 = Ub1 - \frac{Isint}{Cb1}$$

$Vs = Us$

In the computer program, these formulae will be stored in a subroutine called sub4.

Program structure

The modelling program can be written around the four subroutines. The central part of the program will make successive calls to the appropriate subroutine. The calculated values of current and voltage will be used to determine when the circuit moves form one mode to the next. The final values of Io, Is, Vb1 and Vs will be used as the initial values, Jo, Js, Ub1 and Us, for the next mode. The actual sequence of the modes depends upon the operating frequency and load condition. Under full load condition when Ep is not close to zero, the sequence of modes will be as shown in Table 7.

One cycle of operation ends when Io falls below Ioref. This would result in S1 being turned ON, putting the circuit in to mode I and starting the cycle once more. At the end of each cycle, the input power can be compared with a reference value (Pref) and Ioref can be adjusted until the powers are equal. It is then possible to read various important values

S1-D1	B1	Mode	End Condition
ON	ON	I	Is>0
ON	OFF	II	Vs<-Eo
ON	ON	I	Is<0
ON	OFF	II	Isw=Io+Is<0
OFF	OFF	III	Vs>Eo
OFF	ON	IV	Io<Ioref

Table 7 PRPS Operating Sequence

such as the initial conditions for Io, Is, Vb1, Vs, the cycle time, output power, RMS values of Io and Is, DC and AC fluxes in the ferrite cores, etc.

Writing a program like this is well within the capabilities of anyone with some experience of programming. The calculations involved are so simple that there will be little difficulty in using almost any programming language. A model produced in this way will be faster and more accurate than could be produced with any of the standard modelling programs.

Conclusions

The PRPS configuration is well suited to the needs of the pre-converter application. It can boost the low mains voltages, near zero crossing, to high levels so that some power is delivered to the load throughout all of the mains cycle. This helps the PRPS appear as a resistive load to the mains.

A PRPS pre-converter can deliver a DC output voltage with low levels of mains ripple using only moderately sized output smoothing capacitors. The addition of a high frequency transformer gives mains isolation and the ability to have a wide range of output voltages.

The transformer need not be a major additional cost. The high operating frequency means the transformer uses ferrite core and is relatively small (5% of the size of copper / iron transformer). A side by side arrangement of the windings means the transformer is easy to wind, easy to insulate and can have the right leakage inductance to replace the resonant network inductor.

The resonant action of the PRPS circuit allows the main semiconductor switching device to be turned off at zero current. This reduces, considerably, the switching loss of this device allowing a smaller device to be used in higher power / frequency circuits than it could normally resulting in a significant cost saving.

Unfortunately an overall analysis of the performance of a PRPS pre-converter is difficult. However, by breaking the cycle of operation into its logical modes, it becomes easy to generate the time functions for all the currents and voltages. It is simple to incorporate these equations into a computer program to produce an accurate, detailed and fast running model of the system.

The use of pre-converters is become increasingly necessary and the characteristics of PRPS circuits mean that there are well suited to this function. It is easy to overcome the apparent complexity of resonant systems to produce PRPS pre-converters which are elegant, efficient and cost effective.

CHAPTER 3

Motor Control

3.1 AC Motor Control
3.2 DC Motor Control
3.3 Stepper Motor Control

AC Motor Control

3.1.1 Noiseless a.c. motor control: introduction to a 20kHz system

Controlling an a.c. induction motor by the technique of sinewave-weighted pulse-width modulation (PWM) switching gives the benefits of smooth torque at low speeds, and also complete speed control from zero up to the nominal rated speed of the motor, with only small additional motor losses.

Traditional power switches such as thyristors need switching frequencies in the audible range, typically between 400 and 1500Hz. In industrial environments, the small amount of acoustic noise produced by the motor with this type of control can be regarded as insignificant. By contrast, however, the same amount of noise in a domestic or office application, such as speed control of a ventilation fan, might prove to be unacceptable.

Now, however, with the advent of power MOSFETs, three-phase PWM inverters operating at ultrasonic frequencies can be designed. A three-phase motor usually makes even less noise when being driven from such a system than when being run directly from the mains because the PWM synthesis generates a purer sinewave than is normally obtainable from the mains.

The carrier frequency is generally about 20kHz and so it is far removed from the modulation frequency, which is typically less than 50Hz, making it economic to use a low-pass filter between the inverter and the motor. By removing the carrier frequency and its sidebands and harmonics, the waveform delivered via the motor leads can be made almost perfectly sinusoidal. RFI radiated by the motor leads, or conducted by the winding-to-frame capacitance of the motor, is therefore almost entirely eliminated. Furthermore, because of the high carrier frequency, it is possible to drive motors which are designed for frequencies higher than the mains, such as 400Hz aircraft motors.

This section describes a three-phase a.c. motor control system which is powered from the single-phase a.c. mains. It is capable of controlling a motor with up to 1kW of shaft output power. Before details are given, the general principles of PWM motor control are outlined.

Principles of Pulse-Width Modulation

Pulse-width modulation (PWM) is the technique of using switching devices to produce the effect of a continuously varying analogue signal; this PWM conversion generally has very high electrical efficiency. In controlling either a three-phase synchronous motor or a three-phase induction motor it is desirable to create three perfectly sinusoidal current waveforms in the motor windings, with relative phase displacements of 120˚. The production of sinewave power via a linear amplifier system would have low efficiency, at best 64%. If instead of the linear circuitry, fast electronic switching devices are used, then the efficiency can be greater than 95%, depending on the characteristics of the semiconductor power switch.

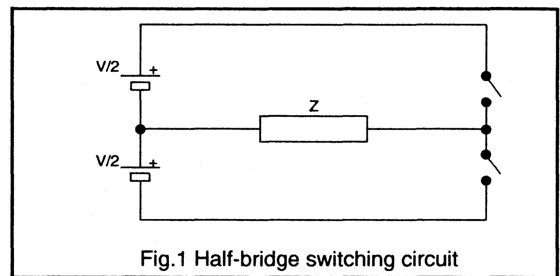


Fig.1 Half-bridge switching circuit

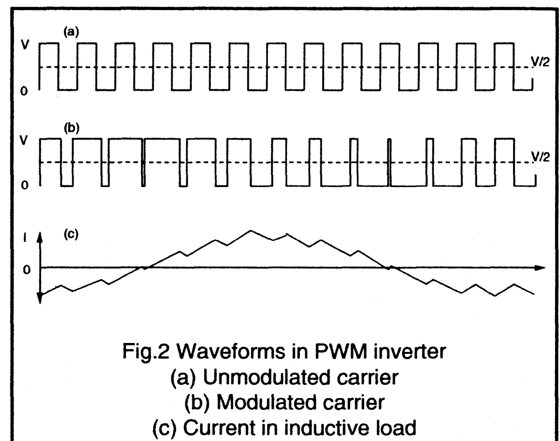


Fig.2 Waveforms in PWM inverter
(a) Unmodulated carrier
(b) Modulated carrier
(c) Current in inductive load

The half-bridge switching circuit in Fig.1 is given as an example: the switches can be any suitable switching semiconductors. If these two switches are turned on alternately for equal times, then the voltage waveform across the load is as shown in Fig.2a. The mean value of this waveform, averaged over one switching cycle is V/2. This square wave with a constant 50% duty ratio is known as the 'carrier' frequency. The waveform in Fig.2b shows

the effect of a slow variation or 'modulation' of the duty ratio; the mean voltage varies with the duty ratio. The waveform of the resultant load current depends on the impedance of the load Z. If Z is mainly resistive, then the waveform of the current will closely follow that of the modulated square wave. If, however, Z is largely inductive, as with a motor winding or a filter choke, then the switching square wave will be integrated by the inductor. The result is a load current waveform that depends mainly on the modulation of the duty ratio.

If the duty ratio is varied sinusoidally in time, then the current in an inductive load has the form of a sinewave at the modulation frequency, lagging in phase, and carrying ripple at the switching frequency as shown in Fig.2c. The amplitude of the current can be adjusted by controlling the depth of modulation, that is, the deviation of the duty ratio from 50%. For example, a sinewave PWM signal which varies from 5% to 95%, giving 90% modulation, will produce a current nine times greater than that produced by a signal which varies only from 45% to 55%, giving only 10% modulation.

For three-phase a.c. motor control, three such waveforms are required, necessitating three pairs of switches like those shown in Fig. 1, connected in a three-phase bridge. The inductance required to integrate the waveform can usually be provided by the inductance of the stator windings of the motor, although in some instances it might be provided by the inductance of a separate low-pass filter. The modulations in the three switching waveforms much be maintained at a constant relative phase difference of 120˚, so as to maintain motor current sinewaves which are themselves at a constant 120˚ phase difference. The modulation depth must be varied with the modulation frequency so as to keep the magnetic flux in the motor at approximately the design level.

In practice, the frequency of the modulation is usually between zero and 50Hz. The switching frequency depends on the type of power device that is to be used: until recently, the only devices available were power thyristors or the relatively slow bipolar transistors, and therefore the switching frequency was limited to a maximum of about 1 kHz. With thyristors, this frequency limit was set by the need to provide forced commutation of the thyristor by an external commutation circuit using an additional thyristor, a diode, a capacitor, and an inductor, in a process that takes at least 40µs. With transistors, the switching frequency was limited by their switching frequency and their long storage times.

In this earlier type of control circuit, therefore, the ratio of carrier frequency to modulation frequency was only about 20:1. Under these conditions the exact duty-ratios and carrier frequencies had to be selected so as to avoid all sub-harmonic torques, that is, torque components at frequencies lower than the modulation frequency. This was done by synchronising the carrier to a selected multiple of the fundamental frequency; the HEF4752V, an excellent IC purpose-designed for a.c. motor control, uses this particular approach. The 1kHz technique is still extremely useful for control of large motors because whenever shaft output powers of more than a few kW are required, three-phase mains input must be used, and there are, as yet, few available switching devices with combined high voltage rating, current rating, and switching speed.

However, using MOSFETs with switching times of much less than 1µs, the carrier frequency can be raised to the ultrasonic region, that is, to 20kHz or more. There are obvious system benefits with this higher frequency, but there are also several aspects of PWM waveform generation that become easier. It is possible to use a fixed carrier frequency because the sub-harmonics that are produced as a result of the non-synchronisation of the carrier frequency with a multiple of the fundamental are insignificant when the ratio of the carrier frequency to the fundamental frequency is typically about 400:1.

To maintain good waveform balance, and thus avoid any d.c. in the motor, and therefore also avoid parasitic torques, a digital waveform generation technique is appropriate. The waveform can be stored as a 'look-up' table of numbers representing the sinewave. To generate the three phases, this table can be read at three points that have the correct 120˚ phase relationship. The numbers taken from the table represent the duty ratios corresponding to 100% modulation: these numbers can then be scaled down by multiplication or some equivalent technique to give the correct duty-ratio numbers for the modulation depth required.

The speed of the motor is controlled by the rate at which the reading pointers scan the look-up table and this can be as slow as desired. If the pointers are stationary, then the system will be 'frozen' at a particular point on the three-phase sinewave waveform, giving the possibility of obtaining static torque from a synchronous motor at zero speed. The rate at which the numbers are produced by this read-out process from the look-up table is constant and determines the carrier frequency.

To convert these three simultaneous parallel digital numbers into time lengths for pulses, three digital counters are needed. The counters can be designed to give double-edged modulation, such that both the leading edge and the trailing edge of each pulse move with respect to the unmodulated carrier. The line-to-line voltage across the load will have most of its ripple at a frequency of twice the switching frequency, and will have a spectrum with minimum even harmonics and no significant component below twice the switching frequency. Motor ripple current is therefore low and motor losses are reduced.

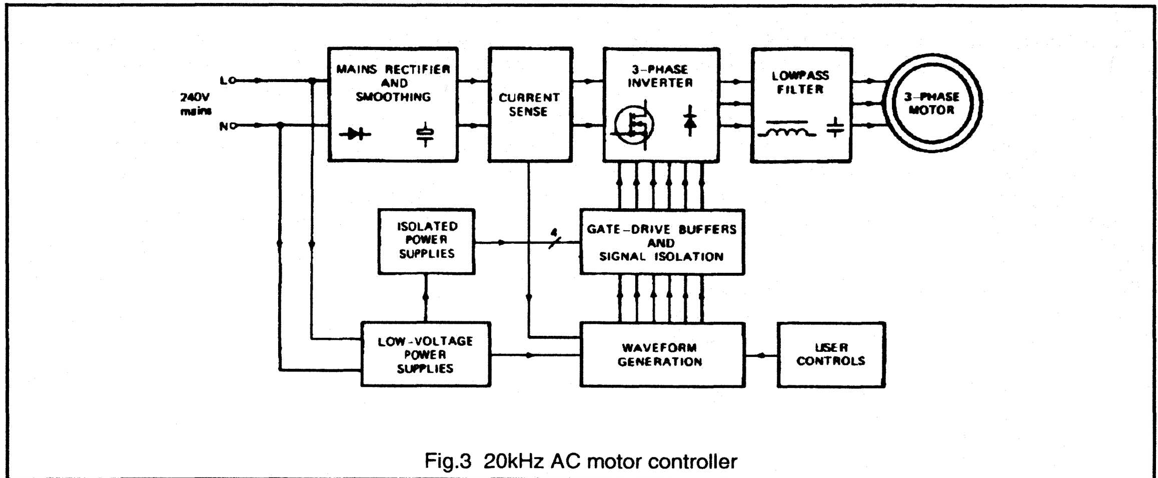


Fig.3 20kHz AC motor controller

There is a further advantage to be obtained from the high ratio of carrier to modulation frequency: by adding a small amount of modulation at the third harmonic frequency of the basic fundamental modulation frequency, the maximum line-to-line output voltage obtainable from the inverter can be increased, for the following reason. The effect of the third harmonic on the output voltage of each phase is to flatten the top of the waveform, thus allowing a higher amplitude of fundamental while still reaching a peak modulation of 100%. When the difference voltage between any two phases is measured, the third harmonic terms cancel, leaving a pure sinewave at the fundamental frequency. This allows the inverter output to deliver the same voltage as the mains input without any significant distortion, and thus to reduce insertion losses to virtually zero.

Overview of a practical system

The principles outlined above are applied to a typical system shown in Fig.3. The incoming a.c. mains is rectified and smoothed to produce about 300V and this is fed to the three-phase inverter via a current-sensing circuit. The inverter chops the d.c. to give 300V peak-to-peak PWM waves at 20kHz, each having low-frequency modulation of its mark-space ratio. The output of the inverter is filtered to remove the 20kHz carrier frequency, and the resultant sinewaves are fed to the a.c. motor.

The six switches in the inverter are under the command of a waveform-generation circuit which determines the conduction time of each switch. Because the control terminals of the six switches are not at the same potential, the outputs of the waveform-generation circuits must be isolated and buffered. A low-voltage power supply feeds the signal processing circuit, and a further low-voltage power supply drives a switch-mode isolating stage to provide floating power supplies to the gate drive circuits.

Signal processing

Fig.4 shows a block diagram of the circuit which generates the PWM control signals for the inverter. The input to the system is a speed-demand voltage and this is also used for setting the required direction of rotation: the analogue speed signal is then separated from the digital direction signal. The speed-demand voltage sets the frequency of the voltage-controlled oscillator (VCO). Information to determine the modulation depth is derived from the speed-control signal by a simple non-linear circuit and is then converted by an analogue-to-digital converter into an 8-bit parallel digital signal.

A dedicated IC, type MAB8051, receives the clock signals from the VCO, the modulation-depth control number from the A/D converter, the direction-control logic signal, and logic inputs from the 'RUN' and 'STOP' switches. By applying digital multiplication processes to internal look-up table values, the microcomputer calculates the 'on-time' for each of the six power switches, and this process is repeated at regular intervals of 50µs, giving a carrier frequency of 20kHz. The pulses from the VCO are used for incrementing the pointers of the look-up table in the microcomputer, and thus control the motor speed.

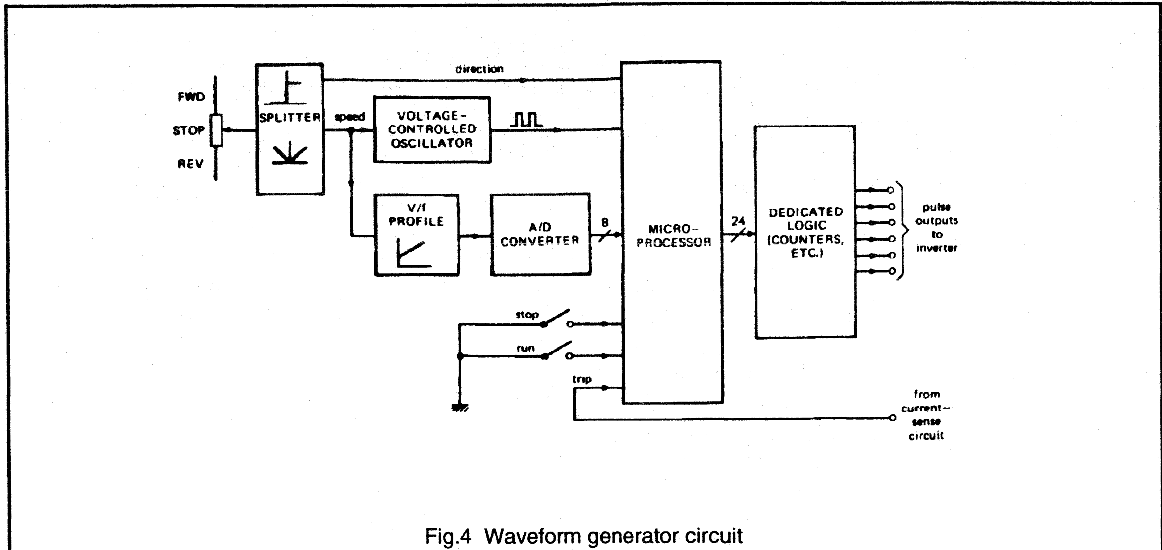


Fig.4 Waveform generator circuit

The output signals of the microcomputer are in the form of three 8-bit parallel numbers: each representing the duty-ratio for the next 50µs switching cycle for one pair of inverter switches, on a scale which represents 0% to 100% on-time for the upper switch and therefore also 100% to 0% on-time for the complementary lower switch. A dedicated logic circuit applies these three numbers from the microcomputer to digital counters and converts each number to a pair of pulse-widths. The two signals produced for each phase are complementary except for a small 'underlap' delay. This delay is necessary to ensure that the switch being turned off recovers its blocking voltage before its partner is turned on, thus preventing 'shoot-through'.

Other inputs to the microcomputer are the on/off switches, the motor direction logic signal, and the current-sensing signal. Each input triggers a processor interrupt, causing the appropriate action to be taken. The STOP switch and the overcurrent sense signals have the same effect, that of causing the microcomputer to instruct all six power switches in the inverter to turn off. The RUN switch causes the microcomputer to start producing output pulses. Any change in the direction signal first stops the microcomputer which then determines the new direction of rotation and adjusts its output phase rotation accordingly.

D.C. link and power supplies

The d.c. link and the low-voltage power supplies for the system are shown in Fig.5. The high voltage d.c. supply for the inverter is derived from a mains-fed bridge rectifier with a smoothing capacitor; the capacitor conducts both the 100Hz ripple from the rectified single-phase mains, and also the inverter switching ripple. A resistor, or alternatively a thermistor, limits the peak current in the rectifier while the capacitor is being charged initially. This resistor is shorted out by a relay after a time delay, so that the resistor does not dissipate power while the motor is running. As a safety measure, a second resistor discharges the d.c. link capacitor when the mains current is removed.

One of the d.c. link lines carries a low-value resistor to sense the d.c. link current. A simple opto-isolation circuit transmits a d.c. link current overload signal back to the signal processing circuit.

The logic circuitry of the waveform generator is powered conventionally by a 50Hz mains transformer, bridge rectifier, and smoothing capacitor. The transformer has two secondary windings; the second one provides power to a switched-mode power supply (SMPS), in which there is a switching transistor driven at about 60kHz to switch power through isolating transformers. Rectifying the a.c. outputs from the isolating transformers provides floating power supplies for the inverter gate drive circuits. As will be seen below, one supply is needed for the three 'lower' power switches (connected to a common d.c. link negative line), but three separate power supplies are needed for the three 'upper' switches (connected to the three inverter outputs). Thus four isolating transformers are required for the gate supply circuits. For low power systems the gate supplies can be derived directly from the d.c. link without excessive loss.

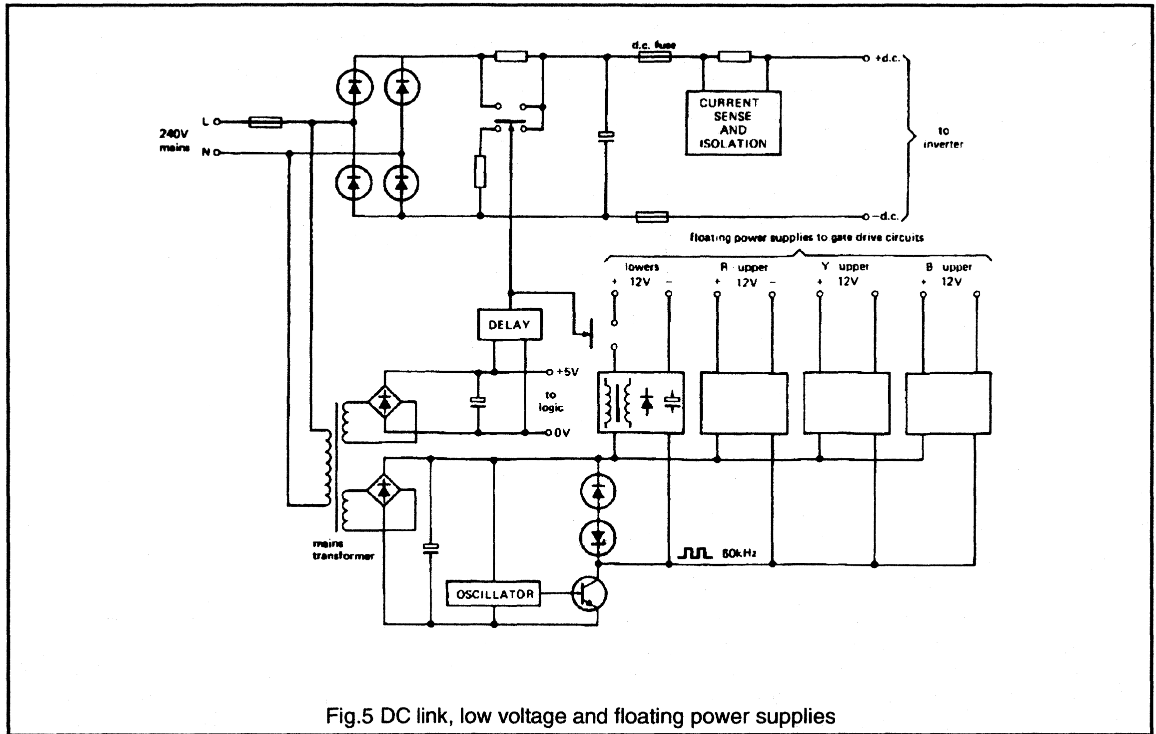


Fig.5 DC link, low voltage and floating power supplies

To prevent spurious turn-on of any inverter switch during the start-up process, the floating power supply to the lower three gate-drive circuits is connected only after a delay. The same delay is used for this as is used for the d.c. link charging-resistor bypass switch.

Signal isolation, gate drive, and inverter

The most important part of the system is the power inverter and it is the use of MOSFETs, with their short switching times, which makes it possible for the inverter to switch at 20kHz. It is in the area of the drive circuits to the power switches that using MOSFETs gives a saving in the number of components needed. Driving MOSFETs is relatively easy: the total power needed is very small because all that must be provided is the capability to charge and discharge the gate-source capacitance (typically between 1 and 2nF) by a few volts in a short time (less than 100ns). This ensures that the quality of the waveform is not degraded, and that switching losses are minimised.

In this circuit the six pulse outputs from the dedicated logic part of the waveform generator section are coupled to the MOSFET gate driver stages via pulse transformers. (see Fig.6). Each gate drive circuit is powered from one of the four floating power supplies described above. The three 'lower' stages share a common power supply, as the source terminals of the three 'lower' MOSFETs are all at the same potential. Each of the three 'upper' stages has its own floating power supply. The isolated signals are coupled to the gate terminals of the six MOSFETs by small amplifiers capable of delivering a few amperes peak current for a short time. Alternative gate driver circuits may use level shifting devices or opto-couplers. (Refer to "Power MOSFET Gate Drive Circuits" for further details.)

Fig.6 Signal isolation, gate drive, inverter and filter (one phase of three)

It will be seen from Fig.6 that each MOSFET has two associated diodes. These are necessary because the MOSFETs have built-in anti-parallel diodes with relatively long reverse-recovery times. If these internal diodes were allowed to conduct, then whenever load current commutated from a diode to the opposite MOSFET, a large current would be drawn from the d.c. supply for the duration of the diode reverse-recovery time. This would greatly increase the dissipation in the inverter. To avoid this, an external fast epitaxial diode is connected in anti-parallel with the MOSFET. Because the internal diode of the MOSFET has a very low forward voltage drop, a second low-voltage epitaxial diode must be connected in series with each MOSFET to prevent the internal diode from conducting at all. Thus, whenever the MOSFET is reverse-biased, it is the external anti-parallel diode which conducts, rather than the internal one. FREDFETs have internal diodes which are much faster than those of MOSFETs, opening the way for a further cost-saving by omitting the twelve diodes from the 3-phase inverter.

Output low-pass filter

For conventional, lower frequency inverters the size, weight and cost of output filter stages has held back their proliferation. An advantage of the constant high carrier frequency is that a small, economical low-pass filter can be designed to remove the carrier from the inverter output waveform. Compared with low frequency systems the filter component has been reduced by an order of magnitude, and can often be eliminated completely. In unfiltered systems cable screening becomes an important issue although on balance the increased cost of screening is less than the cost and weight of filter components.

A typical filter arrangement was shown in Fig.6. As an example, for a 50Hz motor-drive the filter would be designed with a corner-frequency of 100Hz, so that the attenuation at 20kHz would be about 46dB. The carrier frequency component superimposed on the output sinewave would therefore be only a few mV in 200Vrms. Fig.7 shows the relative spectral characteristics of different types of inverter switching strategies.

There are two main advantages in supplying the motor with pure sinewave power. First, the motor losses are small, because there is no rms motor current at the switching frequency, and second, there is less radio-frequency interference (RFI), because the switching frequency current components circulate entirely within the inverter and filter and do not reach the outside world.

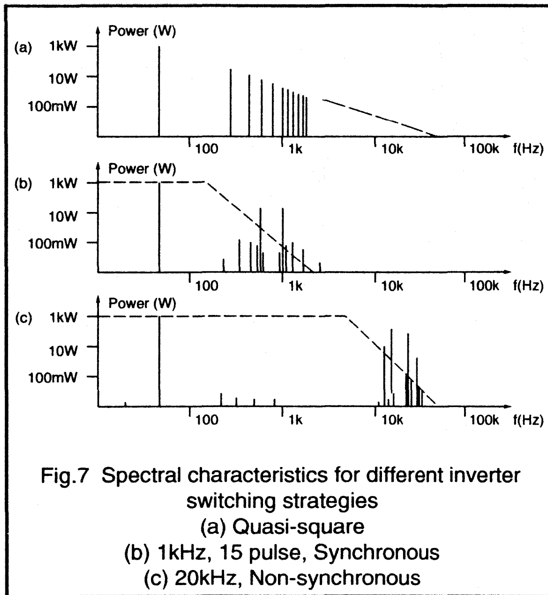


Fig.7 Spectral characteristics for different inverter switching strategies
(a) Quasi-square
(b) 1kHz, 15 pulse, Synchronous
(c) 20kHz, Non-synchronous

Advantages of a 20 kHz system

The principal advantages of the system described here are:

-Controller and motor are acoustically quiet.
-PWM waveform is simple and thus easy to generate.
-Output filter for removal of carrier is economic.
-RFI is low because of output filter.
-No snubbers are required on power devices.
-High efficiency is easily obtainable.
-No insertion loss.

3.1.2 The Effect of a MOSFETs Peak to Average Current Rating on Inverter Efficiency

The control of induction motors using a synthesised sinewave generated using pulse width modulation (PWM) control is becoming increasingly popular. The peak current requirement of switches used for the inverter bridge is based on the maximum current when the output is short circuited. The overcurrent during a short circuit fault is limited by an inductor connected in series with the switches. There is therefore a trade off between the peak current carrying capability of the switch and the size of the inductor. It is demonstrated in this note that the efficiency of the circuit during normal operation of the inverter is affected by the size of this choke. The ratio of peak to average current carrying capability of Philips Powermos is typcially about four. This compares favourably with the typical ratio of Insulated Gate Bipolar Transistors (IGBTs) which is about three.

A simplified diagram of the inverter and the windings of the induction motor is shown in Fig. 1. The MOSFETs are driven with a PWM signal as shown in Fig. 2. The voltages at the outputs of each leg of the inverter are smoothed using a low pass filter and the inductance of the motor windings. The system has the following advantages; it uses an induction motor which is relatively cheap and maintenance free and it has the facility for 0 to 100% speed control. The near perfect sinewaves generated by the PWM technique produce a smooth torque, audible noise is reduced and filtering is made easier since MOSFETs make possible the use of switching frequencies above 20 kHz.

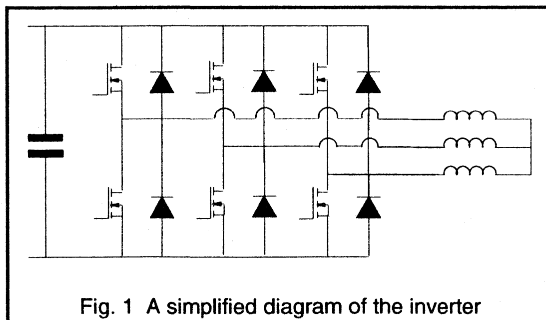


Fig. 1 A simplified diagram of the inverter

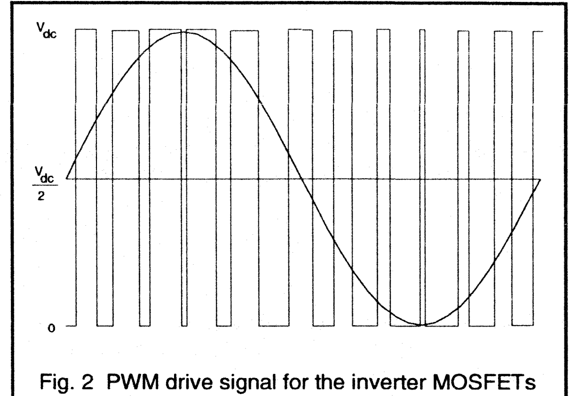


Fig. 2 PWM drive signal for the inverter MOSFETs

If the output of the inverter is short circuited there will be a rapid rise of current in the switches. To limit this peak current an inductor, L_S is often connected in each leg of the inverter as shown in Fig 3. The rate of rise of current under short circuit conditions, is then given in equation 1.

$$\frac{dI_T}{dt} = \frac{V_D}{L_s} \quad (1)$$

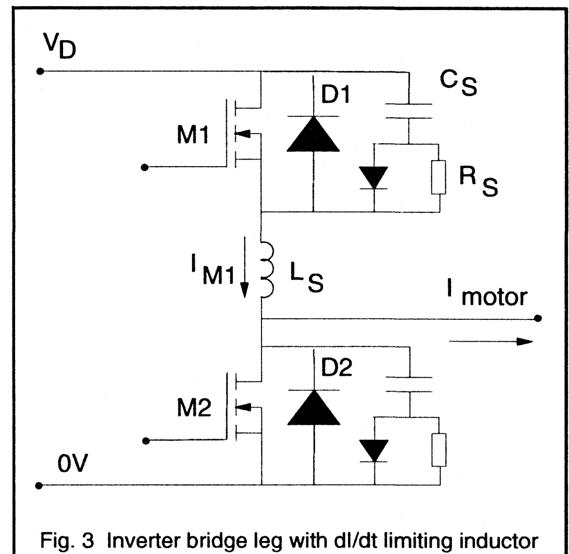


Fig. 3 Inverter bridge leg with dI/dt limiting inductor

When the MOSFETs turn this fault current (I_{SC}) off the energy in the inductor is transferred to a snubber capacitor, C_S. The overvoltage across the MOSFETs is given by equation 2.

$$V = \sqrt{\frac{L_s}{C_s}} \cdot I_{SC} \qquad (2)$$

The presence of inductor L_S affects the normal operation of the inverter. When the MOSFET M1 in Fig. 3 turns off the diode D2 does not turn on until the voltage across C_S is equal to the d.c. link voltage, V_D. If the diode did turn on then the rate of rise of current in L_S would be given by equation 3.

$$\frac{dI_{M1}}{dt} = \frac{V_D - V_{CS} - V_{diode}}{L_s} \qquad (3)$$

This would be greater than the rate of rise of motor current so $I_{M1} > I_{motor}$ and the diode would have to conduct in the reverse direction, which is clearly not possible.

During the time when the capacitor C_S is charging up to V_D, the voltage across L_S will always be such as to increase the current in the bottom MOSFET, I_{M1}. When V_{CS}=V_D the voltage across L_S will reverse and I_{M1} will fall. Diode D2 will now turn on. The energy stored in L_S will now be transferred to C_S. This energy will subsequently be dissipated in R_S and the MOSFET.

If the ratio of peak to average current carrying capability of the switch is large then it follows from equation 1 that L_S can be made smaller. This reduces the energy that is transferred to C_S when the MOSFETs switch off during normal operation. Hence the efficiency of the inverter is improved.

The short circuit fault current can be limited by connecting an inductor in the d.c. link as shown in Fig. 4. In this case analysis similar to that outlined above shows that the excellent ratio of peak to average current carrying capability of Philips Powermos again reduces the losses in the inverter. It has been shown that components chosen to ensure safe shutdown of inverters for motor drives can have deleterious effects on the efficiency of the inverter. In particular the addition of an inductor to limit the peak current through the semiconductor switches when the output is short circuited can increase the switching losses. The high peak to average current carrying capability of Philips Powermos reduces the size of this choke and the losses it causes.

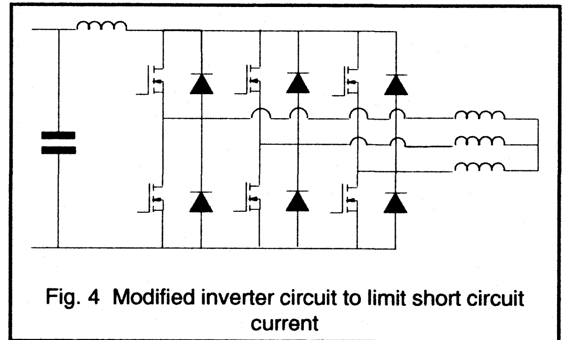


Fig. 4 Modified inverter circuit to limit short circuit current

3.1.3 MOSFETS and FREDFETS for Motor Drive Equipment

The paper discusses the properties of the FREDFET, a technology which yields a MOSFET with a very fast built-in reverse diode with properties similar to a discrete fast epitaxial rectifier. It is shown that its characteristics make the device an excellent choice for high frequency bridge leg systems such as 20 kHz AC motor control systems.

Investigations have been carried out in dedicated test circuits as well as in a 20 kHz ACMC system which show that the FREDFET exhibits very low diode losses. It compares favorably with a discrete solution, using two extra diodes to overcome the slow speed of the standard built-in diode, and also with devices from the present standard ranges.

1. Introduction

The Power MOSFET has inherent in its structure a large built-in diode which is present between the source and drain of the device. Under single switch applications such as forward and flyback converters, this diode isn't forward biased and consequently its presence can be ignored. In the case of bridge legs, however, this diode is forced into forward conduction and the properties of the diode become of prime importance. The reverse recovery of the built-in diode is relatively slow when compared with discrete fast recovery epitaxial diodes (FRED's). As a consequence, the currents flowing through the MOSFET and its diode can be high and the losses considerable.

These losses can be reduced through the application of two extra diodes as discussed in section 2. A more elegant solution is a MOSFET with a built-in diode which exhibits properties similar to discrete fast epitaxial rectifiers. The FREDFET has been designed to satisfy this requirement. This paper presents the results of studies, carried out with new FREDFETs, comparing them with both the conventional MOSFET and the discrete solution.

2. MOSFETS in half bridge circuits

MOSFETS have gained popularity in high frequency AC motor controllers, since they enable frequencies above 20kHz to be used. The short on-times required in ACMC systems make the use of bipolar devices very difficult, due to the storage times. Both the short switching times and the ease of drive of the MOSFET are essential ingredients in the design of a ultrasonic ACMC. Difficulties can arise, however, when trying to use the built in source to drain diode of the MOSFETs.

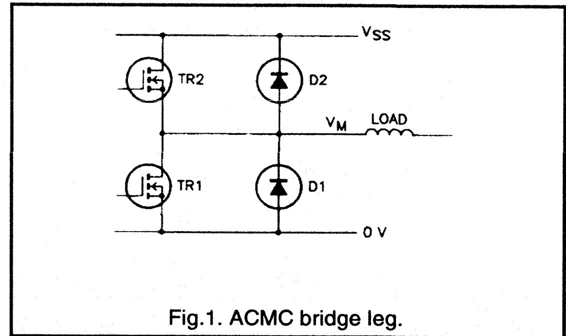


Fig.1. ACMC bridge leg.

One bridge leg of an ACMC is shown in Fig.1. When current is flowing out of the load, MOSFET T1 and freewheel diode D2 conduct alternately. Conversely, when flowing into the load, the current alternates between TR2 and D1. Consider the case when current is being delivered by the load, such that the pair TR1/D2 carries the current. When the MOSFET conducts current, the voltage at the drain is almost zero and the diode blocks. When the MOSFET is turned off by the drive circuit, the inductive load forces the voltage to increase making diode D2 conductive. Associated with conduction of the diode is a volume of stored charge which must be removed as the MOSFET TR1 returns to its on-state.

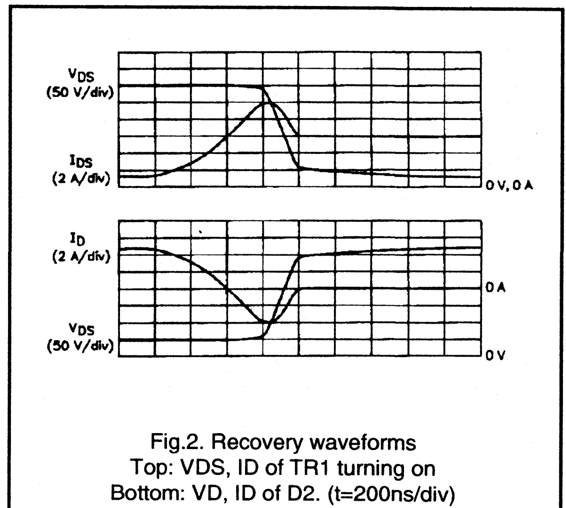


Fig.2. Recovery waveforms
Top: VDS, ID of TR1 turning on
Bottom: VD, ID of D2. (t=200ns/div)

The waveforms appropriate to this situation can be found in Fig.2. One may observe that during the diode recovery time, the voltage across the MOSFET remains high whilst at the same time its current increases rapidly. Temporarily

the drain current will increase to a level higher than the load current since the diode recovery current is added to it. Long recovery times and excessive charge storage result in a very high power dissipation in the MOSFET.

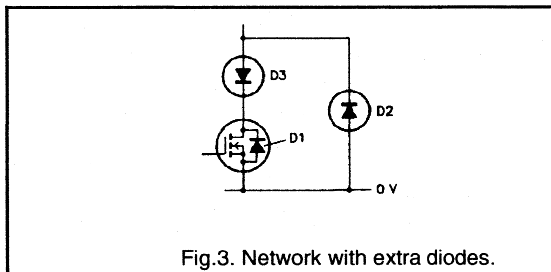


Fig.3. Network with extra diodes.

Using the inherent source drain diode of a conventional MOSFET as the freewheel diode results in considerable losses, since it is not optimised for fast switching or low stored charge. To avoid such losses the internal diode is usually deactivated by means of a special circuit (see Fig.3). This circuit, using two diodes D2 and D3, ensures that all freewheel current is flowing through the external diode D2 and not through the internal diode D1. When the MOSFET is switched on, the current flows via D3. This circuit is required for each MOSFET in the bridge. The FREDFET, which has a fast built-in diode offers the prospect of a much neater solution for these kind of circuits.

3. Technology of the FREDFET

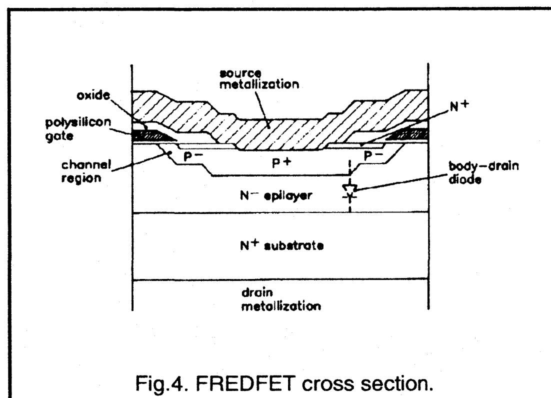


Fig.4. FREDFET cross section.

The power MOSFET is a majority carrier device and features fast turn-on and, in particular, fast turn-off. There are no charge storage effects such as in bipolar devices. In bridge leg applications the internal diode can become forward biased and the N- epitaxial region (see Fig.4) is flooded with holes, which must later be removed when the source becomes negatively biased again with respect to the drain.

The stored charge can be removed by holes diffusing from the N- epilayer into the P+ and P-body regions, and also by recombination of holes and electrons in the N- epitaxial region. A significant reduction in the stored charge Qrr can be achieved by doping the devices with heavy metal atoms to introduce recombination centres. A standard MOSFET will normally have a low concentration of recombination centres. In the FREDFET the heavy metal doping does not have any significant effects on the threshold voltage or the transconductance, however, the efficiency with which the extra recombination centres remove the stored charge is improved substantially. This can be observed when comparing Qrr and trr results for killed and non-killed devices as described in the next section.

4. FREDFET measurements

A comparison of the reverse recovery characteristics of the internal diode has been made for a BUK637-500B FREDFET and a similar competitor conventional MOSFET. The devices were tested using an 'LEM 20 A Qrr' gear.

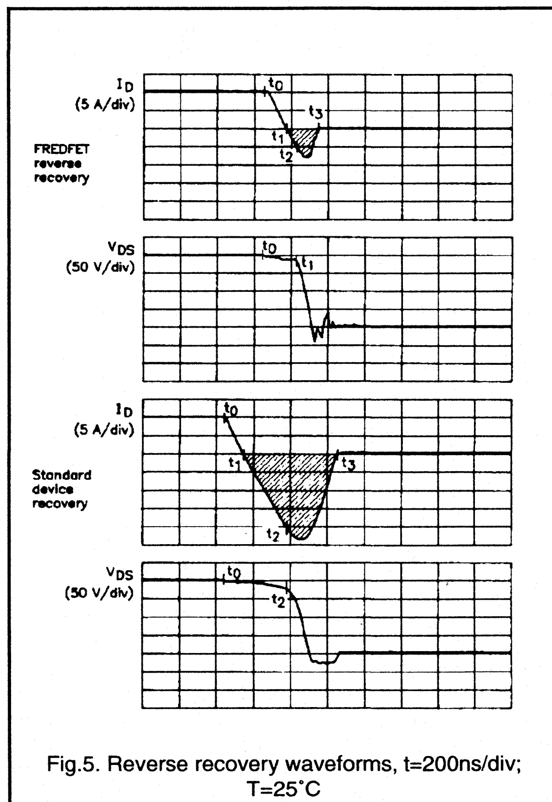


Fig.5. Reverse recovery waveforms, t=200ns/div; T=25˚C

Oscillograms are presented in fig.5. showing the test waveforms for both the FREDFET and the conventional device. The diode turn-off process commences at $t=t_0$, where upon the forward current (set at 10A) is reduced at a preset 100A/usec. The current falls through zero and the diode passes into reverse conduction signifying the removal of stored charge. At $t=t_2$ sufficient charge has been removed for the formation of a depletion layer across the p-n junction. The dI/dt starts to fall and a voltage builds across an inductance in the source circuit such that the source becomes negatively biased with respect to drain. Beyond t_2 the dI/dt reverses and the diode current begins to fall as the drain-source voltage rises to the clamp setting. The moment t_3 identifies the point at which the diode current has fallen to 10% of its peak value, Irrm.

The reverse recovery time, trr is defined as t_3-t_1 while the total stored charge Qrr is equal to the area of the shaded region, fig.5. A direct comparison of the diode reverse recovery at 25˚C is shown in fig.6. The respective values for trr, Qrr and Irrm are presented in Table 1.

T_j = 25˚C	trr (ns)	Qrr (uC)	Irrm (A)
BUK637-500B	193	1.2	8
Conventional device	492	7.5	23

Table 1.

It can be seen that Qrr is 84 % lower for the FREDFET while Irrm and trr approximately 60 % less. Fig.7 shows the same comparison measured at a junction temperature of 150˚C. Corresponding values of trr, Qrr and Irrm are shown in Table 2.

T_j = 150˚C	trr (ns)	Qrr (uC)	Irrm (A)
BUK637-500B	450	4.5	17
Conventional device	650	10.5	26

Table 2.

While higher temperatures are known to reduce the effectiveness of recombination centres, it is clear that significant improvements still exist even at the peak junction temperature with savings of 55 % in Qrr and over 30 % in Irrm and trr evident for the FREDFET

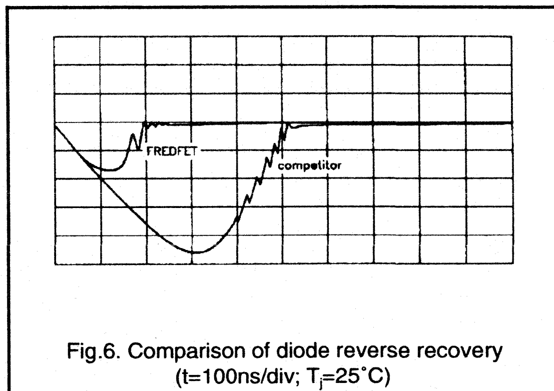


Fig.6. Comparison of diode reverse recovery (t=100ns/div; T_j=25˚C)

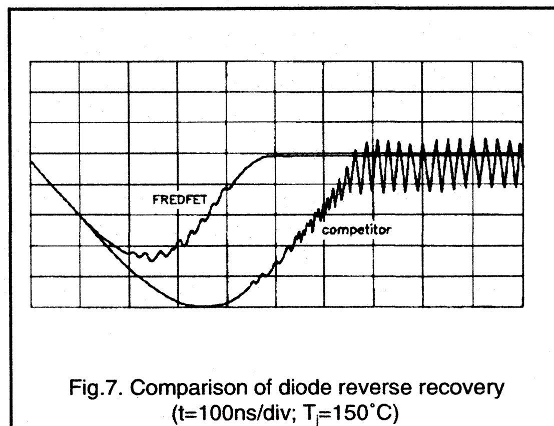


Fig.7. Comparison of diode reverse recovery (t=100ns/div; T_j=150˚C)

5. Performance in a bridge circuit

The circuit of Fig.8 is a simplified representation of a bridge circuit, and was used to evaluate the performance of the BUK637-500B FREDFET against a conventional MOSFET and a conventional MOSFET configured with both series and parallel diodes.

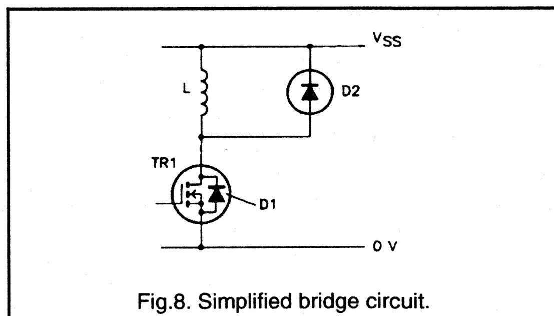


Fig.8. Simplified bridge circuit.

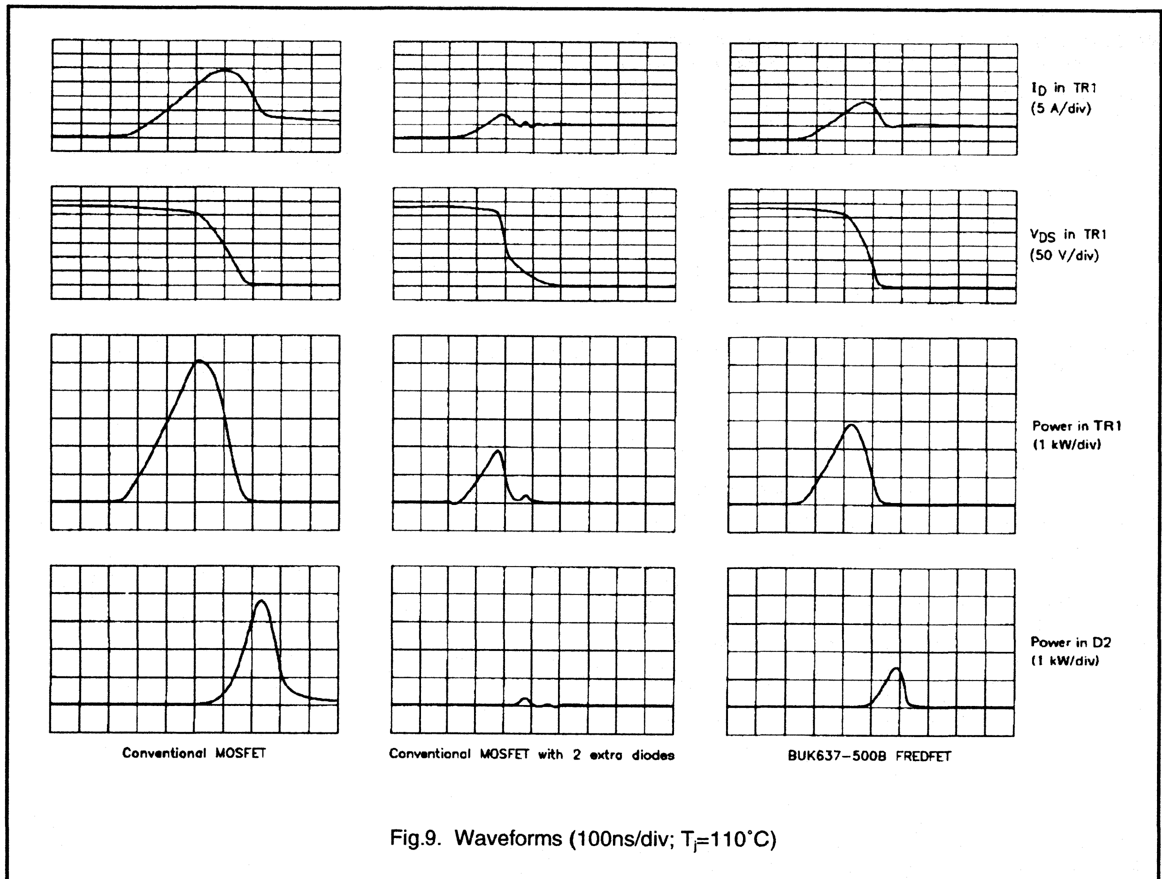


Fig.9. Waveforms (100ns/div; T_j=110˚C)

In each case the MOSFET in the bottom leg was switched on until the load current reached the desired value, at which point it was switched off, forcing the load current to flywheel through the inverse diode of the upper leg. The lower device was then switched on again to obtain reverse recovery of the upper diode. The current levels were set to simulate the conditions found in a 20 kHz 1 kVA ACMC. The device in the upper leg was mounted on a temperature controlled heatsink and the test was performed at very low duty cycle such that T_{case} approximated to T_j.

Oscillograms of current and voltage in relation to the lower leg are shown for the conventional device, conventional device plus external diodes and the FREDFET in Fig.9. The freewheel current in the upper diode is related to current in the MOSFET as shown in Fig.2. Also presented are the power waveforms for both the upper and lower legs in each case.

The superior performance of the FREDFET when compared to the conventional device is clear with the current overshoot kept to below 8 A compared to over 18 A using the latter. The lower reverse recovery current and faster trr are reflected in the power waveforms with nearly double the peak power being dissipated in the lower leg using a conventional device compared to that dissipated using the FREDFET. The power dissipated by the internal diode of the FREDFET is also observed to be remarkably reduced in comparison with the conventional MOSFET.

The performance of the three device implementations is summarised in table 3 which shows the total energy dissipated during switching in both legs for each case.

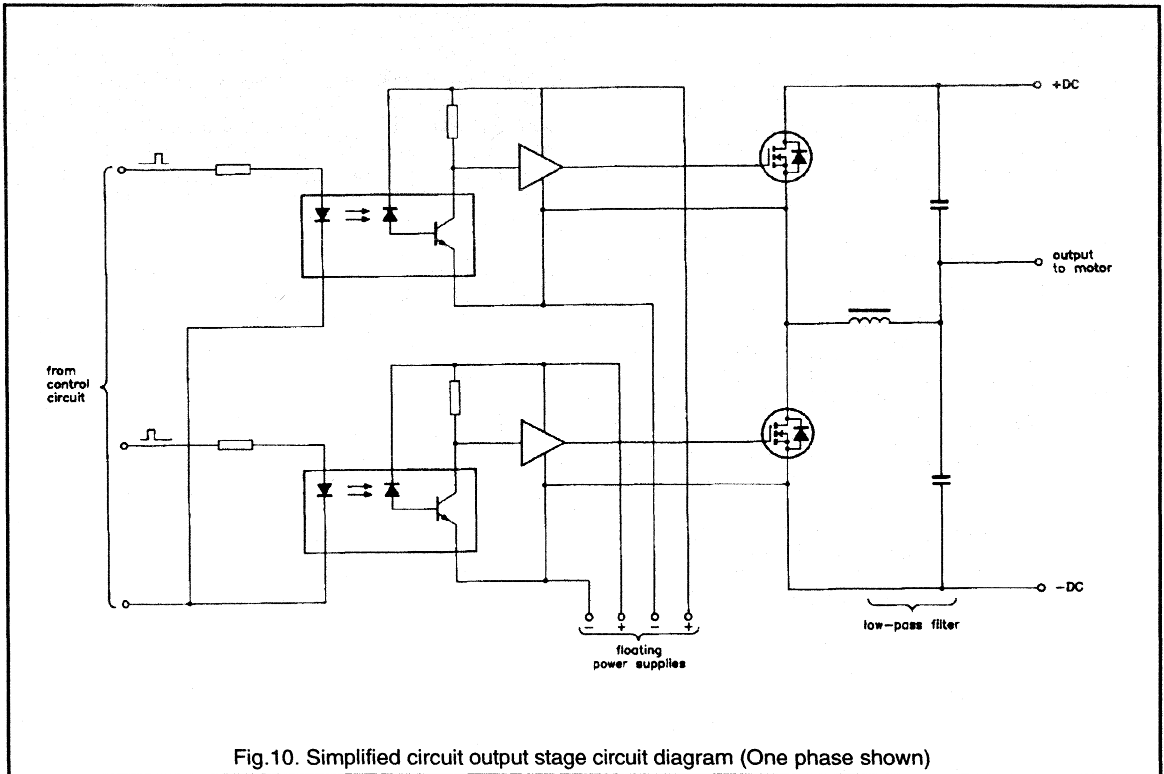


Fig.10. Simplified circuit output stage circuit diagram (One phase shown)

$T_j = 110^{\circ}C$	Energy Dissipated	
	Lower Leg (mJ)	Upper Leg (mJ)
Conventional MOSFET	1.2	0.533
MOSFET plus external diodes	0.2	0.035
BUK637-500B FREDFET	0.4	0.095

Table 3.

It can be seen that using a conventional MOSFET without the external diode circuitry involves a six fold increase in the energy dissipated in the MOSFET. However if a FREDFET implementation is used the turn-on energy is only a factor of two above the minimum achievable with the extra diodes. Energy loss in the diode itself is relatively small for both the FREDFET and the external diode configuration, being less than 25 % that dissipated in the lower leg. For the conventional device the diode loss is more significant, equal to 44 % of the power dissipated during turn-on in the lower leg. The energy value presented above represent only the losses during turn-on, in addition to these are the on-state losses which for the external diode configuration include the extra power dissipated by the series diode.

6. 20 kHz ACMC with FREDFETS

The three device options discussed above have each been implemented in a 20 kHz AC Motor Control circuit. The inverter provides a three phase 1 kVA output from a single phase mains input. A simplified diagram of one of the output stages is presented in Fig.10.

Figure 11 shows the current waveforms as the load current commutates from the upper leg (anti-parallel diode in conduction) to the lower leg (turn-on of the MOSFET) for each device option. In each case the load current is 4.5 A. Fig.11a illustrates the large overshoot current obtained with a conventional device while Fig.11b shows what is achieved when the two external diodes are incorporated. Finally Fig.11c shows the current waveform for the FREDFET implementation where the current overshoot is kept below 1.5 A by the built-in fast recovery diode of the device.

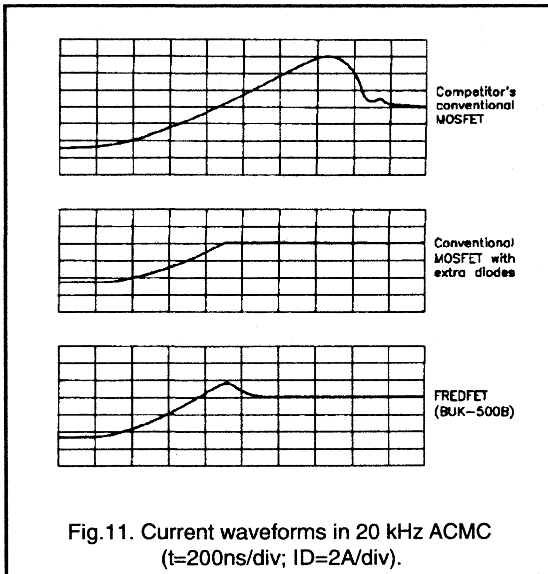


Fig.11. Current waveforms in 20 kHz ACMC (t=200ns/div; ID=2A/div).

7. Conclusions

It has been shown that the FREDFET compares favorably in ACMC systems compared with the standard MOSFET. The normally employed extra diodes can be omitted thus saving considerable costs in the system. The fast internal diode is seen to be comparable with the normally used fast epitaxial rectifiers and enables a simple ultrasonic ACMC.

3.1.4 A Designers Guide to PowerMOS Devices for Motor Control

This section is intended to be used as a designers guide to the use and selection of power MOSFETS and FREDFETS in a.c. motor control (ACMC) applications. It is particularly concerned with the variable speed operation of induction motors using pulse width modulation (PWM) techniques. One of the most important considerations in the design of ACMC inverters is the optimum choice of power switching device and heatsinking arrangement. Other factors which relate to the losses in the power switch are switching speed and design of suitable gate drive circuits. This section addresses each of these factors and presents a series of design graphs relating system operating temperature to device type and heatsink size for systems rated up to 2.2kW and operated from a single phase supply.

Introduction

Variable speed control of induction motors is a widespread requirement in both industrial and domestic applications. The advantages of an induction motor drive over alternative systems such as d.c. motor controllers include:

- -high reliability and long life
- -low maintenance requirements
- -brushless operation
- -availability of standard machines.

With the advent of power switching devices able to provide the required ratings for ACMC applications and the availability of fast PWM pattern generation circuits these advantages have lead to an increasing number of applications where the inverter-fed induction motor system produces a cost effective drive. Before considering in detail the use of MOSFETs and FREDFETs in ACMC inverters it is worth briefly considering the principles and operation of the induction motor, the PWM method of voltage control and the characteristics of the switching devices.

The induction motor

Induction motors are three phase machines where the speed of rotation of the stator field (the synchronous speed, N_s) is determined by the number of poles, p, and the frequency of the applied voltage waveforms, f_s.

$$N_s = \frac{120.f_s}{p} \quad \text{(rpm)} \tag{1}$$

Torque production in an induction motor is due to the interaction of the rotating stator field and currents in the rotor conductors. Torque is developed when the rotor speed 'slips' behind the synchronous speed of the stator travelling field. Fig.1 shows the torque-speed characteristic of an induction motor where ω_s is the speed of the stator field ($\omega_s=2\pi f_s$) and ω_r is the rotor speed. The difference between the two is usually relatively small and is the slip speed. The solid portion of the characteristic is the main region of interest where the motor is operating at rated flux and at low slip. In this region the rotor speed is approximately proportional to the stator supply frequency, except at very low speeds. The operating point of the motor on its torque-speed characteristic is at the intersection of the load torque line and the motor characteristic. For small amounts of slip and at constant airgap flux the motor torque is proportional to the slip speed.

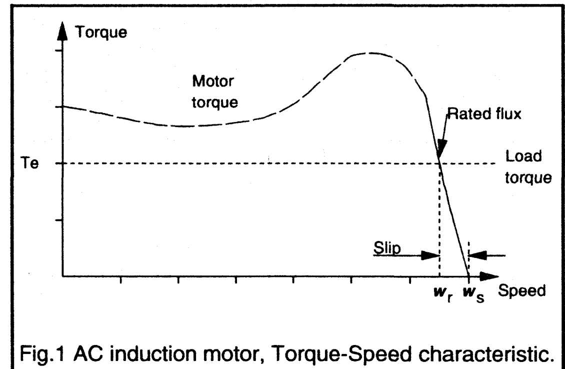


Fig.1 AC induction motor, Torque-Speed characteristic.

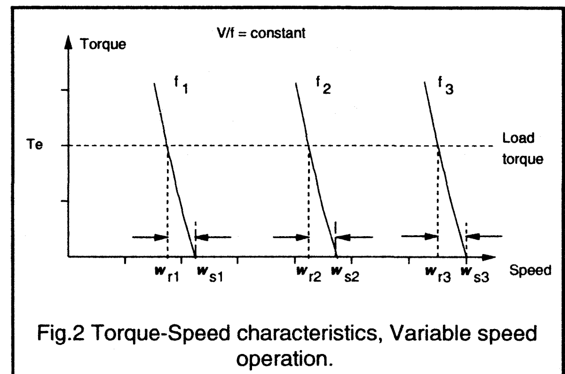


Fig.2 Torque-Speed characteristics, Variable speed operation.

In a variable speed system the motor is operated on a series of torque-speed characteristics as the applied frequency is increased. Fig.2 shows a set of characteristics for three conditions, ω_{s1}, ω_{s2} and ω_{s3}. The corresponding rotor speeds are ω_{r1}, ω_{r2} and ω_{r3}. However in order that the airgap flux in the motor is maintained at its rated value then the applied voltage must be reduced in proportion to the applied

frequency of the travelling field. This condition for constant airgap flux gives the constant v/f requirement for variable speed control of a.c. induction motors. At low speeds this requirement may be modified by voltage boosting the supply to the motor in order to overcome the increased proportion of 'iR' voltage drop in the motor windings which occurs at low speeds.

The PWM Inverter

A variable voltage, variable frequency three phase supply for the a.c. induction motor can be generated by the use of a pulse width modulated (PWM) inverter. A schematic diagram of the system is shown in Fig.3. The system consists of a rectified single phase a.c. supply, which is usually smoothed to provide the d.c. supply rails for the main switching devices. Alternate devices in each inverter leg are switched at a high carrier frequency in order to provide the applied voltage waveforms to the motor. During each switching cycle the motor current remains approximately constant due to the inductive nature of the AC motor load.

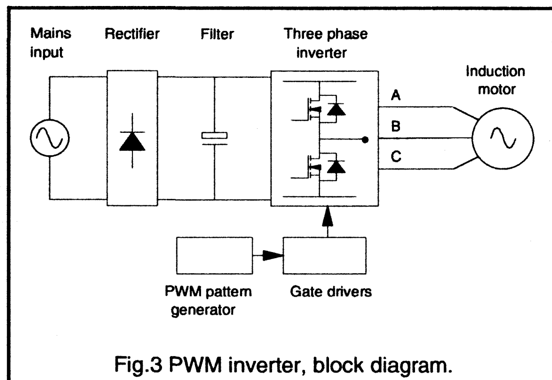


Fig.3 PWM inverter, block diagram.

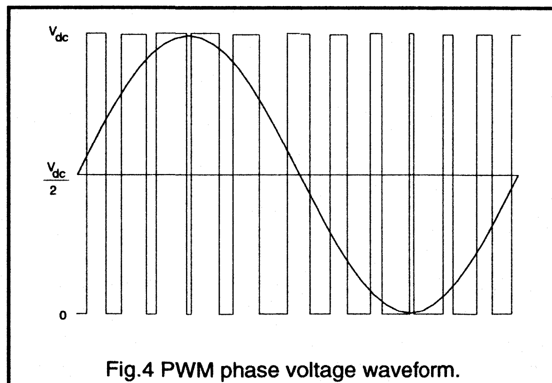


Fig.4 PWM phase voltage waveform.

In the circuit of Fig.3 the main switching devices are MOSFETs and each MOSFET has a freewheeling diode connected in antiparallel. The motor load current is determined by the circuit conditions. When the load current in a particular phase is flowing into the motor then conduction alternates between the top MOSFET and the bottom freewheel diode in that inverter leg. When the load current is flowing from the motor then the bottom MOSFET and top diode conduct alternately. Fig.4 shows a typical sinusoidal PWM voltage waveform for one motor phase. The three phases are maintained at 120° relative to each other.

Both the frequency and amplitude of the fundamental component of the output voltage waveform can be varied by controlling the timing of the switching signals to the inverter devices. A dedicated i.c. is usually used to generate the switching signals in order to maintain the required v/f ratio for a particular system.[1] The PWM algorithm introduces a delay between the switching signal applied to the MOSFETs in each inverter leg which allows for the finite switching times of the devices and thus protects the system from shoot-through conditions.

Additional harmonic components of output voltage, such as the third harmonic, can be added to the PWM switching waveform.[2,3] The effect of adding third harmonic to the output voltage waveform is to increase the amplitude of the fundamental component of output voltage from a fixed d.c. link voltage. This is shown in Fig.5. The third harmonic component of output phase voltage does not appear in the output line voltage due to the voltage cancellation which occurs in a balanced three phase system. Using this technique it is possible to obtain an output line voltage at the motor terminals which is nearly equal to the voltage of the single phase supply to the system.

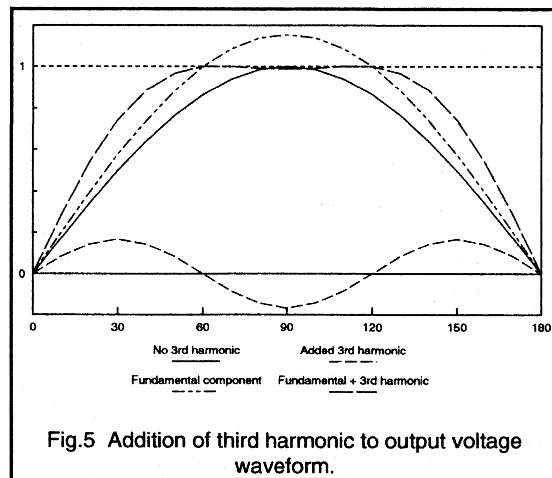


Fig.5 Addition of third harmonic to output voltage waveform.

For many applications the PWM ACMC system is operated at switching speeds in the range 1kHz to 20kHz and above. Operation at ultrasonic frequencies has advantages that the audible noise and RFI interference are considerably reduced. The advantages of PowerMOS devices over bipolar switching devices are most significant at these switching speeds due to the low switching times of PowerMOS devices. Additional advantages include good overload capability and the fact that snubber circuits are not usually required. It is usually straightforward to operate PowerMOS devices in parallel to achieve higher system currents than can be achieved with single devices. This is because the devices have a positive temperature coefficient of resistance and so share the load current equally. The simple gate drive requirements of PowerMOS devices means that a single gate circuit can often be used for a range of devices without modification.

MOSFETs and FREDFETs in ACMC

One of the features associated with the transfer of conduction between the switching devices and the freewheel diodes in an inverter circuit is the reverse recovery of the freewheel diode as each conducting MOSFET returns to its on-state. Reverse recovery current flows due to the removal of stored charge from a diode following conduction. Fig.6 shows the device current paths in an inverter leg when conduction is transferred from the top diode to the bottom MOSFET.

The switching waveforms are shown in Fig.7 where the diode reverse recovery current is I_{rr} and the time taken for the reverse recovery currents to be cleared is t_{rr}. The amount of stored charge removed from the body of the diode is represented by the area Q_{rr}. The reverse recovery current flows through the MOSFET which is being turned on in addition to the load current and thus causes additional turn-on losses. The amount of stored charge increases with increasing temperature for a given diode. Both the magnitude of the reverse recovery current and its duration must be reduced in order to reduce the switching losses of the system.

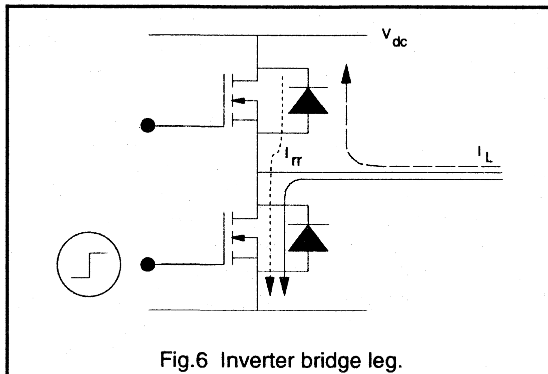


Fig.6 Inverter bridge leg.

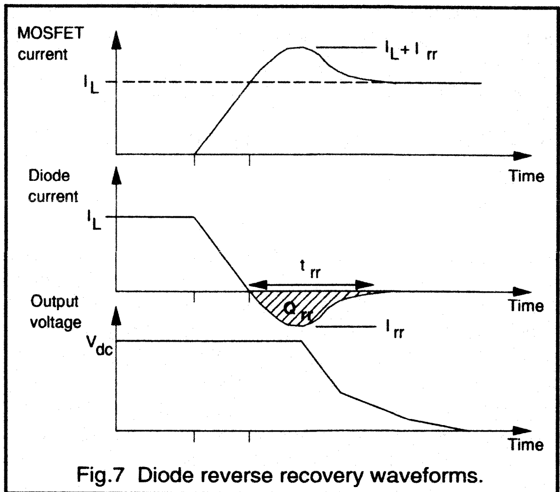


Fig.7 Diode reverse recovery waveforms.

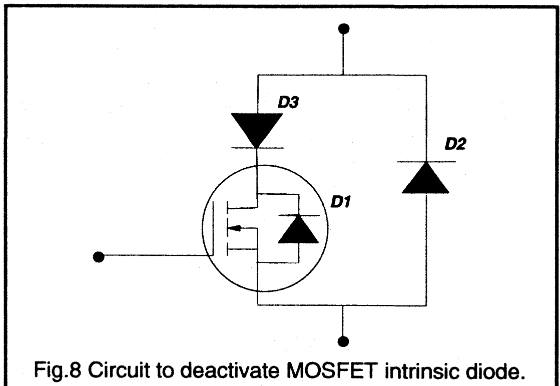


Fig.8 Circuit to deactivate MOSFET intrinsic diode.

This effect is important because inherent in the structure of a power MOSFET is a diode between the source and drain of the device which can act as a freewheeling diode in an inverter bridge circuit. The characteristics of this diode are not particularly suited to its use as a freewheel diode due to its excessive charge storage and long recovery time. These would lead to large losses and overcurrents during the MOSFET turn-on cycle.

In inverter applications the internal diode of a MOSFET is usually deactivated by the circuit of Fig.8. Conduction by the internal MOSFET diode is blocked by the series Schottky diode (D3). This series device must carry all the MOSFET current and so contributes to the total conduction losses. The external diode, usually a fast recovery epitaxial diode (FRED), carries the freewheel current. This device is chosen such that its low values of I_{rr} and t_{rr} reduce the overall switching losses.The FREDFET is essentially a MOSFET with a very fast built-in diode, and hence can replace the network of Fig.8 with a single device giving a very compact ACMC inverter design using only six power switches.[4] The

reverse recovery properties of a FREDFET diode are similar to those of a discrete FRED thus giving a considerably neater circuit without any loss in switching performance.

ACMC design considerations

Voltage rating

The first selection criteria for a PowerMOS device in an inverter application is the voltage rating. For a 240V a.c. single phase supply the peak voltage is 340V. Assuming that the rectifier filter removes the voltage ripple components which occur at twice the mains frequency, and dependent on the values of the filter components and rectifier conduction voltage, then the dc link voltage will be around 320V. Devices with a voltage rating of 500V will allow sufficient capability for transient overvoltages to be well within the capability of the device. Thus the dc link voltage is given by:

$$V_{dc} = \sqrt{2}.V_{ac} \qquad (2)$$

where V_{ac} is the rms ac input line voltage.

The output phase voltage, shown in Fig.4, switches between the positive and negative inverter rail voltages. The mean value of the output voltage is $V_{dc}/2$. Neglecting the delays which occur due to the finite switching times of the devices then the maximum rms output phase voltage is given by:

$$V_{ph} = \frac{1}{\sqrt{2}}.\frac{V_{dc}}{2} \qquad (3)$$

and hence the rms output line voltage is:

$$V_{line} = \sqrt{3}.V_{ph} = \sqrt{3}.\frac{V_{dc}}{2.\sqrt{2}} \qquad (4)$$

Comparing equations (2) and (4) shows that:

$$V_{line} = 0.866.V_{ac} \qquad (5)$$

This shows that the fundamental rms line output voltage is 13% less than the rms ac input voltage. Adding third harmonic to the PWM output waveform can restore this rms output voltage to the ac input voltage. In a practical system the effect of switching delays and device conduction voltages can reduce the output voltage by upto 10-15%.

Current rating

The nameplate rating of an induction motor is usually quoted in terms of its power (W) and power factor (cosφ). The VA requirement of the inverter is found from the simple equation:

$$Power(W) = \eta.\cos\varphi.VA \qquad (6)$$

where η is the efficiency. In terms of the rms motor line voltage (V_{line}) and output current (I_L):

$$VA = \sqrt{3}.V_{line}.I_L \qquad (7)$$

The efficiency of small ac induction motors can be quite high but they usually run at quite poor power factors, even at rated conditions. For small induction motors (<2.2kW) the efficiency-power factor product is typically in the range 0.55 to 0.65. The exact value will vary from motor to motor and improves with increasing size. Thus from equations (6) and (7) it is possible to calculate the approximate rms current requirement. The peak device current for sinusoidal operation is given by equation (8). (NB. The devices will experience currents in excess of this value at switching instants.)

$$I_{max} = \sqrt{2}.I_L \qquad (8)$$

Device package

The device package chosen for a particular application will depend upon device rating, as discussed above, as well as circuit layout and heatsinking considerations. Philips PowerMOS devices are available in a range of package types to suit most applications. These include the ISOTOP package which is especially useful for higher power applications giving good isolation voltage-capability, low thermal resistance and ease of mounting the device on a heatsink.

Drive considerations

Unlike bipolar devices the MOSFET is a majority carrier device and so no minority carriers must be moved in and out of the device as it turns on and off. This gives the fast switching performance of MOSFET devices. During switching instants the only current which must be supplied by the gate drive is that required to charge and discharge the device capacitances. In order to switch the device quickly the gate driver must be able to rapidly sink and source currents of upto 1A. For high frequency systems the effect of good gate drive design to control switching times is important as the switching losses can be a significant proportion of the total system losses.

Fig.9 shows an equivalent circuit of the device with the simplest gate drive arrangement. The drain-source capacitance does not significantly affect the switching performance of the device. Temperature only has a small effect on the values of these capacitances and so the device switching times are essentially independent of temperature. The device capacitances, especially C_{GD}, vary with V_{DS} and this variation is plotted in data for all PowerMOS devices.

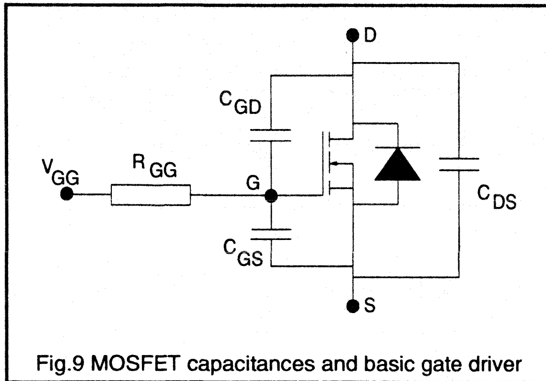


Fig.9 MOSFET capacitances and basic gate driver

Turn-on (Fig. *10*)

A turn-on gate voltage pulse commences at t_0. The gate voltage v_{GS} rises as current flows into the device via R_{GG}. C_{GS} starts to charge up until v_{GS} reaches its threshold value $v_{GS(TO)}$ at time t_1. The device is now operating in its active region with a relatively high power loss. The MOSFET current, rises as a function of v_{GS}-$v_{GS(TO)}$ and causes a corresponding fall in the diode current. Thus the rate of fall of diode current, and hence the amount of diode reverse recovery current, is controllable by the rate of rise of v_{GS}. At time t_4 the diode has recovered and the MOSFET current is equal to the load current, I_L. V_{GS} is clamped to $v_{GS(IL)}$ and so the gate current is given by:

$$i_G = \frac{v_{GG} - v_{GS(IL)}}{R_{GG}} \tag{9}$$

This current flows through C_{GD}, discharging it and so the rate of fall of output voltage is given by:

$$\frac{dv_{DS}}{dt} = \frac{i_G}{C_{GD}} = \frac{(v_{GG} - v_{GS(IL)})}{R_{GG} \cdot C_{GD}} \tag{10}$$

The fall in v_{DS} commencing at time t_3 is not linear, principally because C_{GD} increases with reducing v_{DS}. At time t_5 C_{GD} is fully discharged and the device is on. The gate voltage continues to charge up to its final value, v_{GG}. It is usual to have a value of v_{GG} significantly higher than $v_{GS(IL)}$ because $r_{DS(on)}$ falls with increasing v_{GS}. Additionally a high value if v_{GG} speeds up the turn-on time of the device and provides some noise immunity.

Switching losses occur during the period t_1 to t_5. The minimum turn-on time is usually governed by the dv/dt capability of the system. Reducing the turn-on time increases the amount of diode reverse recovery current and hence increases the peak power dissipation, however the total power dissipated tends to reduce.

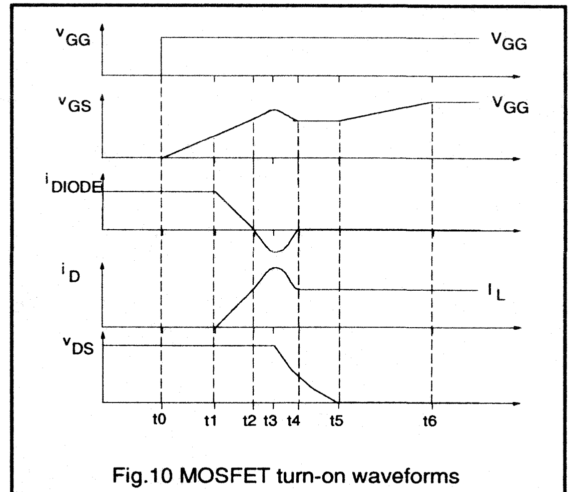


Fig.10 MOSFET turn-on waveforms

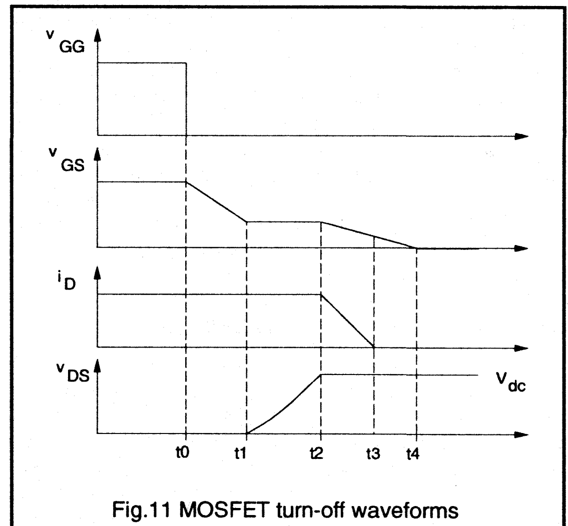


Fig.11 MOSFET turn-off waveforms

Turn-off (Fig. *11*)

Unlike the conditions which occur at turn-on there is no interaction between the switching devices at turn-off. The switching waveforms are, therefore, relatively straightforward. The gate voltage is switched to ground or, if very fast turn-off is required, to a negative voltage. During the delay time t_0 to t_1 the gate voltage falls to the value required to maintain the output current, I_O. From time t_1 to t_2 the gate supply is sinking current and C_{GD} charges the drain up to the positive rail voltage. V_{GS} then continues to fall and so the device current falls between times t_2 and t_3. At t_3 the gate voltage falls below its threshold value and the device turns off. The rate of rise of output voltage is:

$$\frac{dv_{DS}}{dt} = \frac{i_G}{C_{GD}} = \frac{v_{GS(IL)}}{R_{GG}.C_{GD}} \quad (11)$$

Parasitic turn-on

In a high frequency system the device switching times are necessarily short and so the rates of change of inverter output voltage are high. The high values of dv/dt which occur when one device turns on can cause a sufficiently high voltage at the gate of the other device to also turn it on. The coupling occurs via C_{GD} and C_{GS}. If the rate of change of output voltage due to one device turning on is given by dv_{DS}/dt then the voltage that would be seen at the gate of the other device if it were left open circuit is:

$$\frac{dv_{GS}}{dt} = \frac{C_{GD}}{C_{GS}+C_{GD}} \cdot \frac{dv_{DS}}{dt} \quad (12)$$

If C_{GS} is shorted out by a zero impedance, then clearly dV_{GS}/dt can be reduced to zero. In practice achieving a zero impedance in the gate-source circuit is extremely difficult and dV_{GS}/dt will not be zero. In the worst case this rising gate voltage will turn the device fully on and a destructive shoot-through condition occur. If the conditions are less severe then the MOSFET may only turn on for a short period of time giving rise to an additional overcurrent in the turn-on cycle of the device being switched. Parasitic turn-on, as this effect is referred to, must be prevented by either limiting dv_{DS}/dt or by ensuring that v_{GS} is clamped off. In systems where the off-state gate-source voltage is negative then the possibility of parasitic turn-on can be reduced.

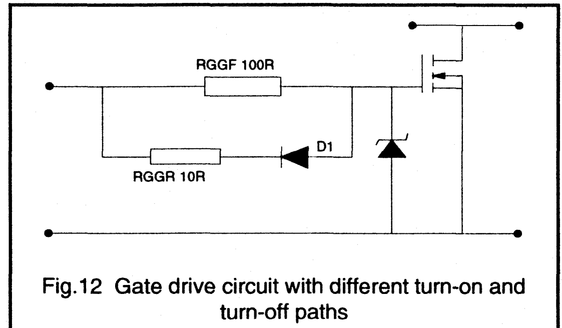


Fig.12 Gate drive circuit with different turn-on and turn-off paths

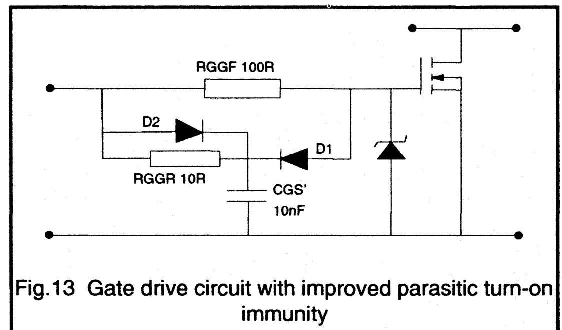


Fig.13 Gate drive circuit with improved parasitic turn-on immunity

Gate drive circuits for ACMC inverters

The previous section discussed device switching waveforms using a resistive gate drive circuit. In this section various alternative gate drive circuits for ACMC applications are presented and compared. The discussion assumes that each MOSFET gate drive circuit is isolated and driven using a CMOS buffer capable of sinking and sourcing the required gate current. In unbuffered gate drive circuits the leakage inductance of an isolating pulse transformer can increase the gate impedance, thus reducing the maximum possible switching rate and making the MOSFET more susceptible to parasitic turn-on. A zener diode clamp protects the gate-source boundary from destructive overvoltages. Identical drivers are used for the top and bottom devices in each inverter leg. The gate drive circuits presented here were tested using BUK638-500A FREDFETS and BUK438-500A MOSFETS in a 20kHz, 2.2kW ACMC system.

Figure 12 shows the simplest arrangement which gives independent control of the turn-on and turn-off of the MOSFET. Increasing the gate impedance to reduce dV_{DS}/dt levels will raise the susceptibility to parasitic turn-on problems. The gate-source voltage can be clamped off more effectively if the dynamic impedance between gate and source is reduced as shown in the circuit of Fig.13. The additional gate-source capacitance ensures that v_{GS} does not rise excessively during conditions when parasitic turn-on could occur (Equation 12). The external capacitor C_{GS}' must be charged up at turn-on. If C_{GS}' is made too large then the current required may be beyond the rating of the drive buffer. The speed-up diode, D2, ensures that the turn-on is not compromised by C_{GS}'and R_{GGR}. At turn off the additional capacitance slows down dI_D/dt since the gate-source RC time constant is increased. It must be noted that one effect of the turn-off diode, D1, is to hold the off-state value of v_{GS} above 0V, and hence somewhat closer to the threshold voltage of the device.

An alternative circuit which may be used to hold the MOSFET off-state gate-source voltage below its threshold value is shown in Fig.14. The pnp transistor turns on if the gate-source voltage is pulled up via C_{GD} and C_{GS} and thus the device remains clamped off.

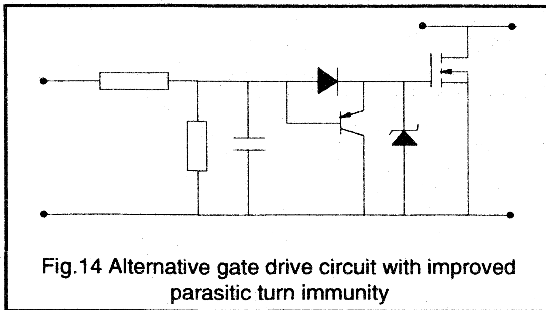


Fig.14 Alternative gate drive circuit with improved parasitic turn immunity

Parallelling of PowerMOS devices

Moving to a system using parallelled MOSFETs requires only slight modifications to the gate drive circuit. One consideration may be the capability of the drive buffer to provide the currents required at the switching instants. The switching speed of the system can be maintained. using a lower impedance gate drive. It is recommended that small differential resistors, as shown in Fig.15, are used to damp out any oscillations which may occur between the switching devices and the rest of the circuit. The circuit of Fig.13 can be modified for operation with parallelled devices to that shown in Fig.16.

Circuit layout considerations

The effects of poor circuit design and layout are to increase RFI and noise and to compromise the performance and speed of the system due to stray inductances. The precautions which must be taken to minimise the amount of stray inductance in the circuit include:

- positioning the gate drive circuits, especially zener diodes and dv/dt clamping circuits as close as possible to the power MOSFETs.
- reducing circuit board track lengths to a minimum and using twisted pairs for all interconnections.
- for parallelled devices, keeping the devices close to each other and keeping all connections short and symmetrical.

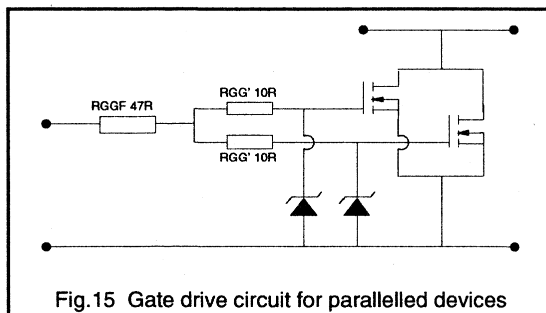


Fig.15 Gate drive circuit for parallelled devices

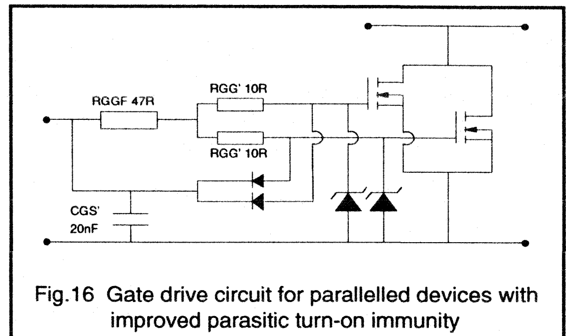


Fig.16 Gate drive circuit for parallelled devices with improved parasitic turn-on immunity

Modelling of parasitic turn-on

Using the simple MOSFET model of Fig.9 it is possible to study the susceptibility to parasitic turn-on of alternative gate drive circuits. Considering the switching instant when the bottom MOSFET is held off and the top MOSFET is switched on, the voltage across the bottom MOSFET swings from the negative inverter rail to the positive one. The switching transient can be modelled by an imposed dv_{DS}/dt across C_{GD} and C_{GS} and hence the effect of gate circuit design and dv_{DS}/dt on v_{GS} can be studied using simple SPICE models.

Typical data sheet values of C_{GD} and C_{GS} for a 500V MOSFET were used. The simulated results assume constant dv_{DS}/dt, that freewheel diode reverse recovery can be neglected and that the off-state gate drive buffer output is at 0V with a sink impedance of around 5Ω. In practice the dv_{DS}/dt causing parasitic turn-on is not constant and is only at its maximum value for a small proportion of the voltage transition. Thus the results shows here represent a 'worst-case' condition for the alternative gate drive circuits used to clamp v_{GS} to below its threshold value, typically 2V to 3V. (The simple circuit model used here ceases to become valid once v_{GS} reaches $v_{GS(TO)}$ (time t_1 in Fig.10) when the MOSFET starts to turn on.)

Fig.17 shows the relevant waveforms for the circuit of Fig.9 with R_{GG}=100Ω. The top waveform in Fig.17 shows an imposed dv_{DS}/dt of 3.5V/ns and a dc link voltage of 330V. The centre trace of Fig.17 shows that v_{GS} rises quickly (reaching 3V in 25ns); at this point the MOSFET would start to turn on. The bottom trace shows the C_{GD} charging current sinking through the gate drive resistor R_{GG}. For the circuit of Fig.12 with R_{GGF}=100Ω and R_{GGR}=10Ω, Fig.18 shows that the gate source voltage is held down by the reduced drive impedance but still reaches 3V after 35ns.

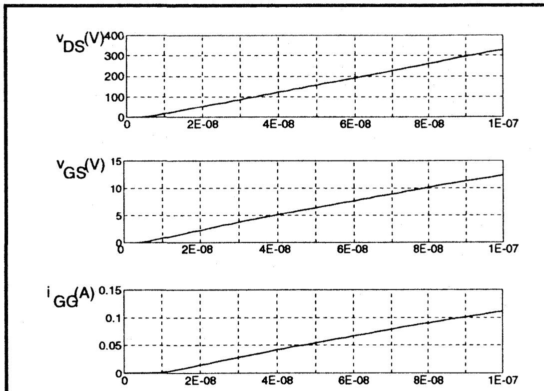


Fig. *17* Parasitic turn-on waveforms for circuit of Fig.9

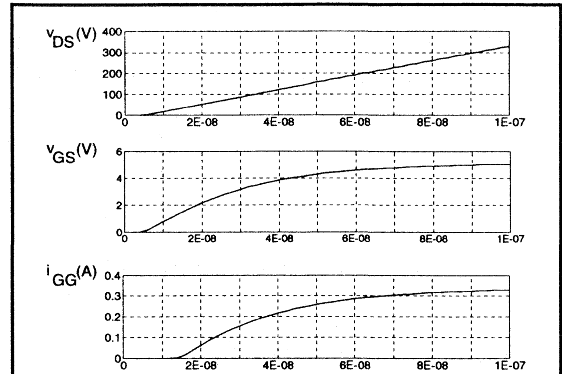


Fig. *18* Parasitic turn-on waveforms for circuit of Fig.12

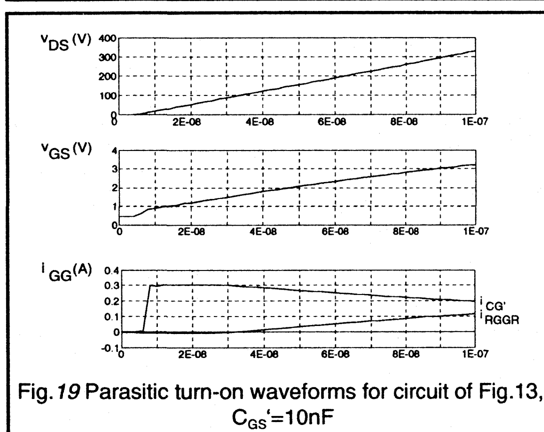


Fig. *19* Parasitic turn-on waveforms for circuit of Fig.13, C_{GS}'=10nF

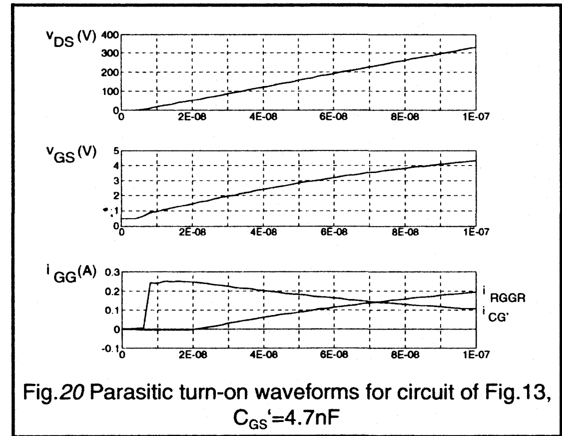


Fig.*20* Parasitic turn-on waveforms for circuit of Fig.13, C_{GS}'=4.7nF

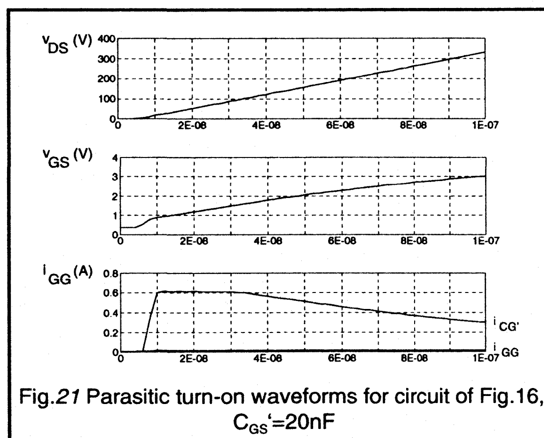


Fig.*21* Parasitic turn-on waveforms for circuit of Fig.16, C_{GS}'=20nF

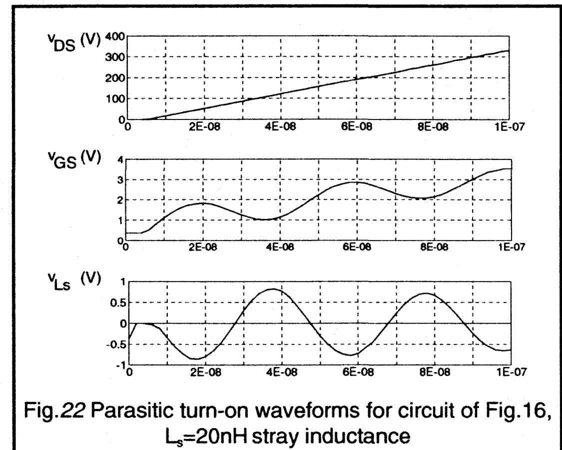


Fig.*22* Parasitic turn-on waveforms for circuit of Fig.16, L_s=20nH stray inductance

Figure 19 shows the response of the circuit of Figure 13 with C_{GS}'=10nF. Here the gate-source voltage is held down during the parasitic turn-on period and so the MOSFET stays off. If the value of C_{GS}' is reduced to 4.7nF then the results given in Fig.20 show that v_{GS} reaches 3V after 55ns thus reducing immunity to parasitic turn-on.

Figures 21 and 22 show the conditions for parallel connected MOSFETs using the circuit of Fig.16. In Fig.21, for R_{GG1}=47Ω, R_{GG}'=10Ω and C_{GS}'=20nF, the bottom trace in the figure shows that a potential parasitic turn-on condition is avoided and v_{GS} is held below its threshold value. The bottom trace in Fig.21 shows most of the parasitic turn-on current is taken by C_{GS}'. Figure 22 shows the effect of stray inductance between the gate drive circuit and the PowerMOS device. The circuit of Fig.16 has been modified by the addition of 20nH of stray inductance between the gate node and the dv/dt clamping network. During switching of the top device with dv/dt=3.5V/ns the stray inductance develops over 0.6V due to coupling via C_{GD}. Clearly this could significantly affect the performance of the drive during normal turn-on, and increase the prospect of the bottom MOSFET being subject to parasitic turn-on problems.

These results show that immunity to parasitic turn-on can be greatly improved by alternative gate circuit design. The SPICE modelled circuits show the worst case conditions of constant dv_{DS}/dt and show that v_{GS} can be held below its threshold voltage using the circuits shown in the previous section. Experimental measurements have confirmed these results in a prototype 20kHz ACMC system.

Device losses in ACMC inverters

It is important to be able to calculate the losses which occur in the switching devices in order to ensure that device operating temperatures remain within safe limits. Cooling arrangements for the MOSFETs or FREDFETs in an ACMC system will depend on maximum allowable operating temperatures, ambient temperature and operating conditions for the system. The components of loss can be examined in more detail:

MOSFET Conduction losses

When a MOSFET or FREDFET is on and carrying load current from drain to source then the conduction 'i^2R' loss can be calculated. It is important to note that the device current is not the same as the output current, as demonstrated by the waveforms of Fig.23. The figure shows a sinusoidal motor load current waveform and the top and bottom MOSFET currents. The envelopes of the MOSFET currents are half sinusoids; however the actual device currents are interrupted by the instants when the load current flows through the freewheel diodes. For the purposes of calculating MOSFET conduction losses it is acceptable to neglect the 'gaps' which occur when the freewheel diodes are conducting for the following reasons:

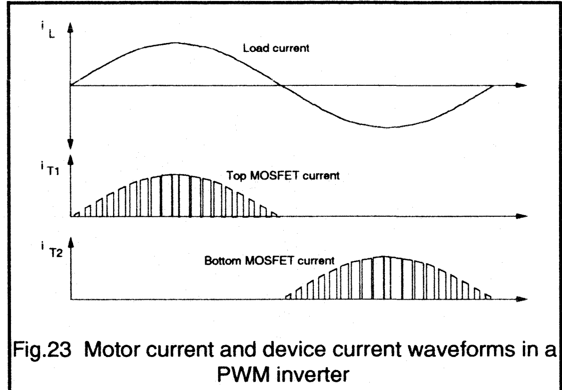


Fig.23 Motor current and device current waveforms in a PWM inverter

-When the motor load current is near its maximum value the switching duty cycle is also near its maximum and so the proportion of time when the diode conducts is quite small and can be neglected.
-When the motor load current is near zero then the switching duty cycle is low but the MOSFET is only conducting small amounts of current. As the MOSFET current is low then the contribution to total conduction loss is small.

Thus if the MOSFET is assumed to be conducting load current for the whole half-period then the conduction losses can be calculated using the current envelope of Fig.23. These losses will be overestimated but the discrepancy will be small. The conduction losses can be given by:

$$P_{M(ON)} = I_T^2.R_{DS(ON)}(T_j) \quad (13)$$

where I_T is the rms value of the half sinusoid MOSFET current envelope.

and: $$R_{DS(ON)}(T_j) = R_{DS(ON)}(25^{\circ}C).e^{k(Tj-25)} \quad (14)$$

where k=0.007 for a 500V MOSFET, and k=0.006 for a 500V FREDFET.

I_T is related to the rms motor current, I_L, by:

$$I_T = \frac{I_{max}}{2} = \frac{I_L}{\sqrt{2}} \quad (15)$$

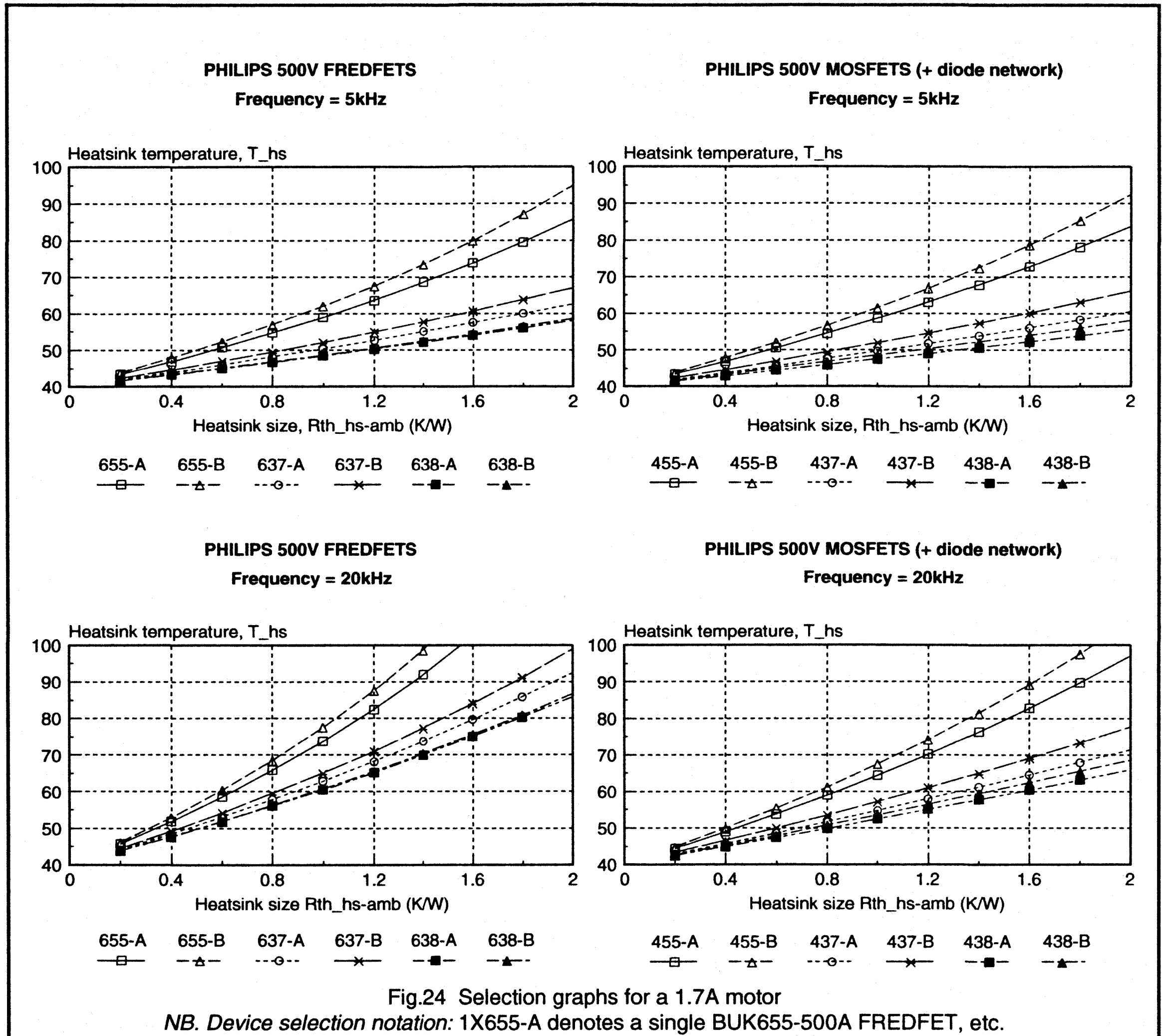


Fig.24 Selection graphs for a 1.7A motor
NB. Device selection notation: 1X655-A denotes a single BUK655-500A FREDFET, etc.

Additionally in a MOSFET inverter the series blocking Schottky diode (D3 of Fig.8) has conduction losses. The current in this diode is the main MOSFET current and so its loss is approximated by:

$$P_{Sch(ON)} = V_f(T_j).I_T \qquad (16)$$

Diode conduction losses

In a MOSFET inverter the freewheel diode losses occur in a discrete device (D2 of Fig.8) although this device is often mounted on the same heatsink as the main switching device. In a FREDFET circuit the diode losses occur in the main device package. The freewheeling diode carries the 'gaps' of current shown in Fig.23 during the periods when its complimentary MOSFET is off. Following the argument used above the diode conduction loss is small and can be neglected. Using this simplification we have effectively transferred the diode conduction loss and included it in the figure for MOSFET conduction loss.

MOSFET switching losses

During the half-cycle of MOSFET conduction the load current switched at each instant is different (Fig.23). The amount of current switched will also depend on the reverse recovery of the bridge leg diodes and hence on the

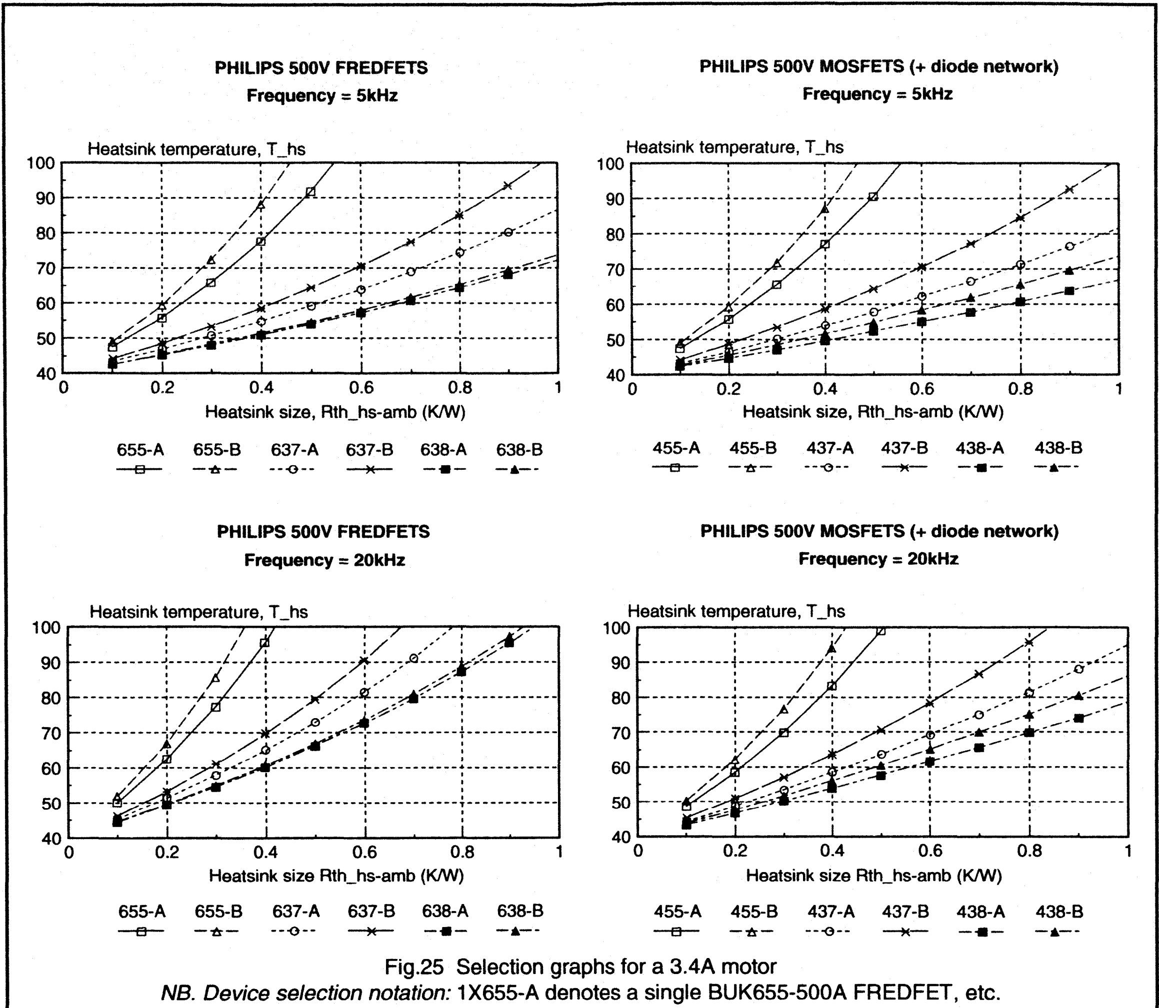


Fig.25 Selection graphs for a 3.4A motor
NB. Device selection notation: 1X655-A denotes a single BUK655-500A FREDFET, etc.

temperature of the devices. The total turn-on loss ($P_{M(SW)}$) will be a summation of the losses at each switching instant:

$$P_{M(SW)} = \sum_{n=0}^{\infty} f(T_j, I_n) \qquad (17)$$

MOSFET turn-off times are usually only limited by dv/dt considerations and hence are as short as possible. The turn-off loss of the MOSFETs or FREDFETs in an inverter is small compared with the turn-on loss and can usually be neglected.

Diode switching losses

Diode turn-off loss ($P_{D(SW)}$) is calculated in a similar manner to the MOSFET turn-on loss. The factors which affect the diode turn-off waveforms have been discussed earlier. Diode turn-on loss is usually small since the diode will not conduct current unless forward biassed. Thus at turn-on the diode is never simultaneously supporting a high voltage and carrying current.

Gate drive losses

Some loss will occur in the gate drive circuit of a PowerMOS device. As the gate drive is only delivering short pulses of current during the switching instants then these losses are negligibly small.

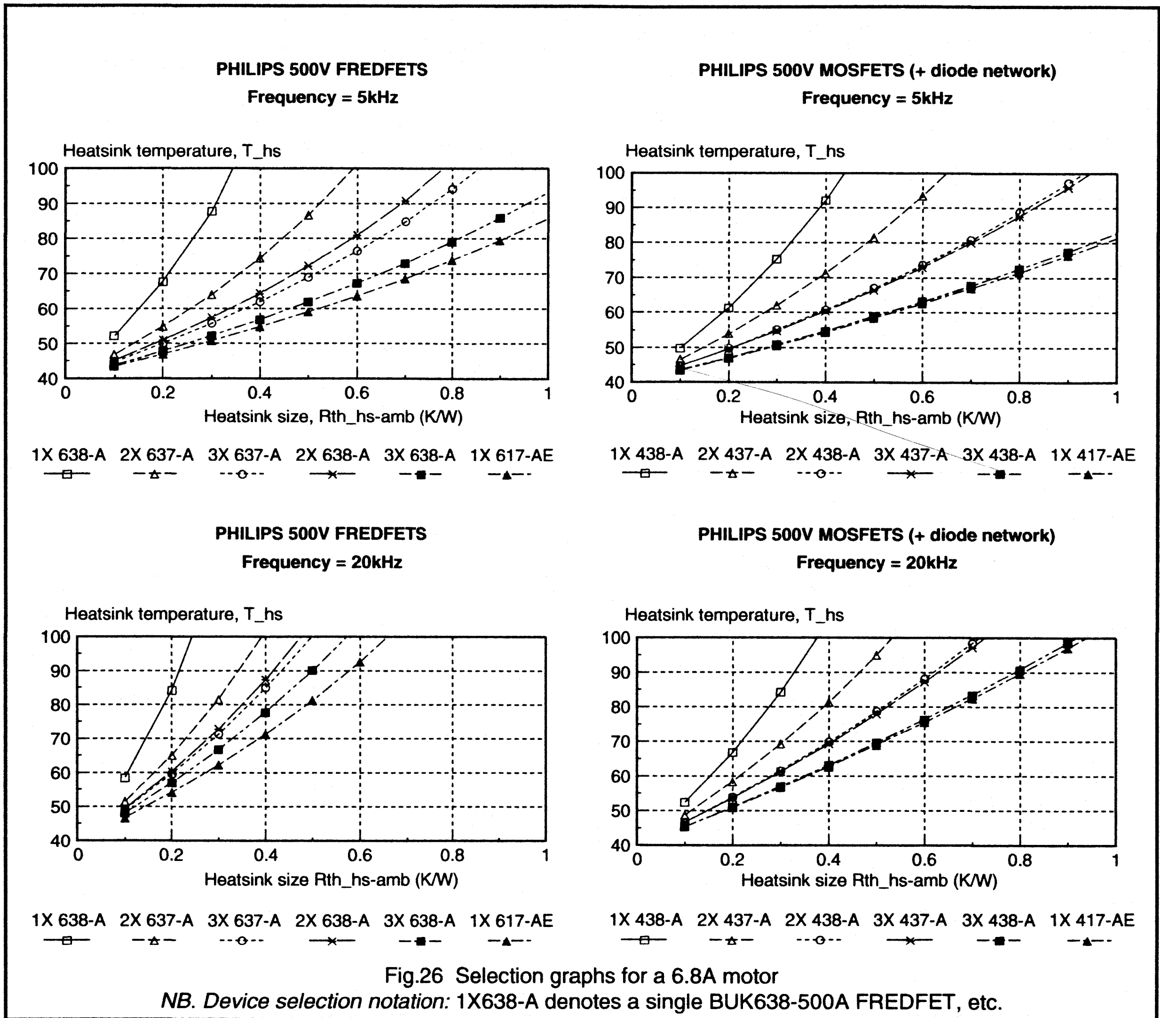


Fig.26 Selection graphs for a 6.8A motor
NB. Device selection notation: 1X638-A denotes a single BUK638-500A FREDFET, etc.

System operating temperatures

In this section the device losses discussed in the previous section are calculated and used to produce a design guide for the correct selection of Philips PowerMOS devices and appropriate heatsink arrangements for ACMC applications. The following factors must be take into account when calculating the total system loss, P_{LOSS}:

- -Device characteristics
- -Switching frequency
- -Operating temperature
- -Load current
- -Number of devices used in parallel.
- -Additional snubber or di/dt limiting networks.

$$P_{LOSS} = P_{M(ON)} + P_{M(SW)} + P_{D(SW)} + P_{Sch(ON)} \quad (18)$$

For the results presented here the device parameters were taken for the Philips range of 500V MOSFETs and FREDFETs. The on-state losses can be calculated from the equations given above. For this analysis the device switching losses were measured experimentally as functions of device temperature and load current. As there are six sets of devices in an ACMC inverter then the total heatsink requirement can be found from:

$$T_{hs} = T_{ahs} + 6.P_{LOSS}.R_{th(hs-ahs)} \quad (19)$$

$$T_j = T_{hs} + P_{LOSS}.R_{th(j-hs)} \quad (20)$$

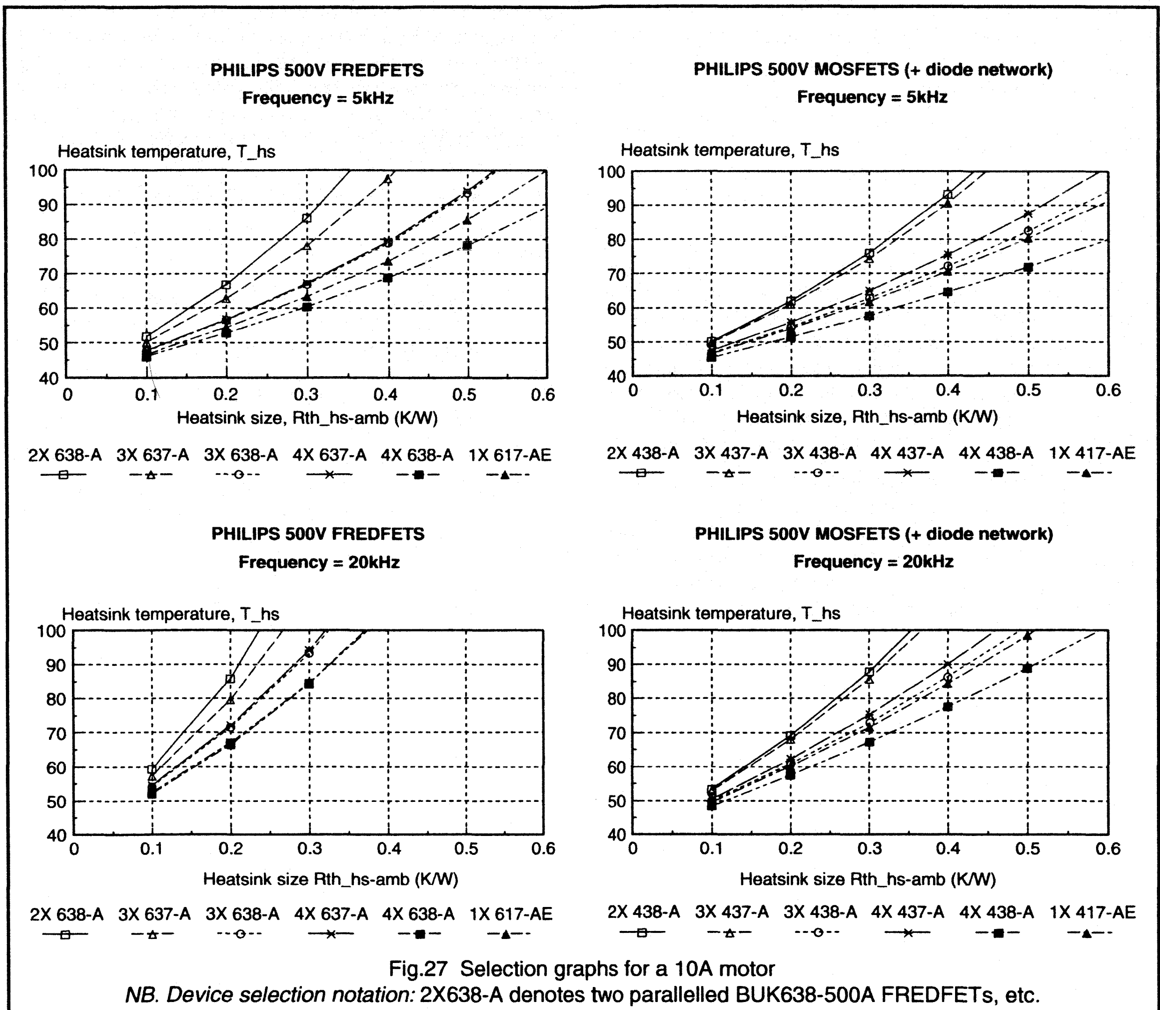


Fig.27 Selection graphs for a 10A motor
NB. Device selection notation: 2X638-A denotes two parallelled BUK638-500A FREDFETs, etc.

Equations 18 to 20 can be used to find the heatsink size ($R_{th(hs-ahs)}$) required for a particular application which will keep the heatsink temperature (T_{hs}) within a required design value. Results are plotted in Figures 24 to 27 for motor currents of I_L = 1.7A, 3.4A, 6.8A and 10.0A. These currents correspond to the ratings of several standard induction motor sizes. The results assume unsnubbed devices, an ambient temperature of T_{ahs}=40˚C, and are plotted for inverter switching frequencies of 5kHz and 20kHz.

Two examples showing how these results may be used are given below:

1) -The first selection graph in Fig.24 shows the possible device selections for 500V FREDFETs in a 5kHz ACMC system where the full load RMS motor current is 1.7A. Using a BUK655-500A FREDFET, T_{hs} can be maintained below 70˚C with a total heatsink requirement of 1.2K/W (if each FREDFET was mounted on a separate heatsink then each device would need a 7.2K/W heatsink). The same heatsinking arrangement will give T_{hs}=50˚C using a BUK638-500A. Alternatively T_{hs} can be maintained below 70˚C using a 2K/W heatsink (12K/W per device) and the BUK637-500B.

2) -In Fig.27 the selection graphs for a 10A system are given. The fourth selection graph is for a 20kHz switching frequency using 500V MOSFETs. Here two BUK438-500A devices connected in parallel for each switch will require a total heatsink size of 0.3K/W if the

heatsink temperature is to remain below 90˚C. The same temperature can be maintained using a 0.5K/W heatsink and a single BUK417-500AE ISOTOP device.

For different motor currents or alternative PWM switching frequencies the appropriate device and heatsink arrangement for a particular application can be found by interpolating the results presented here.

Conclusions

This section has outlined the basic principles and operation of PWM inverters for ACMC applications using Philips PowerMOS devices. MOSFETs and FREDFETs are the most suitable devices for ACMC systems, especially at high switching speeds. This section has been concerned with systems rated up to 2.2kW operating from a single phase supply and has shown that there is a range of Philips PowerMOS devices ideally suited for these systems.

The characteristics and performance of MOSFETs and FREDFETs in inverter circuits and the effect of gate drive design on their switching performance has been discussed. The possibility of parasitic turn-on of MOSFETs in an inverter bridge leg can be avoided by appropriate gate drive circuit design. Experimental and simulated results have shown that good switching performance and immunity to parasitic turn-on can be achieved using the Philips range of PowerMOS devices in ACMC applications . Using the device selection graphs presented here the correct MOSFET or FREDFET for a particular application can be chosen. This guide can be used to select the heatsink size and device according to the required motor current, switching frequency and operating temperature.

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3.1.5 Using fast switching power transistors and Darlingtons in the ISOTOP package

1. Introduction.

High power applications with output powers in excess of, 2kW generally use bridge configurations. Traditional applications for power transistors and darlingtons are switch mode power supplies, ac and dc motor drives, uninterruptable power supplies (UPS) and battery chargers. Recently, electronic welders, high dynamic motor drive converters and induction heating are becoming more important. When defining circuits and components for these high power systems compromises should be made with regards to both technical and cost aspects.

There is a slow but steady trend towards higher frequencies. This is due to the required low noise operation, as in the case of uninterruptable power supplies and ac motor controllers. Size reduction and a large bandwidth also play an important role. As a consequence of this increase in switching frequencies PowerMOS is gaining more and more popularity and is now widely applied in energy conversion systems. Bipolar transistors and darlingtons, which are the subject of this paper, find a place mainly in higher voltage applications and in low frequency higher power systems. New generation bipolar switches, primarily high voltage transistors, are being used for systems above a few hundred of watts. Darlingtons, discrete or composed, are preferred above 1kW. Improvements in semiconductor devices and related technologies have led to an increase in switching frequencies in medium-power systems (1-50kVA) operating from the rectified 380/440V mains.

Not only has the silicon technology improved based on the progress made with PowerMOS devices, but also the development of new packages, in particular the ISOTOP package, have made this increase in frequency possible. The ISOTOP package as shown in Fig.1 has many properties which make it very useful for high frequency high power switching applications. A wide range of diodes, transistors, darlingtons and PowerMOS are available in ISOTOP. The properties of the ISOTOP package have contributed greatly to the improvements in power devices. It enables easier cooling, isolation and wiring of the circuits. The main advantages of the ISOTOP package are:

- One can directly connect it to printed circuits or plates by screws resulting in a reduction in wiring inductances.
- It is a very flat package (12mm height) in order to minimise internal distance between the semiconductor and its external connections. The internal wiring inductances are reduced to c. 5nH.
- Internal insulation is provided: the insulation using built-in alumina provides an optimum compromise between thermal resistance and high insulating voltage (Rthj-mb = 0.5˚C/W; insulating voltage = 2.5kV(rms)).
- The absence of external insulating components (mica, insulating bushes) reduces cost, facilitates assembly and enhances reliability. The low value of the permittivity (dielectric constant) of alumina reduces the parasitic capacitance between heatsink and semiconductor (C=45pF for ISOTOP versus 110pF for a mica insulated T03).
- ISOTOP has a low thermal resistance: R_{thj-mb} = 0.5˚C/W.
- Due to the flat base it is very easy to mount it on a heatsink.

The aim of this paper is to show the feasibility of convertors of several kVA operating from the rectified 380/440V mains, using switching frequencies above 16kHz. Semiconductor technologies and the consequences for the application behaviour are considered as well as base drive techniques and the advantages and disadvantages of the use of snubber networks. This article provides elements which may help to simplify the choice of the components and the related circuit environment.

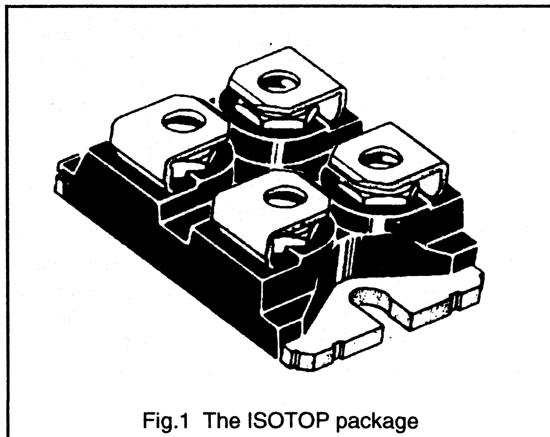


Fig.1 The ISOTOP package

2. The half bridge configuration.

Most high power systems are fed from the three phase mains. which implies input voltages of 380-440V. For high power systems the half bridge configuration (see Fig.2) is the most popular. When using PWM techniques, the current flows through the pair T1/D2 or through T2/D1. Although switching frequencies may be high, the off times of one pair of switches may be very long. Another point to observe is the fact that transistor T1 is not connected to ground and a floating base drive should be made. Operating half bridge circuits directly from the 380/440V mains implies that the minimum blocking voltage capability of the switches must

be 800V. When using bipolar transistors or Darlingtons, two options are possible: one may use snubbers or one may prefer not use them.

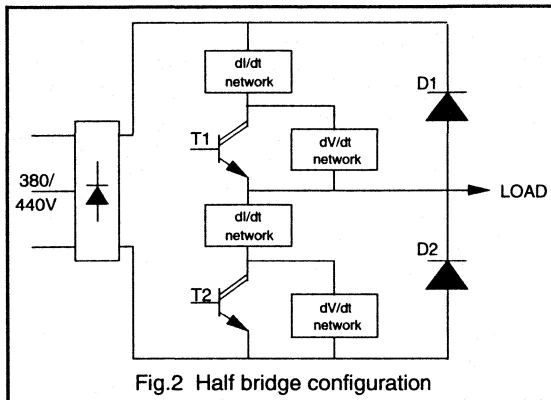


Fig.2 Half bridge configuration

2.1. Choice of switching transistors

Devices whose published RBSOAR permits voltages of 800V or more at the required currents, can operate without a snubber network. Generally, these devices have V_{CEOmax} = 800V. If the devices do not fulfil these RBSOAR requirements, one may choose devices with a V_{CESmax} of 800V (V_{CEOmax} = 400V). One must use snubbers now in order to keep the device inside its safe operating areas. It is important to realise that devices with a higher maximum voltage VCEOmax are worse than lower voltage devices. Not only have higher voltage devices a lower gain, but also switching times are longer and the manufacturer has to invest more silicon area for the same value of I_{Csat}, the useful current. With higher voltages switching will be also be proportionally worse. Figure 3 displays the effects of the value of V_{CEO} on gain and switching parameters.

As a result, transistors with a V_{CEOmax} of 800 V and above are not well suited for 20kHz PWM systems, but when lower voltage transistor are used, higher frequencies become possible. For this reason, the use of 400V V_{CEOmax} transistors and Darlingtons and associated snubbers is advised for ultrasonic medium power converters operating from 380/440V.

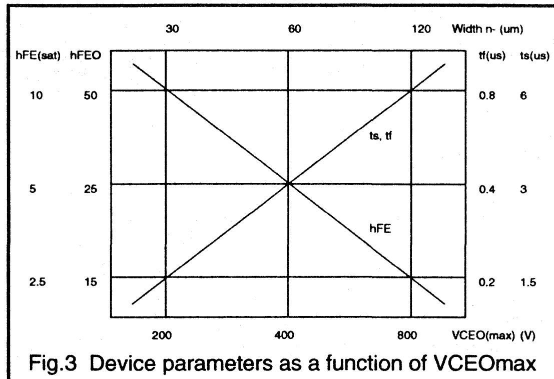


Fig.3 Device parameters as a function of VCEOmax

2.2. Reverse currents in the switches

In bridge circuits, the phenomenon of reverse current through the transistor followed by a high dV/dt gradient is quite well documented. In a bridge leg a non conducting transistor can become forward biased (working in reverse) when its anti-parallel diode is conducting. Then a considerable charge is stored in the transistor. When the other transistor in the half bridge starts conducting again, the stored charge can lead to very high peak currents. This may lead to high switching losses and possibly device destruction. Counter measures are discussed in section 4.

3. Semiconductor technology

3.1. Manufacturing trade-offs

Several trade-offs exist when manufacturing power transistors and Darlingtons. Increasing the maximum voltage V_{CEOmax} by using thicker collector layers will result in a lower current gain and switching times will increase. An increase in current gain by higher efficiency base and emitters, will often result in longer switching times.

3.2. Technological improvements

Recent improvements in the performance of bipolar transistors and Darlingtons have been obtained by using optimised starting material. Also new finer emitter geometries extend the reverse safe operating areas and shorten switching times. The extension of safe operating areas was also made possible by CAD-optimised doping profiles. Fast-switching Darlingtons have also benefited from these technological improvements:

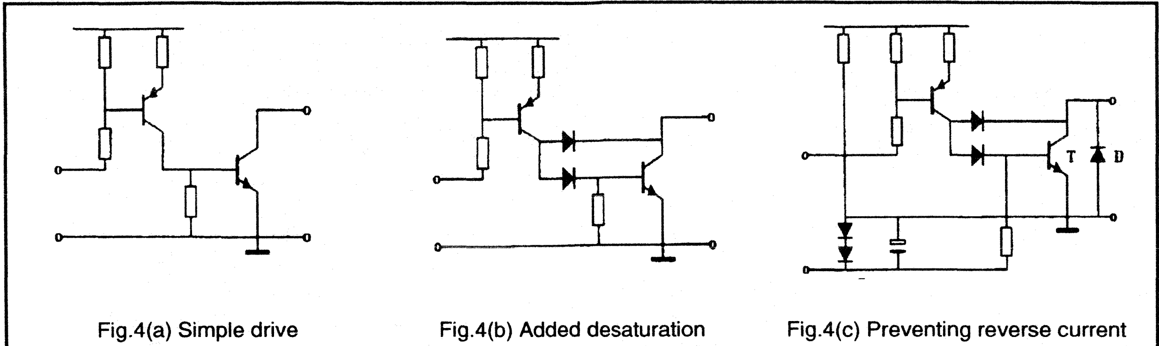


Fig.4(a) Simple drive Fig.4(b) Added desaturation Fig.4(c) Preventing reverse current

- Reduction of the collector-emitter saturation voltage at higher junction temperatures.
- Reduction of base currents required for saturation.
- A higher value for the overcurrent allowed at turn-on:
  Ipeak = 2 . ICsat
- Operation with lossless or dissipative snubbers is possible up to the peak voltage VCESmax and consequently the switchable power is multiplied by 2.
- The parasitic collector-emitter diode of Darlingtons has been replaced by an ultra-fast diode (50 to 60ns) with low reverse recovery current.

4. Base drive concepts

The circuits described in this section are concepts showing the essential elements. The value of the components will normally be optimised for the specific application.

4.1. The base drive

The switching speed of a power transistor depends not only on the power device technology, but also on the base drive. Very simple base drives without a negative auxiliary supply voltage only permit relatively long switching times. When using more complicated base drives or emitter switching or REC (Reverse Emitter Current) configurations, shorter switching times result.

For all semiconductor switches, there is a relationship between the drive circuit, switching losses, safe operation area and maximum switching frequency. Driver circuits may be simplified when the required switching speed is low. If the transistor is subject to a reverse current followed by a fast voltage rise as described in section 2, then this must be taken into account when designing the base drive circuit.

4.2. Low frequency switching.

At low switching frequencies (about 1kHz), power transistors and Darlingtons can operate without negative bias. As an example, the circuit shown in Fig.4a, with a single positive voltage source, may be sufficient. A low value base-emitter resistance is often sufficient to turn off the power transistor or Darlington. For further turn-off time reduction a small inductance (some µH) can be connected in series with the base-emitter resistor. As indicated in Fig.4b one can add a desaturation network, thus preventing severe overdrive, improving the turn-off waveforms.

As described in section 2, a reverse current followed by a high dV/dt gradient may lead to high switching losses or possible device destruction. To prevent this, it is advised to provide a negative voltage across the base-emitter for as long as the transistor is supposed to block, thus preventing the transistor going into reverse conduction. When a floating auxiliary source is used for the supply of the base drive circuit, reverse current problems can be suppressed by simply adding a resistor, two diodes and a capacitor as shown in Fig.4c. The generated negative drive voltage improves the turn-off behaviour and the immunity against high voltage gradients.

4.3. Higher frequency switching

The addition of a transistor providing an active negative base drive, as shown in Fig.5a, enables higher frequency switching. The use of a negative auxiliary supply and a base coil gives the same result but turn-off times will be even further reduced. With the circuit shown in Fig.5b the power transistors or Darlingtons can be used for switching applications far beyond the audio frequency range. The driver circuits illustrated in Fig.5 are well suited for power transistors and Darlingtons. If the output current from such driver circuits must be increased for higher output power applications, amplifier stages for the positive or negative base current can be added (Fig.6).

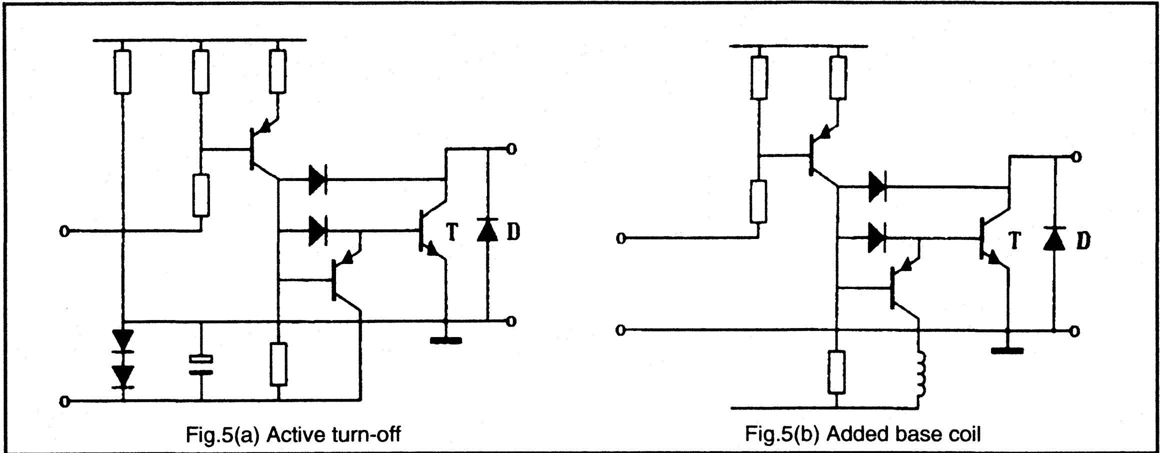


Fig.5(a) Active turn-off

Fig.5(b) Added base coil

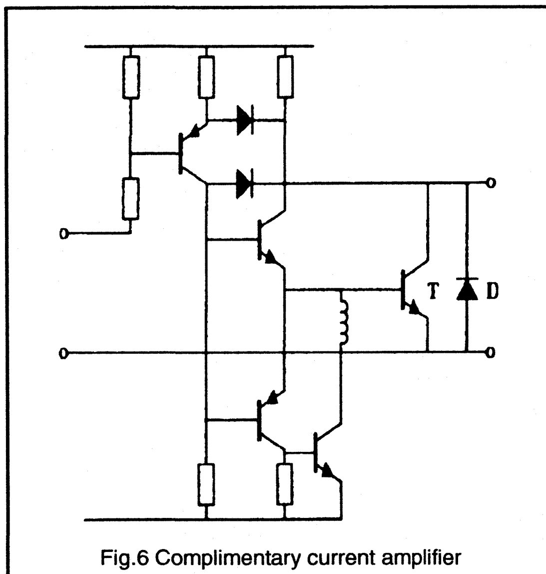


Fig.6 Complimentary current amplifier

Figure 7a shows a base drive concept which yields very short turn-on and turn-off times and requires only one positive supply. The concepts generates its own negative blocking voltage and that without any limitation of the duty cycle. Capacitor C is continuously loaded by the positive source. Transistor T2 is only turned on during the storage time, ts, and fall time, tf, of the driven power transistor. Transistor T2 discharges the capacitor C via the emitter-base junction of the power transistor.

In this drive circuit, capacitor C is charged during both the conduction time, t_{on}, and the off time, t_{off}, minus storage time, t_s. Only during the storage and fall time is energy withdrawn from the capacitor. Its load status is thus independent of the duty cycle. By addition of some extra components, the transistors driven by this circuit can be protected against reverse currents and high dV/dt gradients (Fig.7b).

4.4. Drive circuits in bridge configurations

In bridge circuits, a driver stage with galvanic insulation between input and output is often required for the upper switch. In switch mode power supplies, a driver transformer may be used because the required on- and off-times remain relatively short. As an example, the power required for the base drive can for instance be derived from the collector-emitter circuit (Fig.8). The active part of the driver circuit only has to generate short pulses to trigger status changes of the power switch and has to supply the core demagnetizing current.

When extremely long pulse durations must be handled a floating drive is unavoidable and different base drive concepts must be used . One method (see Fig.9) consists of using differentiated drive signals, to transmit it by means of a small transformer (ferrite core) and regenerate the signal by a bi-stable driver circuit. T1, T2 and the surrounding components form a Schmitt trigger. In this case the active part of the drive circuit must be supplied from a floating auxiliary source. A permanently available negative voltage source allows shorter switching times and lower losses. It leads to an improved design flexibility as it allows the introduction of comparators for overcurrent protection into the driver stage. Such a concept offers the advantage of very short reaction times.

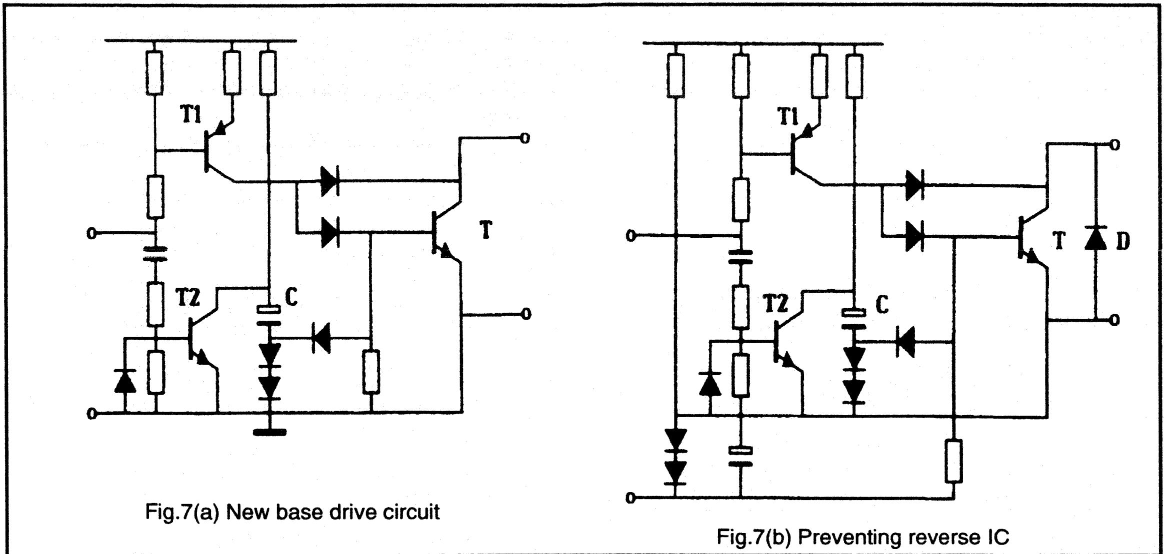


Fig.7(a) New base drive circuit

Fig.7(b) Preventing reverse IC

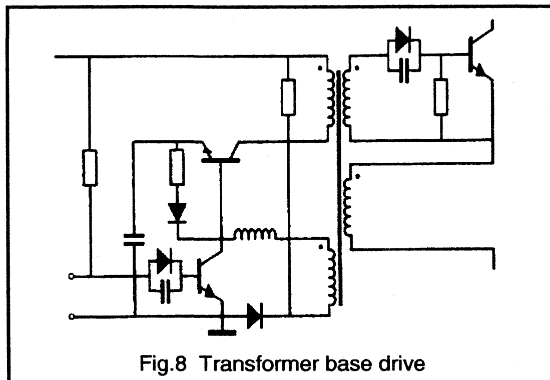


Fig.8 Transformer base drive

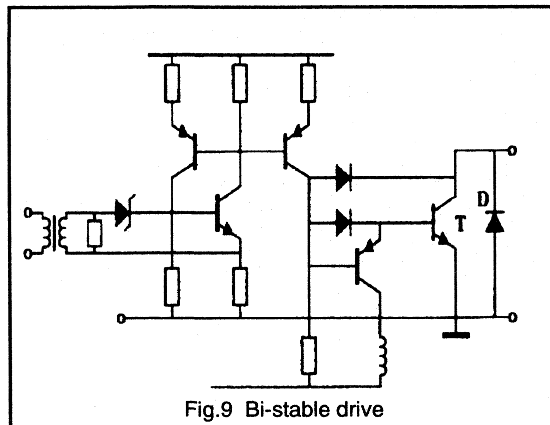


Fig.9 Bi-stable drive

4.5. Drive Circuit for Ultra-Fast Switching

Ultra-fast switching with a collector current fall-time of about 10ns can be obtained with the driver circuit of Fig.10. Thanks to a current source behaviour at turn-on, ultra-fast turn-on is possible (i.e. with a dIC/dt of more than 100A/µs). For ultra-fast turn-off (fall times of 5 to 10ns), a high negative voltage must be applied for about 1µs to the base-emitter junction of the power transistor or Darlington. This can be done with a MOSFET. The MOSFET should conduct for a time that is about the sum of storage- and fall-time of the driven power transistor. The MOSFET can be a low voltage device with a relatively high on resistances (i.e. 50V and 500mΩ).

In this circuit, the average value of the negative base current is not higher than in conventional circuits. The current reaches its high amplitude only for a very short time. Thus the losses in the MOSFET are low and it needs no heatsink. Other components (T5 etc.) prevent the power transistor from being turned on due to parasitic oscillations of the base-emitter voltage.

5. Pros and cons of snubbers.

A snubber network serves to limit the rate of rise of the V_{CE} on a transistor, thereby allowing voltages up to V_{CESmax}. Without a snubber the maximum voltage is roughly half this value. There are high voltage Darlingtons currently available capable of switching 400A under 1200V without snubber networks. When such components are used switching losses must be carefully analysed. Losses

induced in Darlingtons by the reverse recovery current of the freewheel diode and losses due to lead inductances cannot be neglected.

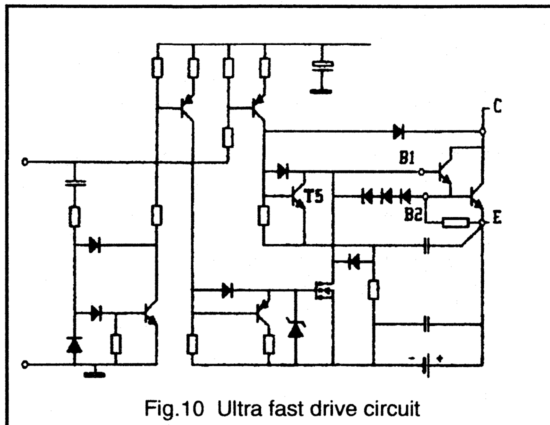


Fig.10 Ultra fast drive circuit

5.1. Advantages of snubbers.

At first glance, snubbers seem to make circuits complicated. However, in electronic power equipment, they may offer notable advantages:

- Turn-off losses in the semiconductor devices are dramatically reduced (see section 5.4), so mounting and cooling are simplified and the switching frequency can be increased.
- The semiconductor components will operate at lower junction temperatures with inherent reliability improvement.
- Snubbers reduce voltage and current gradients, thus reducing the cost of noise suppression and filtering.
- Using low dissipation (or non-dissipative) snubbers improves the overall-efficiency and less heat has to be dissipated. (With converters directly supplied from the 380 V three-phase mains, efficiencies up to 98% have been obtained).
- With non-dissipative snubbers, switching frequencies of over 50kHz are readily accessible. Thus converters with output voltages and currents with particularly low harmonics content and with a high regulation speed can be designed.

5.2. Energy-recovery snubbers

When applying state of the art bipolars, the use of snubbers is, for high-voltage, medium-power converters, the only way to obtain noiseless frequencies (i.e. above 16kHz). Through the use of snubbers, switching energy can be dissipated outside the power switches and, as seen above, lower voltage (therefore fast) Darlingtons can be used. By using energy-recovery snubbers the commutation energy is no longer dissipated but transferred from one non-dissipative element to another and then fed to the mains (Fig 11). In addition to keeping the Darlington load-line inside its safe operating area and to drastically reducing switching losses in power switches, energy-recovery snubbers increase the efficiency of converters.

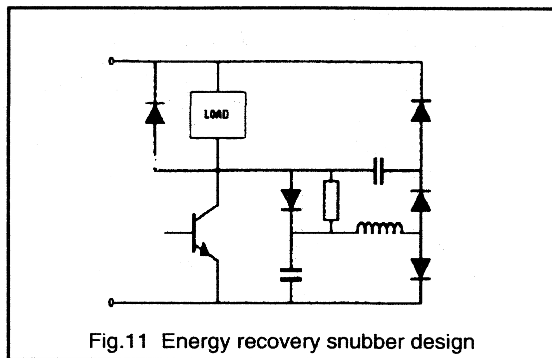


Fig.11 Energy recovery snubber design

5.3. Turn-off losses with and without snubbers.

In good approximation the turn-off losses in a transistor or Darlington can be written as follows:

$$E_{off} = \frac{1}{4} . I_C . t_c^2 . \frac{dV_{CE}}{dt}$$

$$P_{off} = \frac{1}{4} . I_C . t_c^2 . \frac{dV_{CE}}{dt} . f$$

where: I_C = Load current
t_c = Cross-over time at turn-off switching.
dV_{CE}/dt = Rate of rise of the collector current
f = Switching frequency

From the above equations it is obvious that a snubber reduces switching losses. We can compare the application of an 800V V_{CEO} power transistor without a snubber and a 850V V_{CES} transistor with a snubber. Comparing t_c=200ns and dV_{CE}/dt = 8kV/µs with t_c = 100ns and dV_{CE}/dt = 2kV/µs shows that a snubbed 850V V_{CES} device will exhibit 16 times lower turn-off losses than a 800V V_{CEO} device! Apart from this one should also take into account that the lower voltage devices have a gain which is about a factor of 2 higher.

The total losses include also the turn-on and saturation losses and the dissipation caused by the lead inductance. Ignoring saturation and lead inductance losses, the total losses follow approximately from:

$$E_{tot} = E_{off} + V_{cc} . \frac{(I_l + I_{RM})^2}{dI_C/dt}$$

$$P_{tot} = P_{off} + V_{cc} . \frac{(I_l + I_{RM})^2}{dI_C/dt} . f$$

where: I_l = load current
dI_C/dt = rate of rise of the collector current
I_{RM} = freewheel diode reverse recovery current.

Using the above equations one can evaluate the total losses and the resulting junction temperature. It should be checked that the junction temperature does not exceed acceptable values. If the junction is too high, the following measures may lead to a reduction in total losses:

- Reduction of the thermal resistance: this is achieved by using a larger heatsink or the use of a transistor with a package with a lower thermal resistance, or spreading of heat sources (two lower current transistors in parallel instead of one big transistor).
- Reduction of the collector-emitter saturation voltage: use a power transistor or Darlington with a higher nominal collector current I_{Csat} (current derating).
- Lowering the switching frequency: i.e. use of a time discrete control instead of an PWM control.
- Decrease the recovery current I_{RM}: use of a freewheel diode with lower I_{RM}.
- Increase dI_C/dt: Improve the drive circuit to obtain a higher rate of rise of base current, lower the wiring inductance between the driver circuit and the power transistor, use of a power transistor or Darlington with higher nominal collector current ICsat (current derating).
- Reduction of crossover time, tc: use an improved drive circuit or a power transistor with higher nominal collector current ICsat (current derating).
- Use of a turn-on switching aid network: this reduces the turn-on switching losses in the transistor.
- Use of a turn-off switching aid network: this reduces the turn-off switching losses in the transistor.

The decision to use a snubber or not should be taken in accordance with an overall system analyses. Technical and economical factors must be considered: without snubber, a transistor BUV298A can switch a collector current of 32A under 450V, so its switchable power is 14kVA. With a snubber, the same transistor can switch a current of 32A under 1000V, its switchable power attains 32kVA, i.e. twice as much as without snubber. In the second case, cost is transferred from power semiconductors to passive components. It is to be noted that snubbers possibly may already exist in the circuit structure. In an electronic ballast for fluorescent lamps, the capacitor provided to reduce harmonics on the output voltage limits the turn-off stress on the power transistors.

5.4. Summarising snubbers.

For applications where average regulation speed and dynamic performance is satisfactory, circuits with or without snubbers and operating at a relatively low switching frequency will be used. If high regulation performance and/or non audible operation is required it is recommended to use circuits with lossless snubbers. Decision in favour or against snubbers should only be taken following thorough analysis of the equipment specifications. For both circuits optimised bipolar power transistors and Darlingtons as well as ultra-fast recovery rectifiers are available on an industrial basis.

6. Conclusions

From the viewpoint of technical performance, state of the art power transistors and Darlingtons are very well suited for high frequency high power applications. With converters directly supplied from the rectified 380V mains, very high efficiencies (up to 98% have been reported) are achievable when lower voltage transistors are used with lossless snubbers.

New high-efficiency emitter structures have enabled the increase of current gain while reducing conduction and switching losses. The complexity of base drive circuits has been simplified by such improvements. The optimised packages of these components provide better heat dissipation and allow the design of power converters with reduced volume and cost. Modern semiconductor technologies and packages give new possibilities for the realization of high frequency converters. The combination of these new devices with resonant structures is going to be of a great importance in the development of high performance converters such as power supplies, welding equipment, battery charges, induction heating, etc.

3.1.6 A 300V, 40A High Frequency Inverter Pole Using Paralleled FREDFET Modules

1. Introduction

Voltage source inverters which are switched using some form of pulse width modulation are now the standard in low to medium rated AC and brushless DC variable speed drives. At present, because of device limitations the switching (modulation) frequencies used in all but the lowest drive ratings are restricted to a few kHz. There is however a strong technical advantage in using much higher ultrasonic switching frequencies in excess of 20 kHz, the benefits of which include:

i) The low frequency distortion components in the inverter output waveform are negligible. As a result there is no longer a need to derate the electrical machine in the drive as a consequence of harmonic loss.

ii) The supply derived acoustic noise is eliminated.

iii) The DC link filter component values are reduced.

The device best suited for high switching frequencies is the power MOSFET because of its extremely fast switching time and the absence of secondary breakdown. However, being surface conduction devices, high power rated MOSFETs are difficult and expensive to manufacture and at present single MOSFETs are only suitable for inverter ratings of typically 1-2 kVA per pole. Although higher rated power devices such as bipolar transistors and IGBTs can be switched at medium to high frequencies, the switching losses in these circuits are such that frequencies in excess of 20 kHz are at present difficult to achieve.

Switches with high ratings and fast switching times can be constructed by hard paralleling several lower rated power devices. MOSFETs are particularly suitable because the positive temperature coefficient of the channel resistance tends to enforce good steady-state current sharing between parallel devices. However to achieve good dynamic current sharing during switching, considerable care must be taken in the geometric layout of the paralleled devices on the common heatsink. In addition, the device characteristics may need to be closely matched. As a result modules of paralleled MOSFETs are often expensive.

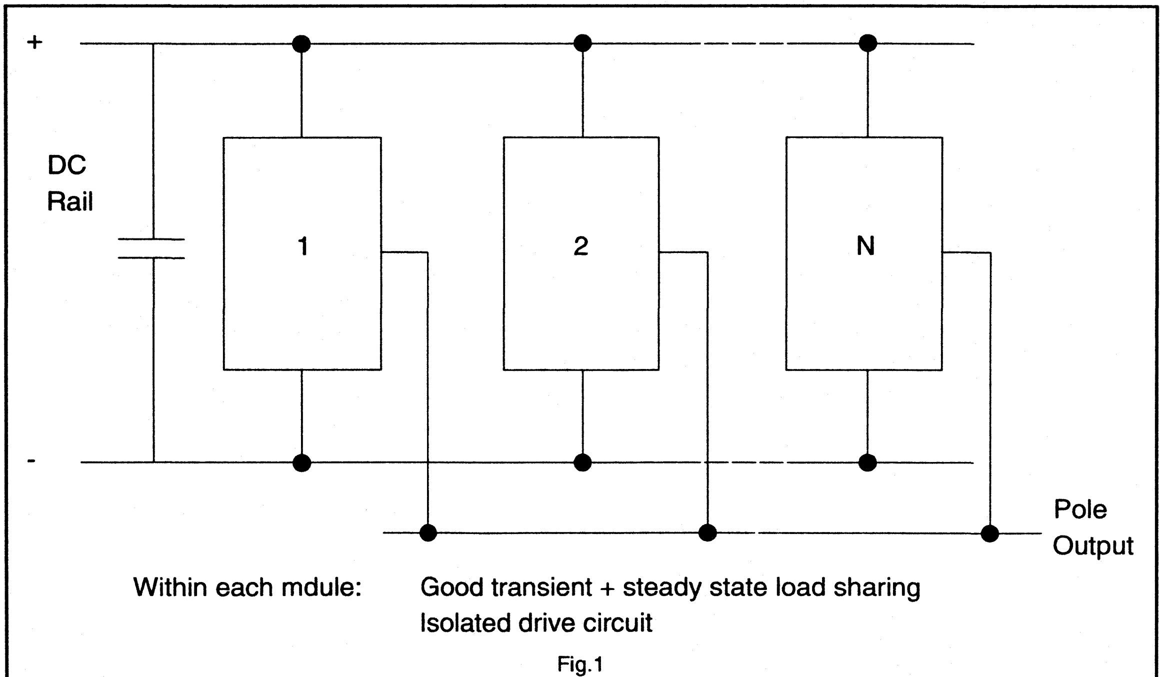


Fig.1

An alternative approach to paralleling is to use small switching aid networks which overcome the constraints of hard paralleling by improving the dynamic load sharing of the individual devices. It is possible to envisage an inverter design where each pole consists of a number of identical pole modules which share a common supply and have outputs connected in parallel, as shown in Fig.1. Each module is designed to operate individually as an inverter pole and contains two power MOSFETs with associated isolated gate drive circuitry. When the modules are connected in parallel their design is such that they will exhibit good transient and steady-state load sharing, the only requirement being that they are mounted on a common heatsink. In this manner any inverter volt-amp rating can be accommodated by paralleling a sufficient number of pole modules.

2. Pole module

The power circuit diagram of an individual pole module which is suitable for the second form of paralleling is shown in Fig.2. The design makes use of the integral body diode of the main switching devices and for this purpose the fast recovery characteristics of FREDFETs are particularly suitable. Two snubber circuits and a centre tapped inductance are included in the circuit. These small switching aid networks perform a number of functions in the circuit:

Fig.2

i) They act to improve the dynamic current sharing between the pole modules when connected in parallel.
ii) They ensure safe operation of the MOSFET integral body diode. The central inductance controls the peak reverse current of the diode and the snubber network prevents secondary breakdown of the MOSFET parasitic internal transistor as the integral body diode recovers.
iii) They reduce the switching losses within the main power devices and thus allows maximum use of the available rating.

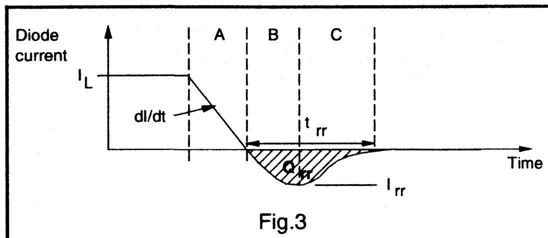


Fig.3

The operation of the circuit is typical of this form of inverter pole. The commutation of the integral body diode will be discussed in detail since it is from this section of the operation that the optimal component values of the switching aid network are determined. The value of the inductor L is chosen to give a minimum energy loss in the circuit and the snubber network is designed to ensure safe recovery of the integral diode at this condition. For example consider the case when there is an inductive load current I_L flowing out of the pole via the integral body diode of the lower MOSFET just prior to the switching of the upper MOSFET. With reference to Fig.3, the subsequent operation is described by the following regions:

Region A: Upper MOSFET is switched on. The current in the lower integral body diode falls at a rate (dI/dt) equal to the DC link voltage V_{DD} divided by the total inductance L of the centre tapped inductance.

Region B: The diode current becomes negative and continues to increase until the junction stored charge has been removed, at which stage the diode recovers corresponding to a peak reverse current I_{RR}.

Region C: The voltage across the lower device increases at a rate (dV/dt) determined by the capacitance C_s of the lower snubber network. The current in the upper MOSFET and the inductor continues to increase and reaches a peak when the voltage across the lower device has risen to the DC link value. At this point the diode D_c becomes forward biased and the stored energy in the inductor begins to discharge through the series resistance R_c.

The energy E_1 gained by the switching aid networks over the above interval is given by:

$$E_1 = \frac{1}{2} I_{RR}^2 L + \frac{1}{2} C_s V_{DD}^2 \qquad (1)$$

and is ultimately dissipated in the network resistors R_s, R_c. For a given forward current, the peak reverse current I_{RR} of the diode will increase with increasing dI/dt and can be approximately represented by a constant stored charge, (Q_{RR}) model, where:

$$I_{RR} = \sqrt{2\left(\frac{dI}{dt}\right) Q_{RR}} \qquad (2)$$

Although in practice I_{RR} will tend to increase at a slightly faster rate than that given by equation (2).

Since in the inverter pole circuit

$$\frac{dI}{dt} = \frac{V_{DD}}{L} \qquad (3)$$

$$I_{RR} = \sqrt{\frac{2 V_{DD} Q_{RR}}{L}} \qquad (4)$$

Inspection of equations (1) and (4) shows that the energy loss E_1 remains approximately constant as L is varied.

During the subsequent operation of the inverter pole when the upper MOSFET is turned off and the load current I_L returns to the integral body diode of the lower device, an energy loss E_2 occurs in the inductor and the upper snubber equal to:

$$E_2 = \frac{1}{2} I_L^2 L + \frac{1}{2} C_s V_{DD}^2 \qquad (5)$$

This loss can be seen to reduce with L. However as L is reduced both I_{RR} and the peak current in the upper MOSFET will increase and result in higher switching loss in the diode and higher conduction loss in the channel resistance of the upper device.

The value of L which gives minimum energy loss in the pole occurs when there is an optimal balance between the effects described above. Typical measured dependencies of the total energy loss on the peak reverse diode current as L is varied are shown in Fig.4. The characteristics of a similarly rated conventional MOSFET and a fast recovery FREDFET are compared in the figure. In both cases the minimum energy loss occurs at the value of L which gives a reverse recovery current approximately equal to the design load current. However the loss in the FREDFET circuit is considerably lower than with the conventional device. The optimal value of L can be found from the manufacturers specified value of stored charge using equation (4), where

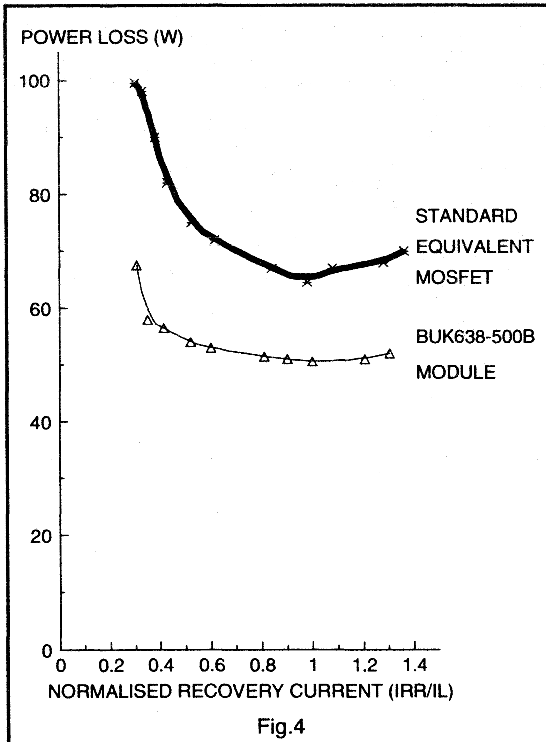


Fig.4

$$L_{opt} = \frac{2V_{DD}Q_{RR}}{I_L^2} \qquad (6)$$

The snubber capacitor value C_s is chosen to limit the dV/dt across the integral body diode as it recovers. Experience has shown that a value of 1V/nS will ensure safe operation, hence:

$$C = (I_L)\,\text{nF} \qquad (7)$$

The resistive component of the switching aid networks are chosen in the usual manner.

3. Parallel operation of pole modules

The principle behind the 'soft' paralleling adopted here is to simply connect the outputs of the required number of modules together and feed them with a common DC link and control signals. The transient load sharing between the parallel modules will be influenced by the tolerances in the individual inductor and snubber capacitor values and any variations in the switching instances of the power devices, the latter being as a result of differences in device characteristics and tolerances in the gate drive circuitry. These effects were investigated using the SPICE circuit simulation package. The SPICE representation of the modules is shown in Fig.5, in which the upper MOSFET channel is modelled by an ideal switch with a series resistance R_{DS}. The full SPICE diode model is used for the lower MOSFET integral body diode, however ideal diode representations are sufficient for the devices in the switching aid networks. The load is assumed to act as a constant current sink over the switching interval.

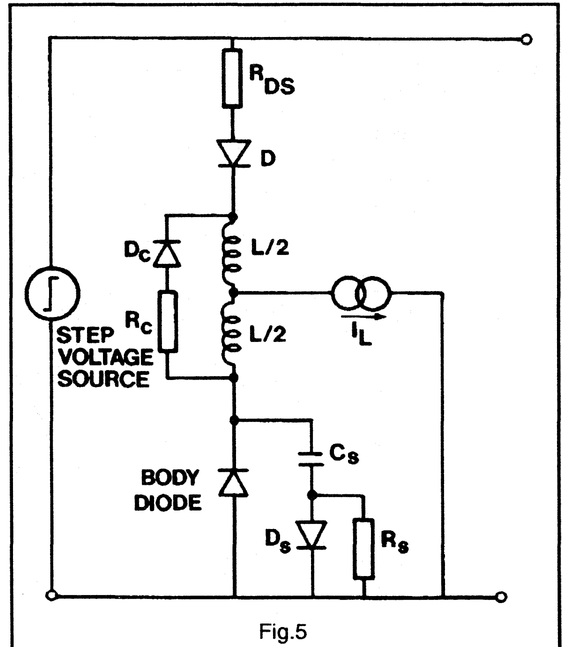


Fig.5

From the SPICE simulation an estimate of the peak transient current imbalance between the MOSFETs of the two modules was obtained for various differences in the inductors, capacitors and device turn-on times. It was found that the transient current sharing was most sensitive to unequal device switching times. An example of the results obtained from a simulation of two paralleled modules using BUK638-500B FREDFETs are shown in Fig.6. With good gate drive design the difference between device switching times is unlikely to exceed 50nS resulting in a peak transient current mismatch of less than 10%. The load sharing would improve if the value of inductor is increased but this has to be traded off against the increase in switching loss. The effect of the tolerance of the inductor values on the load sharing is given for the same module in Fig.7, where it can be seen that a reasonable tolerance of 10% results in only a 7% imbalance in the currents. The load sharing was found to be relatively insensitive to tolerances in the snubber capacitor values.

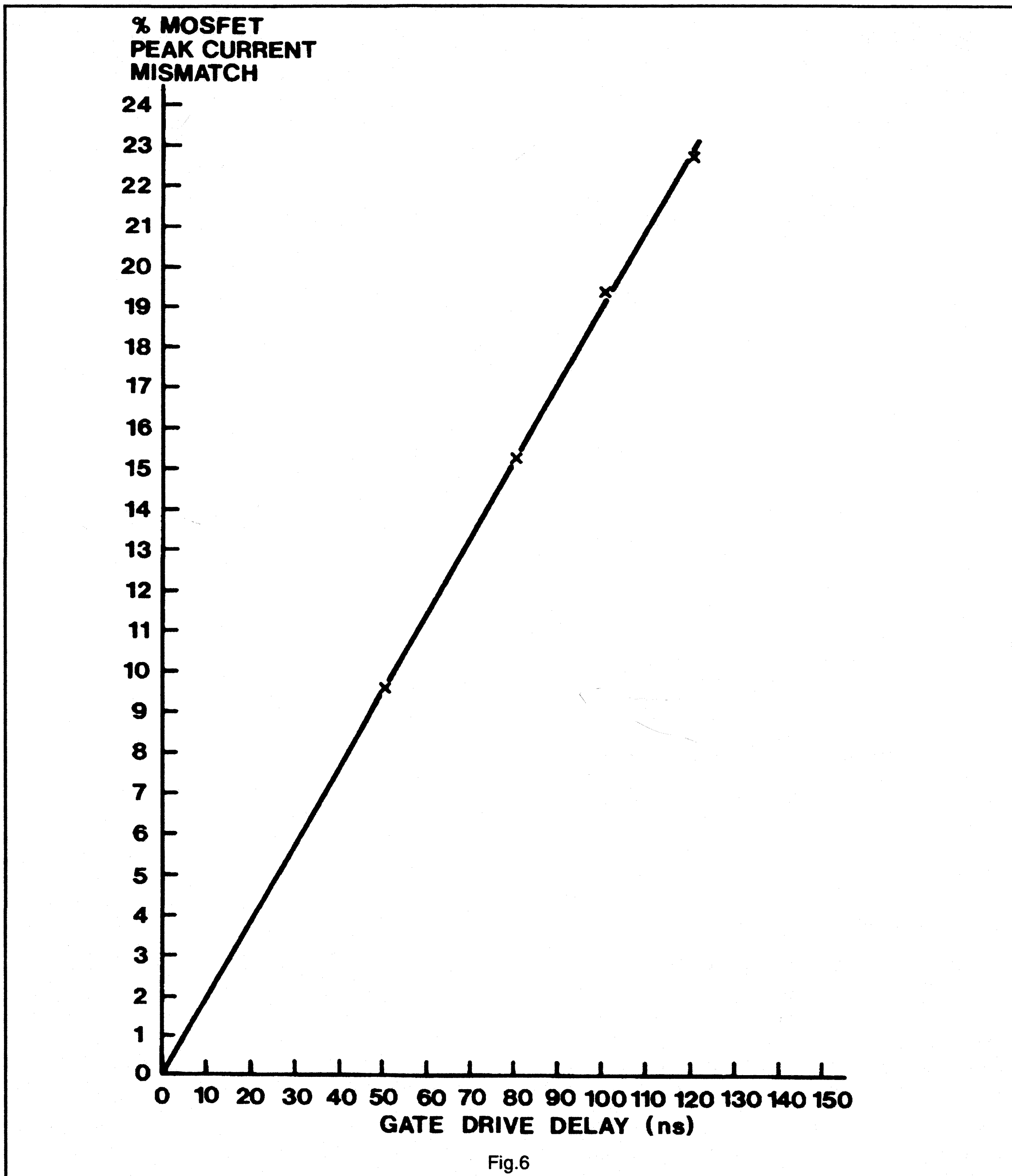


Fig.6

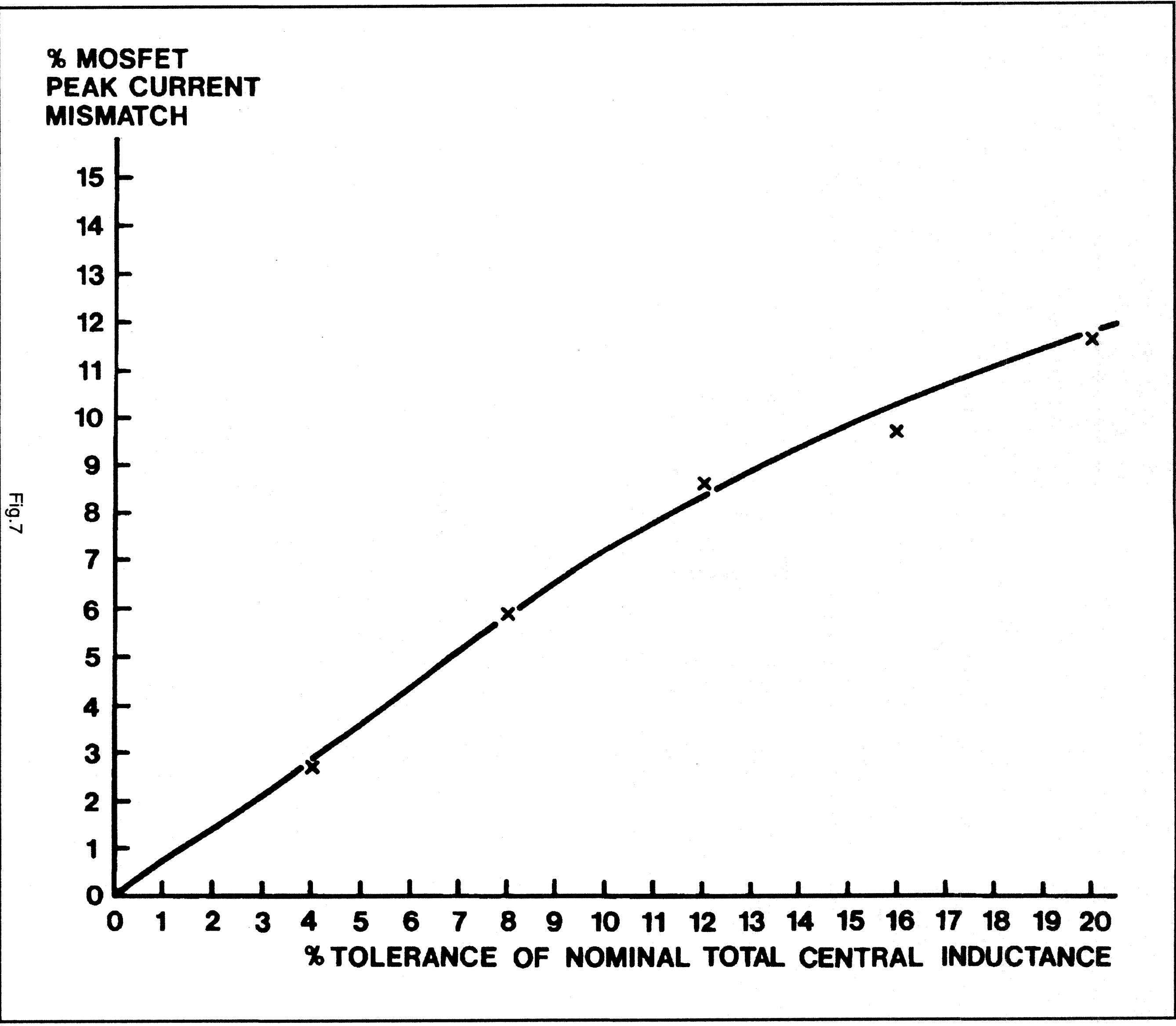


Fig.7

4. A 300V, 10A pole module design using BUK638-500B FREDFETs

The circuit diagram of a 300V, 10A pole module based on BUK638-500B FREDFETs is given in Fig.8. The inductor value was chosen using the criteria discussed in Section 2.

The conventional R-C snubber network has been replaced by the active circuit shown in Fig.9 and involves the use of a second, low rated BUK455-500B MOSFET which is made to act as a capacitance by invoking the 'Miller' effect. The active snubber is more efficient at low load currents because it tends to maintain a constant (dV/dt) regardless of the load, and thus the snubber loss is proportional to the current, as opposed to the conventional circuit in which the loss remains constant. In addition the active circuit is compact and lends itself more readily to a hybrid assembly. The major component costs are the secondary MOSFET and a low voltage power diode and compare favourably with those of the conventional high voltage capacitor and high voltage diode.

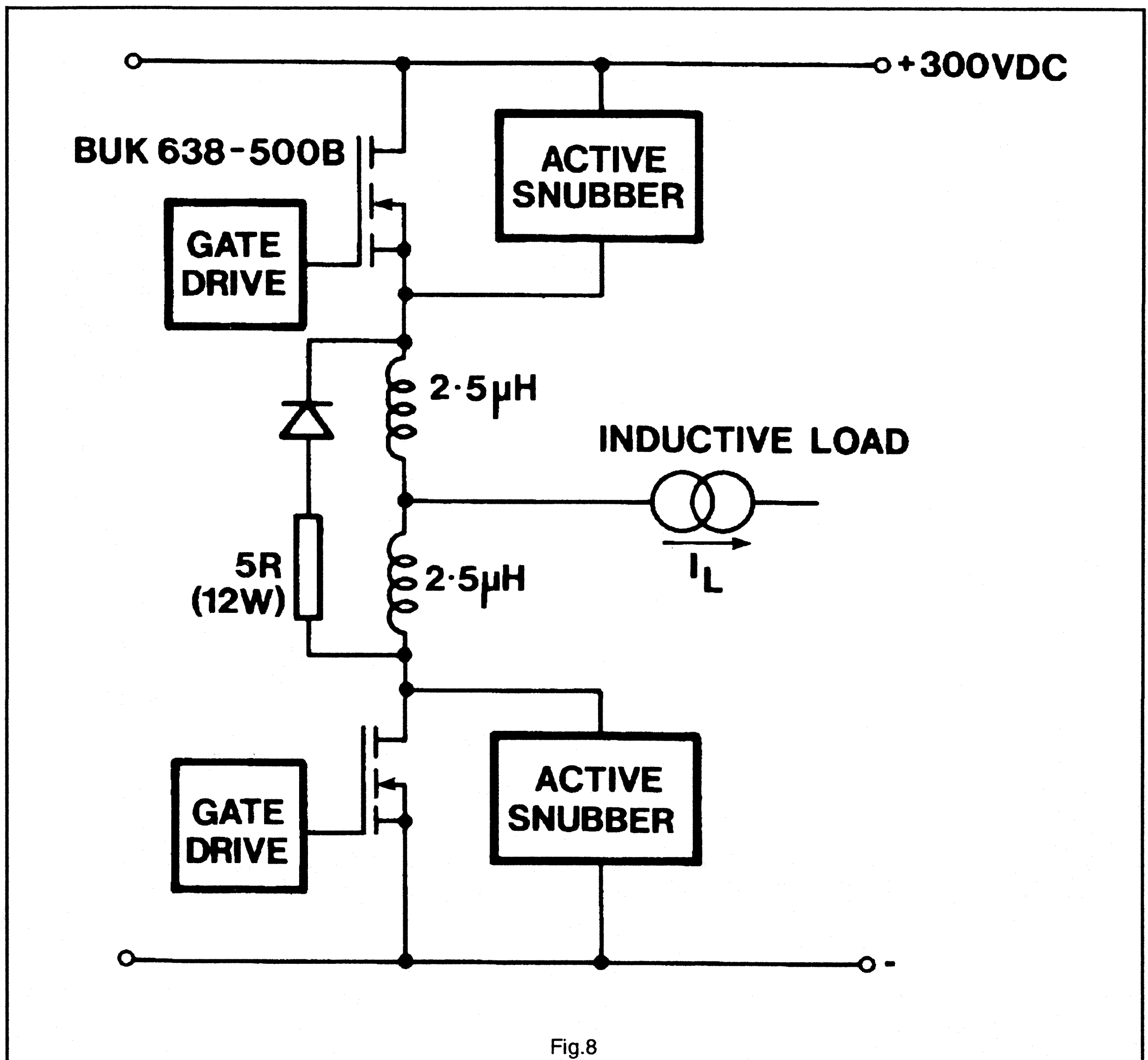


Fig.8

The gate drive circuits are given in Fig.10 and are based upon the pulse transformer configuration described in chapter 1.2.3. A PNP transistor has been added between the gate and source to reduce the drive off-state impedance, to improve the switching and prevent any Miller effect in the main device.

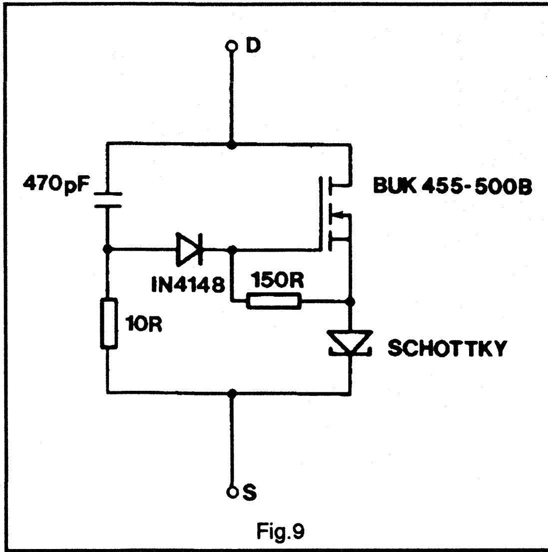


Fig.9

5. FREDFET module performance

The typical voltage and current waveforms of the upper and lower switching devices are shown in Figures 11 and 12 for the case of a single pole module sourcing the rated current of 10 Amps from a 300V DC link. Fig.12 illustrates how the use of the series inductor and active snubber gives a controlled recovery of the fast integral body diode of the FREDFET.

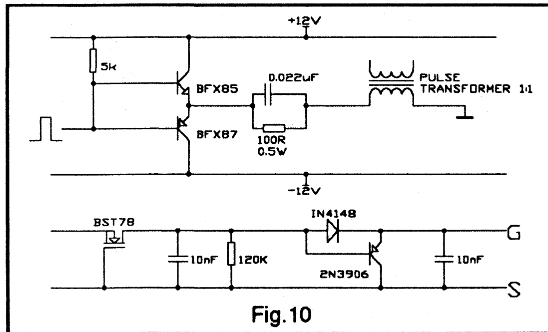
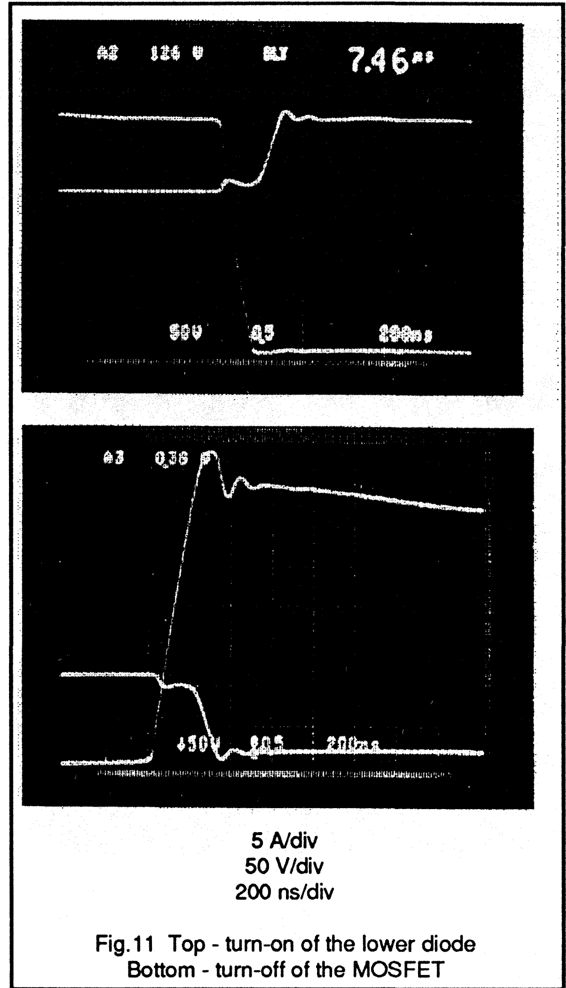


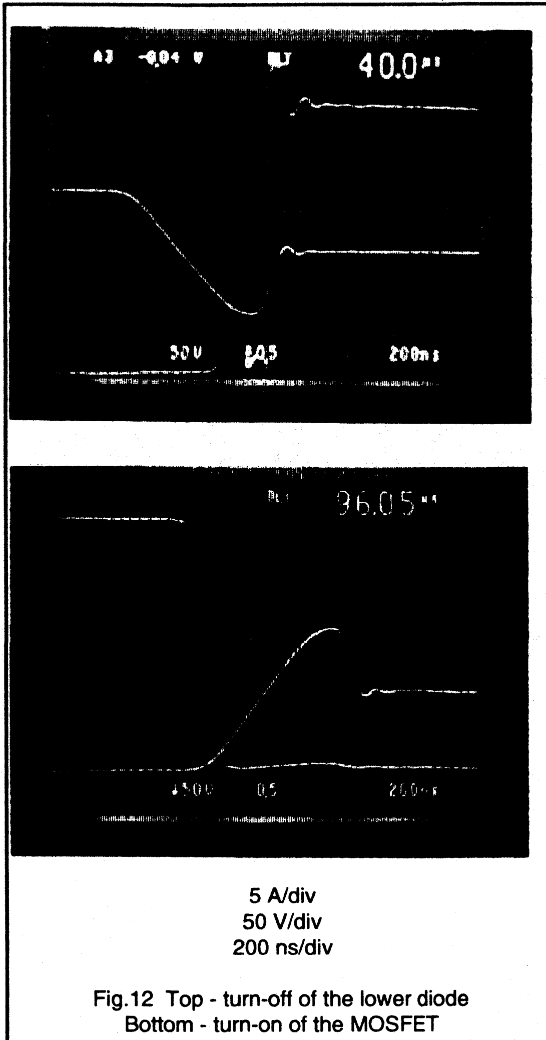
Fig.10



5 A/div
50 V/div
200 ns/div

Fig.11 Top - turn-on of the lower diode
Bottom - turn-off of the MOSFET

The losses of an individual module switched at 20 kHz are plotted in Fig.13 as a function of output current. They mainly stem from conduction loss, the switching loss representing only a third of the maximum loss. Because the switching loss occurs mainly in the aid networks the main FREDFETs can be used at close to their full rating. Similarly operation at higher frequencies will not result in a substantial reduction in efficiency, for example at 40 kHz, 10A operation the losses are 95W.



5 A/div
50 V/div
200 ns/div

Fig.12 Top - turn-off of the lower diode
Bottom - turn-on of the MOSFET

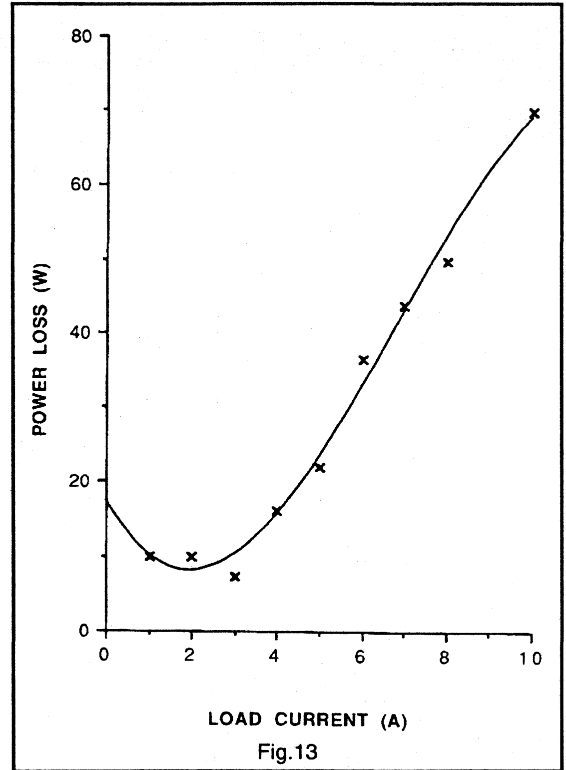
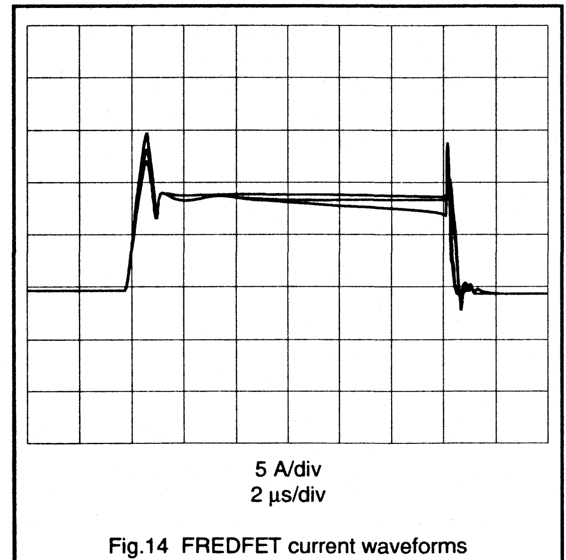


Fig.13



5 A/div
2 µs/div

Fig.14 FREDFET current waveforms

Four modules were connected in parallel and mounted on a common heatsink. The modules operated successfully at 300V with total loads in excess of 40A, four times their individual rating. The common heatsink, which had a thermal resistance to ambient of 0.33˚C/W was sufficient to achieve the full 40A, 300V continuous rating of the parallel units at 20 kHz. The current waveforms of the upper FREDFETs in each module are overlaid in Fig.14, where it can be seen that the load sharing is very even, particularly after the initial switching transients.

6. Conclusion

Parallel, separate MOSFET pole modules provide a method of designing medium rated inverter poles, which can be switched efficiently at frequencies in excess of 20 kHz. The approach is flexible since a single pole module design can be used to achieve a range of inverter volt-amp ratings by paralleling a sufficient number of units.

Through the use of small switching aid networks it is possible to obtain excellent transient and steady-state current sharing between the paralleled modules. The current sharing remains good even if there are substantial variations in component tolerances and the power device switching times. The switching aid networks also reduce the switching losses in the main devices and allows them to be used to their full rating.

The presented design of a 300V, 10A module based on BUK638-500B, FREDFETs has a full load loss of only 70W. Four of these modules connected in parallel and mounted on a 0.33˚C/W heatsink gave an inverter pole with a 300V, 40A continuous rating when switched at 20 kHz. Excellent current sharing between these modules was observed and as a result there would seem to be no technical reasons why further modules could not be paralleled to achieve even higher ratings.

DC Motor Control

3.2.1 Chopper circuits for DC motor control

DC motor drives are used for many speed and position control systems where their excellent performance, ease of control and high efficiency are desirable characteristics. DC motor speed control can be achieved using switch mode DC-DC chopper circuits. For both mains-fed and battery supplied systems, power MOSFETs and FREDFETs are the ideal switching devices for the converter stage. The Philips range of PowerMOS devices includes devices suitable for most DC-DC converters for motor control applications. Additionally, due to the ease with which MOSFETs and FREDFETs can be parallelled, Philips PowerMOS devices can easily be used in chopper circuits for both low power and high power DC motor drives for vehicle, industrial or domestic applications.

Introduction to DC motor drives

In a DC motor, the static field flux is established using either permanent magnets or a stator field winding. The armature winding, on the rotor of a dc machine, carries the main motor current. The armature winding is a series of coils, each connected to segments of a commutator. In order that the motor develops constant torque as the rotor moves, successive armature coils must be connected to the external dc circuit. This is achieved using a pair of stationary brushes held in contact with the commutator.

The motor torque is produced by the interaction of the field flux and the armature current and is given by:

$$T_e \propto I_a \qquad (1)$$

The back emf developed across the armature conductors increases with the motor speed:

$$E_a \propto \omega_m \qquad (2)$$

Permanent magnet DC motors are limited in terms of power capability and control capability. For field wound DC motors the field current controls the flux and hence the motor torque and speed constants. The field winding can be connected in series with the armature winding, in shunt with it, or can be separately excited. For the separately excited dc motor, shown in Fig.1 the field flux is controlled and the motor can be made to operate in two distinct modes: constant torque operation up to the rated speed of the motor, and then constant power operation above rated speed, as shown in Fig.2. The steady state operation of the motor is described by:

$$V_a = E_a + R_a . I_a \qquad (3)$$

For normal motor operation E_a and I_a are positive and the motor is operating in its 'first quadrant'. The motor is said to be operating in its second quadrant, that is braking or regenerating, by reducing V_a below E_a such that I_a is negative. These two quadrants are shown in Fig.3a). If the polarity of the applied voltage is reversed then motoring and regenerating operation can occur with the direction of rotation reversed. Thus by controlling the armature voltage and current polarities, full four-quadrant operation, as shown in Fig.3b), can be achieved.

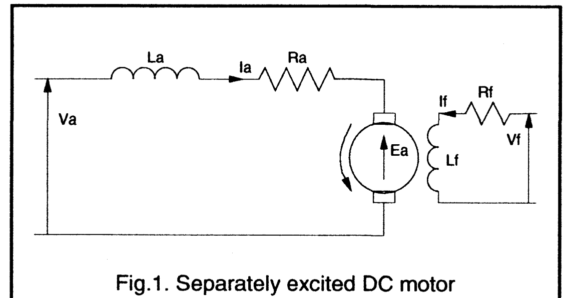


Fig.1. Separately excited DC motor

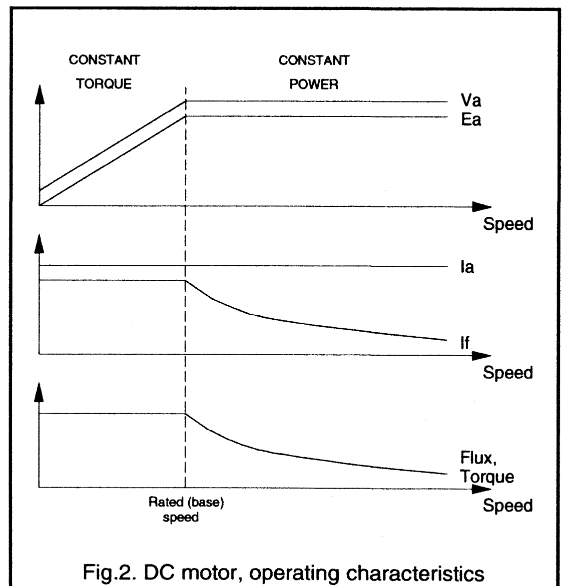


Fig.2. DC motor, operating characteristics

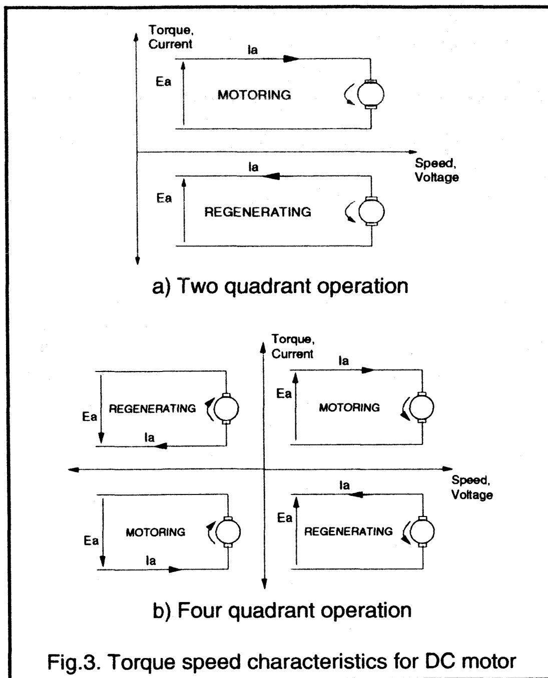


Fig.3. Torque speed characteristics for DC motor

Converter topologies for DC motor drives

Single quadrant (step down) converter

For single quadrant operation the chopper circuit of Fig.4 can be used. The average voltage applied to the motor, and hence its speed, is controlled by varying the duty cycle of the switch, S. Fig.5 shows the switching waveforms for the circuit. During the on time, t_{on}, the supply voltage, V_{dc}, is applied to the motor and the armature current starts to increase. Neglecting the on-state resistance of the switch and the armature winding resistance the voltage across the armature inductance is V_{dc}-E_a and so the rate of rise of armature current is given by:

$$\frac{dI_a}{dt} = \frac{V_{dc} - E_a}{L_a} \qquad (4)$$

When the switch turns off the energy stored in the armature inductance must be dissipated. The polarity of the voltage across L_a reverses, the diode D becomes forward biased and the armature current continues to flow. Assuming that the motor speed remains constant and neglecting the forward voltage drop of the freewheeling diode the inductor voltage is equal to -E_a. The rate of fall of armature current is given by:

$$\frac{dI_a}{dt} = -\frac{E_a}{L_a} \qquad (5)$$

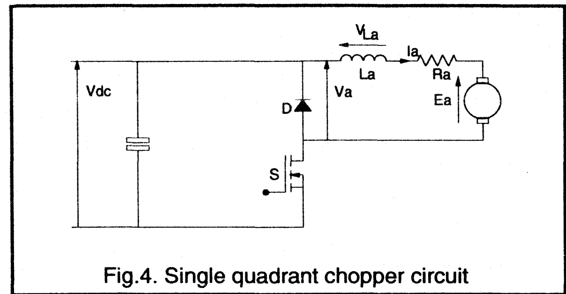


Fig.4. Single quadrant chopper circuit

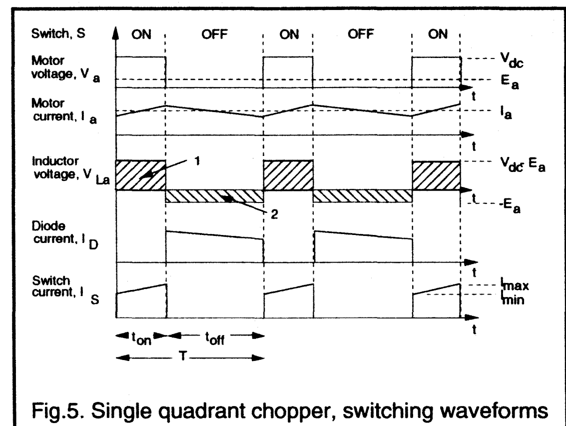


Fig.5. Single quadrant chopper, switching waveforms

If this switching sequence is repeated at some frequency, then the motor voltage can be controlled by altering the relative duration of the on period and off period. Variation of the duty cycle of the switch (t_{on}/T) to control the motor voltage is referred to as Pulse Width Modulation (PWM) control. As the average voltage across the inductor over a period must be zero then:

$$\int_0^T v_L . dt = \int_0^{t_{on}} v_L . dt + \int_{t_{on}}^T v_L . dt = 0 \qquad (6)$$

The integral of inductor voltage for the interval t_{on} corresponds to the shaded area 1 in Fig.5, whilst the integral of inductor voltage for the t_{off} interval corresponds to the shaded area 2 in the Figure. These two areas must be equal and so from equations 4 to 6 or Fig.5 the transfer function of the controller is given by:

$$V_a = \frac{t_{on}}{T} . V_{dc} \qquad (7)$$

Two quadrant, half-bridge converter

Figure 6 shows a half bridge circuit for two quadrant dc drive. For motoring operation S1 and D2 operate as described above for the single quadrant controller. The freewheel diode D2 may be the internal diode of a MOSFET or FREDFET, or a discrete device. For regenerative operation the DC motor acts as the active power source and the power flow is from right to left in Fig.6. The regenerating current is controlled by varying the duty cycle of S2. When S2 is on, the negative armature current increases through the switch and the armature inductance. When S2 is turned off D1 becomes forward biased and the current regenerates into the supply. The relevant circuit waveforms are shown in Fig.7, showing the equal areas of the inductor volt-seconds over each period of the switching cycle. During regeneration the transfer function of the converter is given by:

$$V_a = \left(1 - \frac{t_{on}}{T}\right) . V_{dc} \qquad (8)$$

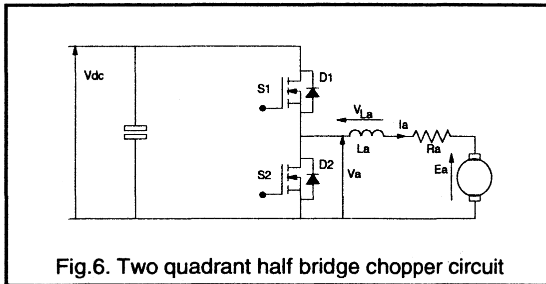


Fig.6. Two quadrant half bridge chopper circuit

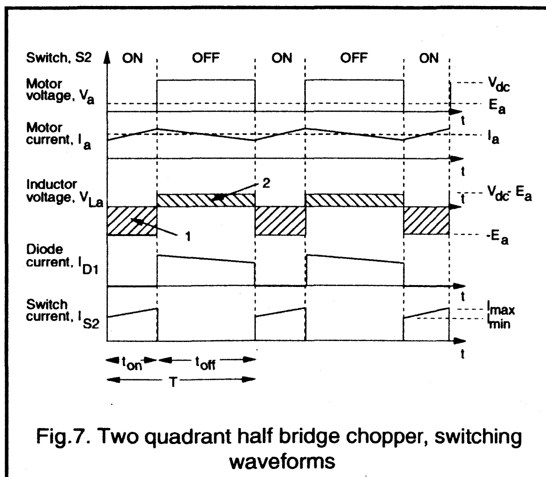


Fig.7. Two quadrant half bridge chopper, switching waveforms

Four quadrant, full-bridge converter

If motoring and regenerating operation are required with both directions of rotation then the full bridge converter of Fig.8 is required. Using this configuration allows the polarity of the applied voltage to be reversed, thus reversing the direction of rotation of the motor. Thus in a full bridge converter the motor current and voltage can be controlled independently. The motor voltage Va is given by:

$$V_a = V_{12} - V_{34} \qquad (9)$$

where V_{12} is controlled by switching S1 and S2 as described above, and V_{34} by switching S3 and S4. The usual operating mode for a full bridge converter is to group the switching devices so that S1 and S3 are always on simultaneously and that S2 and S4 are on simultaneously. This type of control is then referred to as bipolar control.

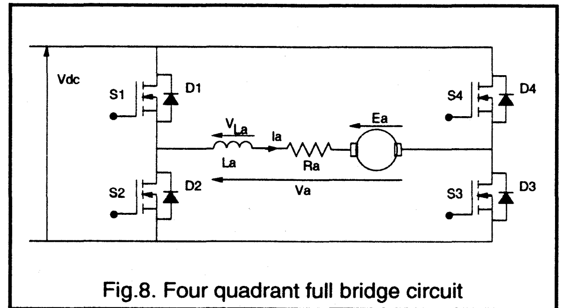


Fig.8. Four quadrant full bridge circuit

MOSFETs and FREDFETs in bridge circuits

In a bridge circuit, conduction transfers between the switching devices and freewheeling diodes as the load current is controlled (eg. switch S2 and diode D1 in Fig.4). Associated with the transfer of conduction between the freewheel diodes and the switching devices is the reverse recovery of the diode as each conducting MOSFET returns to its on-state. Reverse recovery current flows due to the removal of stored charge from a diode PN junction following conduction. Fig.9 shows the device current paths in a half bridge circuit when conduction is transferred from the top diode to the bottom MOSFET.

The switching waveforms are shown in Fig.10 where the diode reverse recovery current is I_{rr} and the time taken for the reverse recovery currents to be cleared is t_{rr}. The amount of stored charge removed from the body of the diode is represented by the area Q_{rr}. The reverse recovery current flows through the MOSFET which is being turned on in addition to the load current and thus causes additional turn-on losses. The amount of stored charge increases with increasing temperature for a given diode. Both the

magnitude of the reverse recovery current and its duration must be reduced in order to reduce the switching losses of the system.

This effect is important because inherent in the structure of a power MOSFET there is a diode between the source and drain of the device which can act as a freewheeling diode when forward biased. For most DC motor control applications the reverse recovery characteristics of the MOSFET intrinsic diode are acceptable and do not compromise the switching performance of the half bridge circuit. However, the characteristics of a MOSFET intrinsic diode are not optimised for minimum reverse recovery and so, especially in high frequency systems, the FREDFET is more suitable for use in half bridge circuits.

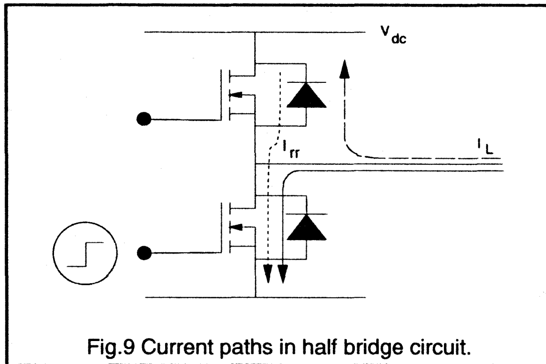


Fig.9 Current paths in half bridge circuit.

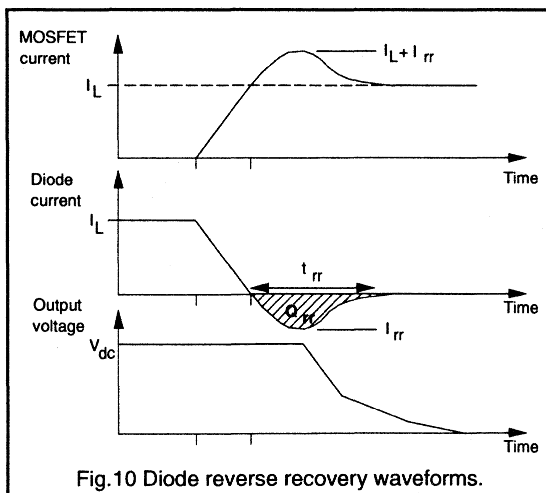


Fig.10 Diode reverse recovery waveforms.

The FREDFET is essentially a MOSFET with a very fast built-in diode where the reverse recovery properties of a FREDFET diode are similar to those of a discrete fast recovery epitaxial diode (FRED). This gives improved switching performance in high frequency applications.

Considerations for converter driven DC motors

Device current rating

The power electronic converter must be matched to the requirements of the motor and the load. DC motor drives can be used to provide torques in excess of the maximum continuous rated torque of the motor for short intervals of time. This is due to the long thermal time constants of the motor. The peak torque requirement of the motor will determine its peak current demand, and hence the peak current requirement for the power switches. The current rating of a PowerMOS device is limited by the maximum junction temperature of the device, which should not be exceeded even for short periods of time due to the short thermal time constant of the devices. The devices must therefore be rated for this peak current condition of the drive. Operation at maximum current usually occurs during acceleration and deceleration periods necessary to meet the performance requirements of DC servo systems.

Device voltage rating

The voltage rating of the power switches will be determined by the power supply DC link voltage and the motor emfs, including those which occur when the motor is operating in its constant power region at above rated speed but below rated torque.

Motor performance

It can be seen from the waveforms of Figures 5 and 7 that the armature current supplied to the motor by the switching converter is not constant. The presence of ripple current in addition to the normal DC current affects the performance of the motor in the following ways:

Torque pulsations. Ripple in the motor current waveform will cause a corresponding ripple in the motor output torque waveform. These torque pulsations may give rise to speed fluctuations unless they are damped out by the inertia of the mechanical system. The torque pulsations occur at high frequencies where they may lead to noise and vibration in the motor laminations and mechanical system.

Losses. Winding losses in a DC motor are proportional to i_{RMS}^2, whereas the torque developed by the motor is proportional to i_{DC}. Ripple in the motor current will increase the RMS current and thus give rise to additional losses and reduce the system efficiency.

Overcurrents. If the ripple current is large then the peak device current will be significantly higher than the design DC value. The devices must then be rated for this higher current. Current ripple will also increase the current which must be handled by the motor brushes possibly increasing arcing at the brush contacts.

The amount of current ripple depends primarily upon the switching frequency and amount of motor inductance (See equations 4 and 5). Increasing L_a and f_s will both reduce the amount of current ripple. The motor inductance is fixed by the motor selection but can be increased by the addition of a discrete component. Increasing the switching frequency of the system will reduce the amount of current ripple but will increase the switching losses in the power devices.

Using PowerMOS devices in DC drives

For many applications the motor control system is operated at switching speeds in the range 1kHz to 20kHz. PowerMOS devices are ideally suited for this type of converter giving the following advantages:

Switching performance

Unlike bipolar devices the MOSFET is a majority carrier device and so no minority carriers must be moved in and out of the device as it turns on and off. This gives the fast switching performance of MOSFET devices. However, at higher switching speeds the switching losses of the system become important and must be considered in addition to the device on-state losses. The device conduction loss depends on the MOSFET on-state resistance, RDS(ON), which increases with the temperature of the device. Switching times are essentially independent of device temperature. PowerMOS devices have good overload capability and Safe Operating ARea (SOAR) which makes them easy to us in a chopper circuit, although the need for snubber circuits will depend on the system operating and performance requirements.

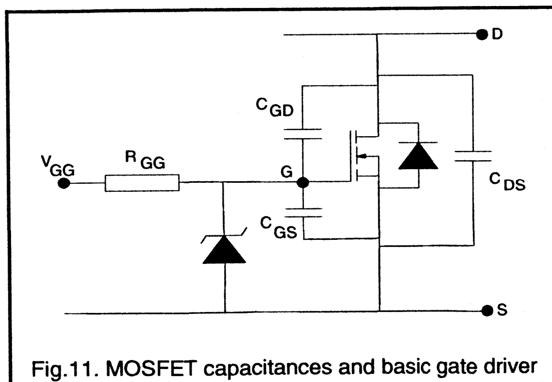


Fig.11. MOSFET capacitances and basic gate driver

Ease of use

PowerMOS devices are essentially voltage driven switches and so the gate drive circuits required to switch the devices are usually relatively simple low power circuits. It is only during switching instants that the gate drive is that required provide current in order to charge and discharge the device capacitances (shown in Fig.11) and thus switch the device. In order to switch the device quickly the gate driver must be able to rapidly sink and source currents of up to 1A. For the simplest gate drive circuit the MOSFET can be switched using a resistive drive and some gate-source overvoltage protection, as shown in Fig.11. Alternative MOSFET gate drive circuits are discussed more fully elsewhere in this handbook.

Parallelling of PowerMOS devices

It is usually straightforward to operate PowerMOS devices in parallel to achieve higher system currents than can be achieved using single devices. The problems of parallelling PowerMOS are much less than those which occur when using bipolar devices. MOSFETs and FREDFETs have a positive temperature coefficient of $R_{DS(ON)}$ and so tend to share the total load current equally. Any discrepancy in device or circuit resistance which causes one device to be carrying a higher proportion of the total current will cause the losses in that device to increase. The device carrying the increased current will then heat up, its resistance will increase and so the current carried will be reduced. The total load current will therefore be equally shared out between all the parallelled MOSFETs. Current sharing during dynamic (switching) instants is achieved by ensuring good circuit design and layout.

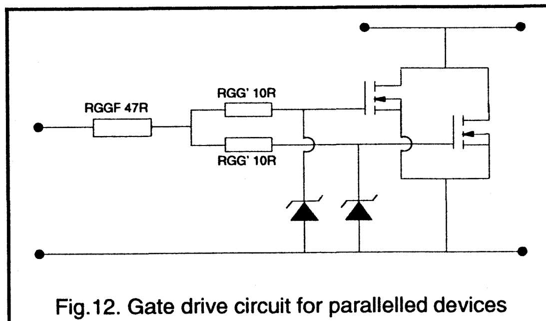


Fig.12. Gate drive circuit for parallelled devices

Moving to a system using parallelled MOSFETs requires only slight modifications to the gate drive circuit. One consideration may be the capability of the drive circuit to provide the currents required at the switching instants. It is recommended that small differential resistors, as shown in Fig.12, are used to damp out any oscillations which may occur between the switching devices and the rest of the circuit.

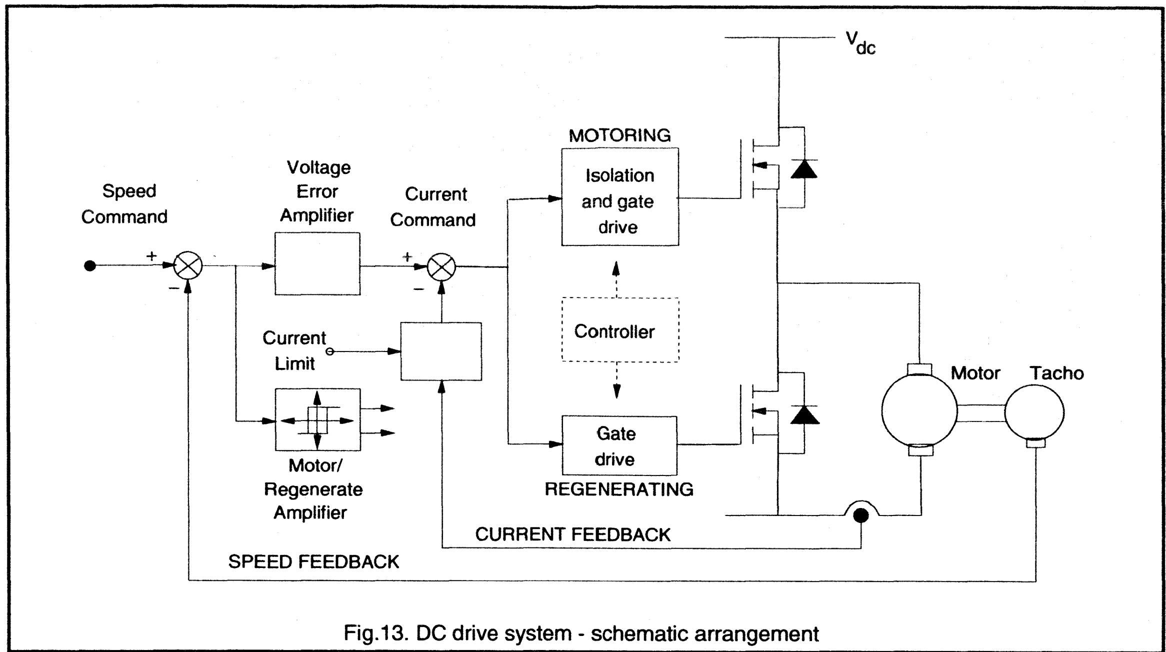


Fig.13. DC drive system - schematic arrangement

Circuit layout considerations

The effects of poor circuit design and layout are to increase RFI and noise and to compromise the performance and speed of the system due to stray inductances. The precautions which must be taken to minimise the amount of stray inductance in the circuit include:

- positioning the gate drive circuits as close as possible to the power MOSFETs.
- reducing circuit board track lengths to a minimum and using twisted pairs for all interconnections.
- for parallelled devices, keeping all connections short and symmetrical.

DC motor control system

Figure 13 shows a schematic arrangement for a two quadrant controller, showing the outer speed control loop and the inner current control loop. The speed feedback signal is derived from a tachogenerator (TGF), although alternatively an approximation to the motor speed can be derived by feeding back a signal proportional to the motor voltage, (AVF). Position feedback can be included for servo applications by using a position encoder on the motor shaft. The speed feedback loop compares the tacho- output voltage with a speed reference signal. The voltage error signal gives the current reference command.

The current command signal is compared with the actual motor current in the inner control loop. This control loop includes a current limit setting which protects the motor and the devices from overcurrents. If the controller demands a large speed change then the current demand is maintained below the maximum level by this current limit setting. Motoring or regenerating operation is detected directly from the polarity of the voltage error signal and used to determine whether it is the top or bottom MOSFET which is controlling the current. The motoring/regenerating logic circuit includes some hysteresis to ensure that control does not oscillate between the motoring and regenerating modes at low motor currents.

There are several possible ways of controlling motor current by controlling the switching sequences to the main PowerMOS devices. In tolerance band control the motor current is compared with the reference signal and an allowed current ripple tolerance. During motoring operation if the actual current is greater than the allowed maximum value of the tolerance band then the output comparator turns off the gate drive to the power MOSFET thus allowing the motor current to fall. The current then freewheels until it reaches the lower limit of the tolerance band, when the comparator turns the MOSFET back on. Using this current control strategy the effective switching frequency is variable, depending on the rate at which the armature current changes, but the peak to peak current ripple in the system is constant. Alternatively the devices can be

switched a constant frequency using a PWM method current control. Here the current error signal is compared with a fixed frequency triangular wave and the comparator output is then used to provide the signal for the main switching devices. When the error signal is greater than the triangular wave then the power device is switched on, when the error signal is less than the triangular carrier then the device is switched off.

Conclusions

DC motor controllers using PowerMOS devices can be used in many speed control and servo applications giving excellent drive performance. The advantages of PowerMOS devices include their simple gate drive requirements, rugged performance and their ease of use in parallel configurations. The intrinsic diode between the drain and source of MOSFETs and FREDFETs can be used as the freewheel diode in half bridge and full bridge circuit configurations giving a cost effective, compact design with the minimum of switching devices. PowerMOS choppers can operate at much higher switching frequencies than thyristor or power transistor controllers, giving reduced current ripple, reduced noise and interference and good dynamic system response. Using higher switching frequencies reduces the need for additional discrete inductances in the motor circuit whilst still achieving low ripple currents in separately excited, permanent magnet and series connected field wound motors.

3.2.2 A switched-mode controller for DC motors

The purpose of this paper is to demonstrate the use of an integrated switched-mode controller generally used for DC power conversion as the primary control and element in a practical Pulse Width Modulated (PWM) DC drive. Basic principles relating to DC motor specifications and drive frequency are presented. The PWM method of switched-mode voltage control is discussed with reference to armature current control, and hence output torque control, of DC motors. A series of circuit configurations are shown to illustrate velocity and position servo applications using a switched mode driver IC. Philips Components produce a wide range of control ICs for Switched Mode Power Supply (SMPS) applications which can also be used as controllers for PWM driven DC motors. This paper demonstrates how one switched-mode controller, the NE5560, can be used to give a velocity and position servo systems using Philips power MOSFETs as the main power switches. Additional application ideas using the NE5560 controller for constant speed and constant torque operation are also presented.

Principles of the PWM DC motor drive

Pulse width modulated drives may be used with a number of DC motor types: wound field or permanent magnet. The discussion here will be particularly concerned with permanent magnet excited DC motors. This does not impose a restriction on the applicability of switched mode control for DC drives since permanent magnet motors are available in a wide range of sizes, ratings and configurations to suit many applications. The design of a pulse width modulated drive is affected by the characteristics of the DC motor load, and this will now be considered in more detail.

The permanent magnet DC motor may be represented by the simplified equivalent circuit shown in Fig.1. L_a represents the total armature inductance, R_a is the equivalent series resistance, and E_a the armature back emf. This induced emf represents that portion of the total input energy which is converted to mechanical output. The magnitude of the armature emf is proportional to motor speed.

Motor inductance, which may vary from tens of μH to mH, will have a significant effect on PWM drive designs. This is due to the fact that average motor current is a function of the electrical time constant of the motor, τ_a, where. $\tau_a = L_a/R_a$. For a PWM waveform with a period T the ratio of pulse width to switching period is denoted by δ. The average pulse current will depend upon the ratio of the current pulse-width, δT, to the motor electrical time constant, τ_a.

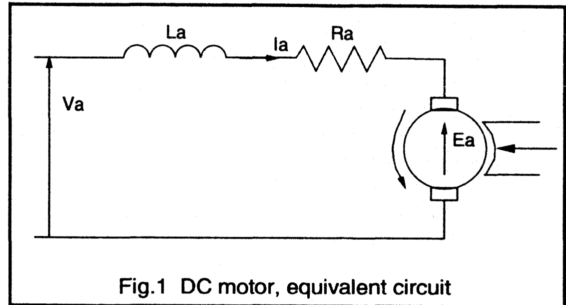


Fig.1 DC motor, equivalent circuit

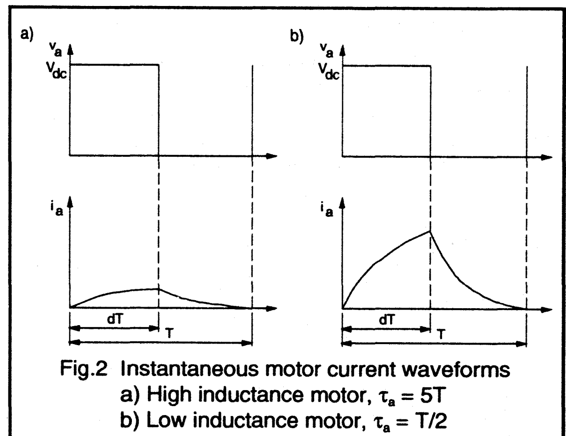


Fig.2 Instantaneous motor current waveforms
a) High inductance motor, τ_a = 5T
b) Low inductance motor, τ_a = T/2

Figure 2 shows the conditions for two different motors and a fixed period PWM waveform. For the case when the motor time constant is much greater than the pulse width, in Fig.2(a) then the current cannot be established in the inductive motor windings during the short duration of the applied pulse. For a low inductance motor and the same pulse width, Fig.2(b), the armature current is easily established. In most instances a motor which has high armature inductance will require a lower PWM drive frequency in order to establish the required current levels, and hence develop the necessary torque. A low inductance motor allows the use of a high switching drive frequency thus resulting in an overall faster system response.

In general, to achieve optimum efficiency in a PWM motor drive at the highest practical frequency, the motor should have an electrical time constant, τ_a, close to the duration of the applied waveform T. (τ_a= kT where k is small). The printed circuit motor is one of the lowest inductance DC

motors available since the armature is etched from a flat disc-like material much like a double-sided printed circuit board: Consequential these low inductance, low inertia motors also exhibit very fast response with quite high torque. Electrical time constants in the order of 100µs allow these motors to be used with switching rates as high as 100kHz, with typical drive circuits being operated at 10kHz.

Thus an appropriate choice of switching frequency and motor inductance ensures a high average motor current during each switching pulse. Motor current control, and hence torque control, is achieved by varying the width of the applied pulsed waveforms. As the base, or carrier, frequency is held constant then the pulse width relays torque control information to the motor. Torque is dependent on average motor current (equation 1) which, in turn, is controlled by duty cycle.

$$T_c = K_T \bar{I}_a \qquad (1)$$

PWM motor control

The PWM method of current control will be considered by examining the conditions at motor start-up for a simple arrangement, shown in Fig.3, where the duty cycle is controlled using the DC control voltage, V_{REF}. At start-up the duty cycle is adjusted to be long enough to give sufficient motor starting torque. At zero rotational velocity (ω=0) the back emf, E_a, is zero and so the full DC voltage appears across the series R_a/L_a impedance. The initial motor current is determined according to the equation:

$$L_a \cdot \frac{di_a}{dt} + R_a \cdot i_a = V_{dc} \qquad (2)$$

If the duty cycle ratio, controlled using V_{REF}, is given by δ, then the duration of the 'ON' pulse is simply given by δT. During this interval the rise of motor current prior to armature rotation is shown by Equation 3.

$$i_a = \frac{V_{dc}}{R_a} \cdot \left(1 - e^{-t/\tau_a}\right) \qquad (3)$$

The current in the motor windings rises exponentially at a rate governed mainly by average supply voltage and motor inductance. If the pulse width is close to the time constant of the motor then the current at the end of the first pulse will reach nearly 60% of its maximum value, $I_{max} = V_{dc}/R_a$. This is shown as I_1 in Fig.4. For the remainder of the PWM cycle switch S1 is off and motor current decays through the diode at a rate dependant upon the external circuit constants and internal motor leakage currents, according to the equation:

$$i_a = I_1 . e^{-(t - \delta T)/\tau_a} \qquad (4)$$

The motor current at the end of the period, T, remains at a level I_2, which is then the starting current for the next cycle, as shown in Fig.4. As the switching sequence repeats, sufficient current begins to flow to give an accelerating torque and thus cause armature rotation. As soon as rotation begins, back emf is generated which subtracts from the supply voltage. The motor equation then becomes:

$$L_a \cdot \frac{di_a}{dt} + R_a \cdot i_a = V_{dc} - E_a \qquad (5)$$

The current drawn from the supply will consequently be less than that drawn at start-up due to the effect of the motor back emf term, E_a. For a given PWM duty cycle ratio, δ, the motor reaches a quiescent speed governed by the load torque and damping friction. Maximum motor torque is required at start-up in order to accelerate the motor and load inertias to the desired speed. The current required at start-up is therefore also a maximum. At the end of the starting ramp the controller duty cycle is reduced because less current is then needed to maintain the motor speed at its steady state value.

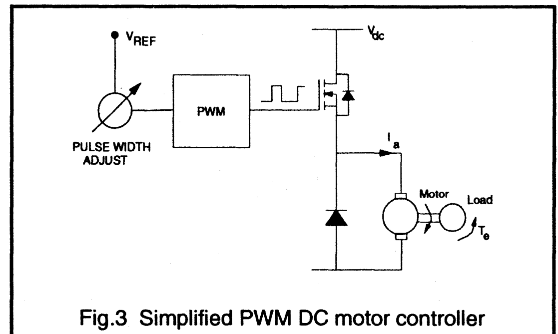


Fig.3 Simplified PWM DC motor controller

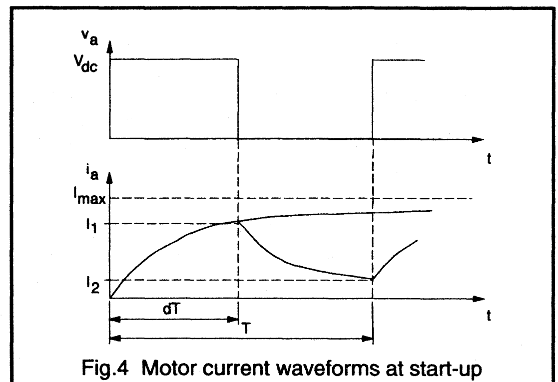


Fig.4 Motor current waveforms at start-up

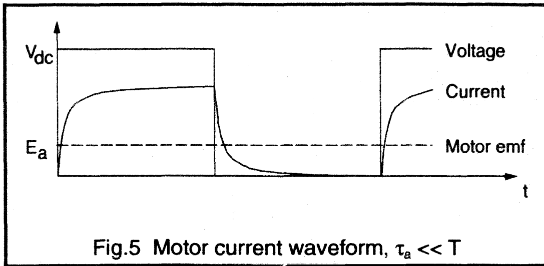


Fig.5 Motor current waveform, $\tau_a << T$

For a low inductance motor where the electrical time constant is much less than the duty cycle then the motor current waveform will closely follow the applied voltage waveform, as shown in Fig.5. An approximate expression for the average motor current is given by:

$$I_{ave} = \delta . \frac{(V_{dc} - E_a)}{R_a} \qquad (6)$$

In summary, the principle control variable in the PWM motor control system is 'duty cycle', δ. Motor torque and velocity can be tightly controlled by controlling the PWM duty cycle and motor current.

The switched mode controller

For the remaining portion of the paper integrated switched-mode control will be considered with specific reference to the NE/SE5560 controller IC. This device incorporates control and protection functions for SMPS and DC motor control applications including internal temperature compensation, internal reference voltages, a sawtooth waveform generator, PWM amplifier and output stage. Protection circuitry includes cycle-by-cycle current limiting, soft start capability, overcurrent protection, voltage protection and feedback loop protection circuits. In the following sections some of the features of the controller will be examined and its use in a number of motor drive designs will be presented.

Fig.6 NE5560 Block diagram

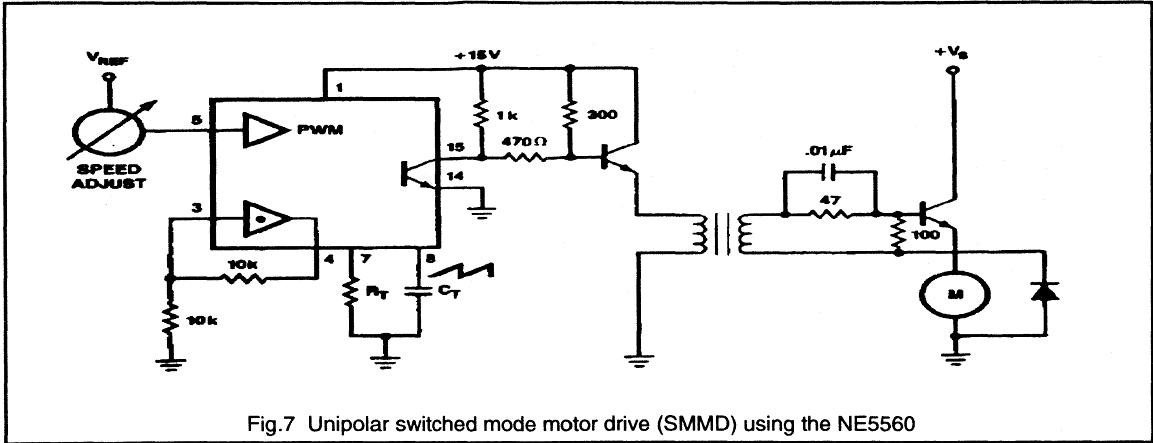


Fig.7 Unipolar switched mode motor drive (SMMD) using the NE5560

The device (see Fig.6) contains an internal voltage reference which is connected to the non-inverting input of the error amplifier. The feedback signal is obtained from either a tachogenerator (TGF - tachogenerator feedback) or from a signal proportional to the armature voltage less the winding iR voltage drop (AVF - armature voltage feedback). This feedback signal must be scaled to centre about the internal voltage reference level. The error amplifier output, in addition to being available for gain adjustment and op amp compensation, is connected internally to the pulse-width modulator. Frequency may be fixed at any value from 50Hz to 100kHz and duty cycle adjusted at any point from 0 to 98%. Automatic shut-down of the output stage occurs at low supply threshold voltage. The error amplifier has 60dB of open loop gain, is stable for closed loop gains above 40dB and can also can be compensated for unity gain. The single ended switching output is from either the emitter or collector of the output stage. The device has protective features such as high speed overcurrent sense which works on a cycle-by-cycle basis to limit duty cycle, plus an additional second level of slow start shutdown. It is this input which can be adapted to act as a motor torque limit detector.

Open loop PWM control using the NE5560

For a given application the switched-mode controller frequency should be set to allow the best dynamic response considering the starting current requirement and motor electrical time constant, as discussed previously. The main drive transistors or MOSFETs must be capable of carrying the peak motor current requirement which occurs at start-up. Device protection using snubber networks and transient suppression networks will depend on the choice of switching device, system ratings and the application requirements. Power MOSFETs provide an excellent solution to many DC drive designs since very low drive power is required and they are self-protected from reverse transients by an internal intrinsic diode. PowerMOS devices may be parallelled for added power handling capability.

Figure 7 shows a simple unipolar drive capable of driving a low voltage motor supplied from an external DC voltage and PWM controlled using the NE5560.

Constant velocity servo

Figure 8 shows in block form the general circuit used to obtain a constant speed switched mode motor drive (SMMD) servo. Figure 8(a) shows a unipolar drive using DC tachometer feedback to the PWM error amplifier. Figure 8(b) shows a bidirectional drive in a half-bridge configuration. In this case the duty cycle controls the direction of motor rotation in addition to the motor speed. A 50% duty cycle corresponds to the standstill condition. If the average duty cycle is greater than 50% (CW command) then the motor accelerates clockwise, and vice-versa for CCW rotation when the duty cycle is less than 50%. This circuit configuration can be used for both velocity and position servo-designs. The reversing switch allows the tachogenerator output to match the polarity of the PWM reference, which is always positive.

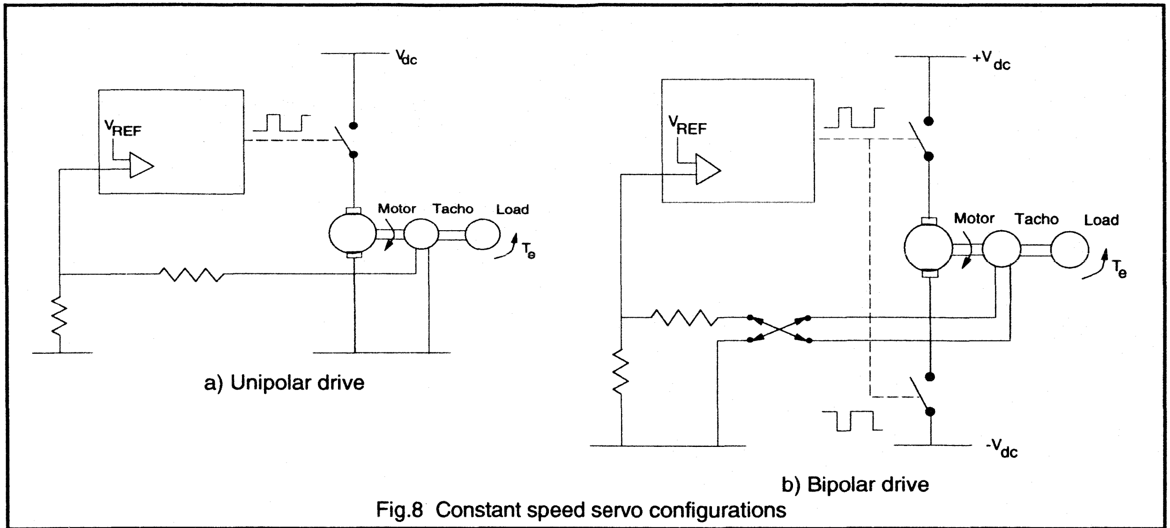


Fig.8 Constant speed servo configurations

Fig.9 Basic unidirectional drive with dynamic braking

The unipolar drive circuit in Fig.9 uses the NE5560 to develop a SMMD with constant speed control suitable for a small DC motor. The switching device is a single Philips BUK426-100A Power MOSFET capable of I_D=20A continuous current, with a voltage rating of 100V V_{DS} and $R_{DS(ON)}$=0.057Ω. The PWM drive from the NE5560 is applied to the gate at a nominal 10kHz, although much higher frequencies are possible. The peak gate to source voltage, V_{GS}, is 15V to ensure minimum $R_{DS(ON)}$ and hence minimum loss in the PowerMOS switch.

A sense resistor is placed in the source lead to monitor motor drive current on a cycle-by-cycle basis. The value of this resistor is set to develop the error amplifier threshold voltage at the desired maximum current. The NE5560 then automatically limits the duty cycle, should this threshold be exceeded. This is therefore used as an auto torque limit feature in addition to simply protecting the switching device. A slow start network (Pins 2,5,6) gradually ramps up the duty cycle at power on. Fixed braking duty cycle control is achieved by forcing the input error amplifier during braking conditions. The over-current circuit is still active during braking.

SMMD Position servo with μP control

By coupling the switched mode motor drive in a bidirectional configuration as shown in Fig.10, and then sensing linear position with a potentiometer or LVDT connected to a lead screw, for instance, the position feedback loop can be closed to give a position servo. The input to control position of the mechanical stage may be fed as a DC offset to a summing amplifier whose output is fed to Pin 5 of the NE5560, as shown. Forward lead-lag compensation may be combined with the summing amplifier function to achieve a stable response. A velocity loop may be closed through the error amplifier at Pin 3. The controller may easily be interfaced to a microprocessor by means of a unipolar D/A converter working in the 1 to 6V output range as an input to Pin 5.

Conclusions

The switched-mode motor drive, SMMD, using small, easily available, monolithic integrated control devices designed for switched-mode power applications may easily be adapted to perform a number of useful and efficient torque, velocity and position control operations. The ready availability of good controller ICs, easily compatible with the Philips range of switching power devices in both bipolar and PowerMOS technologies makes such designs even more effective and easily attainable by the control systems designer.

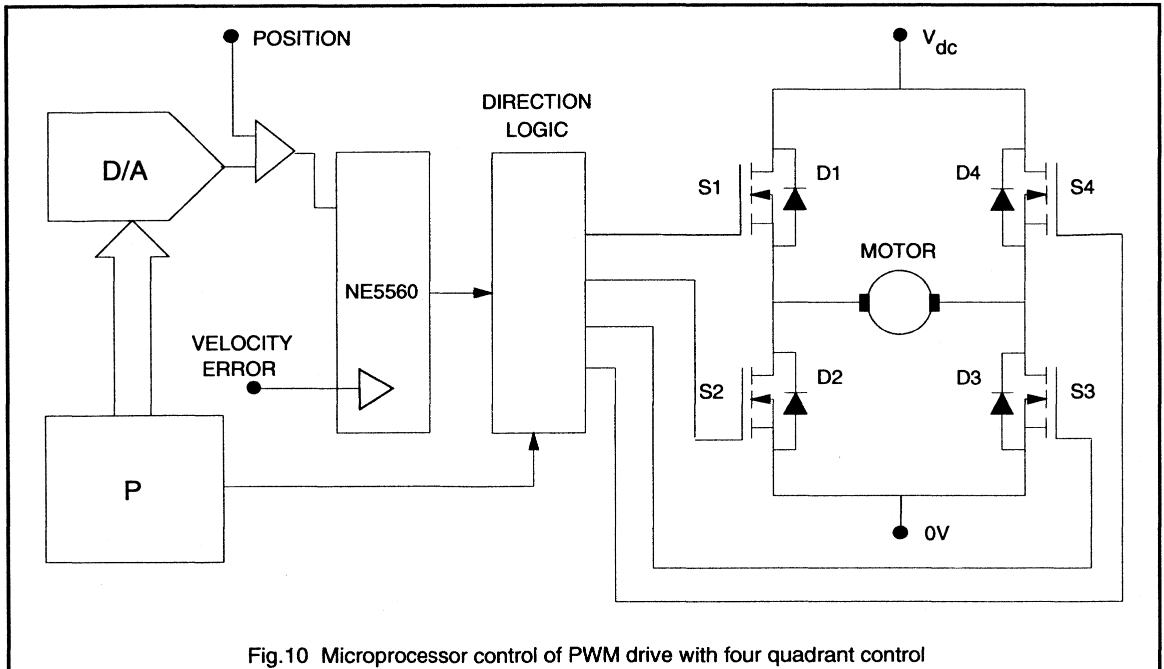


Fig.10 Microprocessor control of PWM drive with four quadrant control

3.2.3 Brushless DC Motor Systems

In recent years the number of drive systems available to designers has increased considerably. The advent and increasing use of stepper motors, inverter-fed ac machines, switched reluctance motors and brushless machines have all addressed particular applications and in some cases these application areas overlap. The correct choice of a drive system for a particular application depends not only upon the speed and torque requirements but also on performance, response, complexity and cost constraints. The brushless DC motor (BDCM) system is emerging as one of the most useful drive options for a wide range of applications ranging from small, low power fans and disc drives, through medium size domestic appliance motors and up to larger industrial and aviational robotic and servo drives.

This section will review the theory and operation of brushless DC motors and describe some of the considerations to be made when designing BDCM drive systems using PowerMOS devices as the main inverter switches.

Background

The principal advantage of a conventional DC machine compared to an AC machine is the ease with which a DC motor can be controlled to give variable speed operation, including direction reversal and regenerative braking capability. The main disadvantage of a DC machine is that the carbon brushes of a DC motor generate dust and also require maintenance and eventual replacement. The RFI generated by the brushgear of a DC motor can be quite large and, in certain environments, the sparks themselves can be unwelcome or hazardous. The brushless DC motor was developed to achieve the performance of a conventional DC machine without the problems associated with its brushes.

The principal advantages of the BDCM system are:

- Long life and high reliability
- High efficiency
- Operation at high speeds and over a wide speed range
- Peak torque capability from standstill up to high speeds
- Simple rugged rotor construction
- Operation in vacuum or in explosive or hazardous environments
- Elimination of RFI due to brush commutation

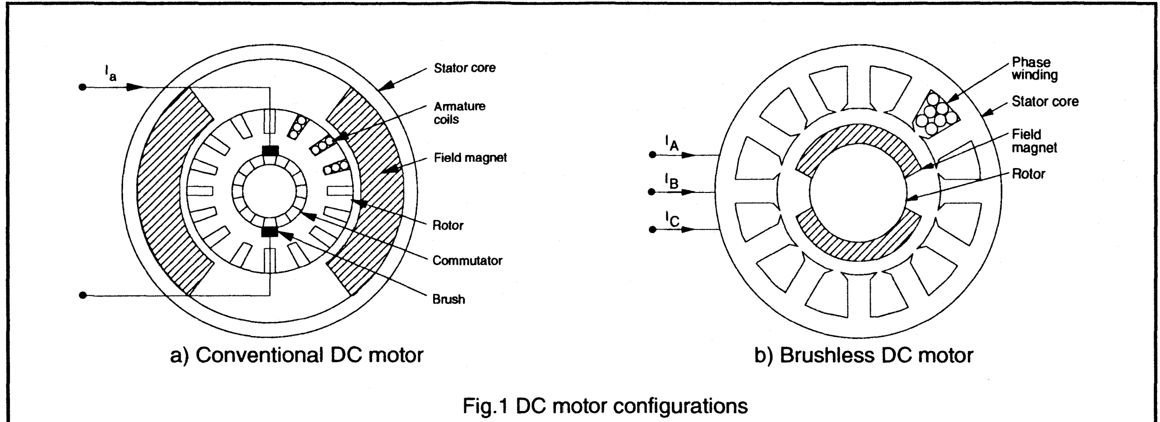
DC motor configurations

In a conventional DC motor the field energy is provided by either a permanent magnet or a field winding. Both of these arrangements involve quite large, bulky arrangements for the field. In the case of wound field DC motors this is due to large number of turns needed to generate the required electromagnetic field in the airgap of the machine. In the case of permanent magnet DC machines the low energy density of traditional permanent magnet materials means that large magnets are required in order to give reasonable airgap fluxes and avoid demagnetisation. If either of these two options are used with the field excitation on the rotor of the machine then the inertia and weight of the rotor make the machine impractical in terms of its size and dynamic response.

A conventional DC machine has a large number of armature coils on the rotor. Each coil is connected to one segment of a commutator ring. The brushes, mounted on the stator, connect successive commutator segments, and hence armature coils, to the external DC circuit as the motor moves forward. This is necessary to maintain maximum motor torque at all times. The brush/commutator assembly is, in effect, a rotating mechanical changeover switch which controls the direction and flow of current into the armature windings.

In a BDCM the switching of current to the armature coils is carried out statically and electronically rather than mechanically. The power switches are arranged in an inverter bridge configuration in order to achieve bidirectional current flow in the armature coils, i.e. two power switches per coil. It is not possible to have a large number of armature coils, as is the case for a conventional DC motor because this would require a large number of switching devices and hence be difficult to control and expensive. An acceptable compromise is to have only three armature coils and hence six power switches. Reducing the number of armature coils means that the motor is more prone to developing ripple torque in addition to the required DC torque. This problem can be eliminated by good design of the motor. The armature of a three coil brushless DC machine in fact looks similar to the stator of a three phase AC machine and the term 'phase' is more commonly used to describe these three separate coils.

The development of brushless DC machines has made possible by developments in two other technologies: namely those of permanent magnet materials and power semiconductor switches.



a) Conventional DC motor

b) Brushless DC motor

Fig.1 DC motor configurations

Permanent magnet materials

Traditional permanent magnet materials, such as AlNiCo magnets and ferrite magnets, are limited either by their low remanence giving rise to a low airgap flux density in electrical machines, or by their susceptibility to demagnetisation in the presence of high electric fields. However in recent years several new permanent magnet materials have been developed which have much higher remanent flux densities, and hence airgap flux densities, and high coercivities, making them resistant to demagnetisation under normal operating conditions. Amongst these materials, called 'rare earth' magnets, Samarium Cobalt ($SmCo_5$ and Sm_2Co_{17}) and Neodymium--Iron-Boron (Nd-Fe-B) are the most common. These materials, although still quite expensive, give vastly superior performance as the field excitation for a brushless machine.

Due to the increased energy density of rare earth magnets the amount of magnet material required by the application is greatly reduced. The magnet volume using rare earths is small enough that it is feasible to have the permanent magnet field on the rotor of the machine instead of on the stator. The gives a low inertia, high torque motor capable of high performance operation. This resulting motor design, with the armature on the stator and the field on the rotor and shown in Fig.1, can be considered as a conventional DC motor turned 'inside out.'

Power electronic switches

For the 'inside out' BDCM is it still necessary to switch the armature current into successive armature coils as the rotor advances. As the coils are now on the stator of the machine the need for a commutator and brushgear assembly has disappeared. The development of high voltage and high current power switches, initially thyristors, bipolar power transistors and Darlingtons, but more recently MOSFETs, FREDFETs, SensorFETs and IGBTs, has meant that motors of quite large powers can be controlled electronically, giving a feasible BDCM system. The question of appropriate device selection for brushless DC drives will be considered later.

System description (Fig.2)

DC power supply

The fixed DC voltage is derived from either a battery supply, low voltage power supply or from a rectified mains input. The input voltage may be 12V or 24V as used in many automotive applications, 12V-48V for applications such as disc drives or tape drives, or 150V-550V for single-phase or three-phase mains-fed applications such as domestic appliances or industrial servo drives or machine tools.

Inverter

The inverter bridge is the main power conversion stage and it is the switching sequence of the power devices which controls the direction, speed and torque delivered by the motor. The power switches can be either bipolar devices or, more commonly, PowerMOS devices. Mixed device inverters, for example systems using pnp Darlingtons as the high side power switches and MOSFETs as the low side switches, are also possible. The freewheel diodes in each inverter leg may be internal to the main power switches as in the case of FREDFETs or may be separate discrete devices in the case of standard MOSFETs or IGBTs. Detailed considerations of inverter design, gate drive design and layout have been considered in separate articles.

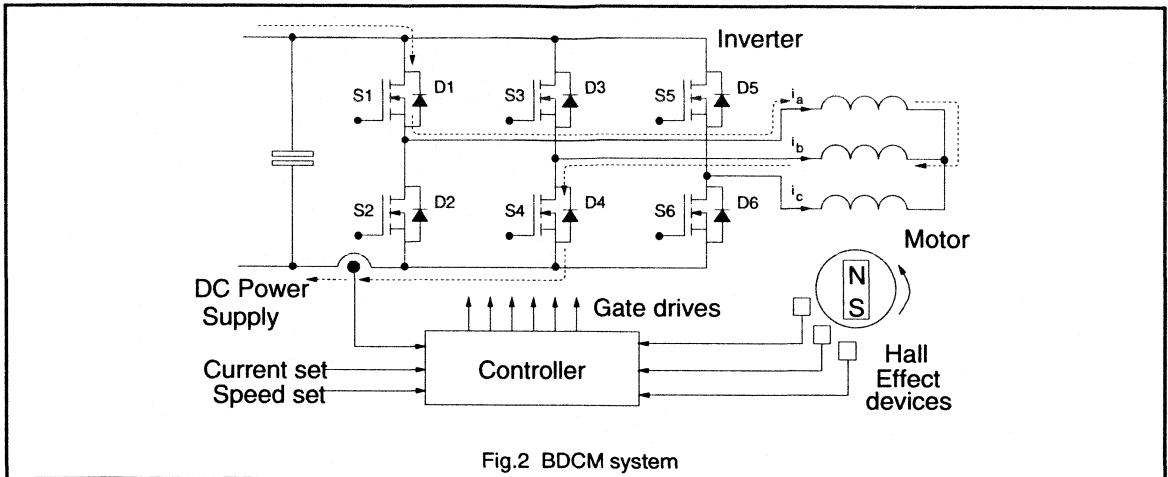


Fig.2 BDCM system

The inverter switching speed may be in the range 3kHz to 20kHz and above. For many applications operation at ultrasonic switching speeds (>15-20kHz) is required in order to reduce system noise and vibration, reduce the amplitude of the switching frequency currents and to eliminate switching harmonic pulsations in the motor. Because of the high switching speed capability of PowerMOS devices they are often the most suitable device for BDCM inverters.

The first choice for the inverter devices might appear to be one with an N-channel MOSFET for the bottom device in each inverter leg and a P-channel device in the top half of each leg. The disadvantage of P-channel devices is that they require around three times more silicon area than equivalent N-channel MOSFETs to achieve the same value of $R_{DS(ON)}$. This makes P-channel devices uncompetitively expensive for many applications. However, using N-channel devices for both the top and bottom switches in an inverter leg means that some sort of floating drive is required for the upper device. Transformer coupled or optically coupled gate driver stages are required, or alternatively, circuits such as the bootstrap circuit shown in Fig.3 can be used to provide the drive for the top device.

In the circuit of Fig.3 the bootstrap capacitor is charged up via the diode D every time the bottom MOSFET is on. When this device turns off the capacitor remains charged up to the gate supply voltage as D is now reverse biassed. When a turn-on pulse is applied for the upper MOSFET the bootstrap capacitor provides the necessary gate source voltage to turn the device on.

Motor

A two pole BDCM with the field magnets mounted on the surface of the rotor and with a conventional stator assembly was shown in Fig.1. Machines having higher numbers of poles are often used depending upon the application requirements for motor size, rotor speed and inverter frequency. Alternative motor designs, such as disc motors or interior magnet rotor machines, are also used for some applications. The motor phases are usually connected in a star configuration as shown in Fig.2. Rotor position sensors are required in order to control the switching sequence of the inverter devices. The usual arrangement has three Hall effect sensors, separated by either 60˚ or 120˚, mounted on the stator surface close to the airgap of the machine. As the rotor advances the switching signals from these Hall Effect latches are decoded into rotor position information in order to determine the inverter firing pattern.

In order to minimise torque ripple the emf induced in each motor phase winding must be constant during all instants in time when that phase is conducting current. Any variation in a motor phase emf whilst it is energised results in a corresponding variation in the torque developed by that phase. The so-called 'trapezoidal emf' motor, shown in Fig.4, has a constant induced emf for 120˚ and so is a practical motor design which gives optimum performance in a BDCM system.

Controller

The inverter is controlled in order to limit the device currents, and hence control the motor torque, and to set the direction and speed of rotation of the motor. The average ouput torque is determined by the average current in each phase when energised. As the motor current is equal to the DC link current (Fig.2) then the output torque is proportional to the DC input current, as in a conventional DC motor. The motor speed is synchronous with the applied voltage waveforms and so is controlled by setting the frequency of the inverter switching sequence.

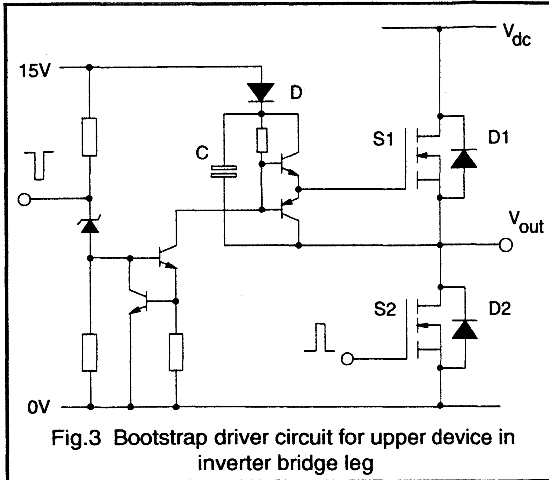


Fig.3 Bootstrap driver circuit for upper device in inverter bridge leg

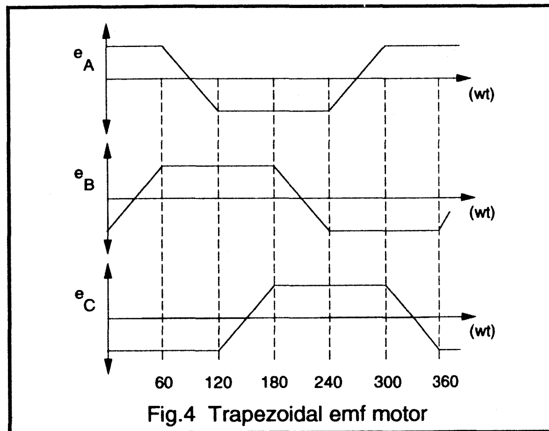


Fig.4 Trapezoidal emf motor

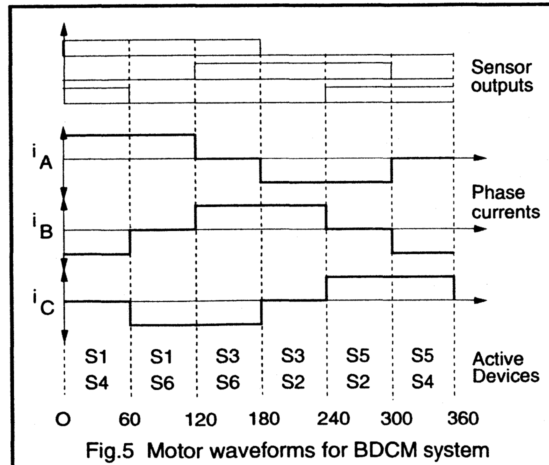


Fig.5 Motor waveforms for BDCM system

Rotor position feedback signal are derived from the Hall effect devices as discussed earlier or from opto-transducers with a slotted disc arrangement mounted on the rotor shaft. It is also possible to sense rotor position by monitoring the emfs in the motor phase windings but this is somewhat more complex. In some applications the Hall effect sensor outputs can be used to provide a signal which is proportional to the motor speed. This signal can be used in a closed loop controller if required.

The controller also requires a current feedback signal. Usually this is taken from the DC link of the inverter as shown in the Fig.2. The current is controlled using either PWM techniques or hysteresis type of control. A current reference command is compared with the current feedback signal and then used to determine the switching signal to the main power devices. Additional controller functions include undervoltage protection, thermal protection and current ripple limit controls, error amplifier inputs for incorporation in closed loop servos and microprocessor compatible inputs.

Several IC manufacturers offer dedicated ICs providing all the functions for PWM control of brushless DC motors. The Philips version of the NE5570 CMOS controller is one such device which can be used for three phase BDCM systems using a serial data input command from a microprocessor controller. This device contains the PWM comparator and oscillator, dynamic current loop controller and output pre-drivers suitable for a MOSFET power stage. Its operation is described more fully in Philips Application Note AN1281.

Brushless DC motor operation

The operation of a BDCM system can be explained with reference to Fig.5. At any instant in time the rotor position is known by the output states of the three airgap mounted Hall effect devices. The output state of one Hall effect device switches for every 60˚ of rotation, thus defining six conduction zones as shown in the Figure. The switching of the inverter devices is arranged to give symmetrical 120˚ intervals of positive and negative constant current in each motor phase winding. The position of the sensors and controller logic ensures that the applied currents are in phase with the motor emfs in order to give maximum motor torque at all times.

Referring to Figures 2 and 5, during the first 60˚ conduction zone switches S1 and S4 are on and the current flows through the 'A' and 'B' phase windings. The 'C' phase is inactive during this interval. At the end of this 60˚ conduction zone one of the Hall effect devices changes state and so switch S1 turns off and S3 turns on. The switching sequence continues as the motor advances. At any instant in time two motor phases are energised and one motor phase is off. The motor phase current waveforms are described as being

'quasi-square' in shape. The motor windings are energised for two thirds of the total time and the maximum switch duty cycle ratio is one third.

The other function of the controller is to maintain the motor phase currents at their desired constant value for each 120° interval that a particular phase is energised. The precise method of current limiting depends upon the controller algorithm. In order to limit the current to its desired value either one or both of the conducting devices are switched off thus allowing the motor current to freewheel through the bridge leg diodes. The current is limited by controlling the switch duty cycle to ensure that device current ratings and the motor current rating are not exceeded, especially during start-up conditions or low speed operation. The amount of current ripple is controlled by the switching frequency of a PWM waveform or by the width of a hysteresis band.

Power Semiconductor switches for Brushless DC motors

Philips Components produce a range of power semiconductor devices suitable for use in BDCM systems. The include transistors and Darlingtons, MOSFETs, FREDFETs, Logic Level MOSFETs (L^2FETs), SensorFETs and IGBTs. These devices are available in a variety of current and voltage ratings and a range of packages, including high power packages such as ISOTOP, to suit individual applications.

FREDFETs

For higher voltage applications the FREDFET is an appropriate device for the inverter switches in a brushless DC drive. The FREDFET is a PowerMOS device where the characteristics of the MOSFET intrinsic diode have been upgraded to those of a discrete fast recovery diode. Thus the FREDFET is ideally suited to bridge circuits such as that shown in Fig.2 where the recovery properties of the bridge diodes significantly affect the switching performance of the circuit. Fig.6 shows a conventional MOSFET inverter bridge circuit, where the MOSFETs intrinsic diode is disabled by a series Schottky diode. A discrete antiparallel FRED carries the motor freewheeling current. Using the FREDFET reduces the component count and circuit layout complexity considerably.

L^2FETs

For many lower voltage applications logic level FETs (L^2FETs) can be used to interface the power circuit with standard TTL or CMOS drive circuits without the need for level shifting stages. L^2FETs require gate source voltage of only 5V in order to reach device saturation and typically have $V_{GS(th)}$ = 1-2V. Using Philips L^2FETs in BDCM applications such as tape or disc drives where the MOSFETs are driven directly by a controller IC produces an efficient overall design with the minimum of gate drive components.

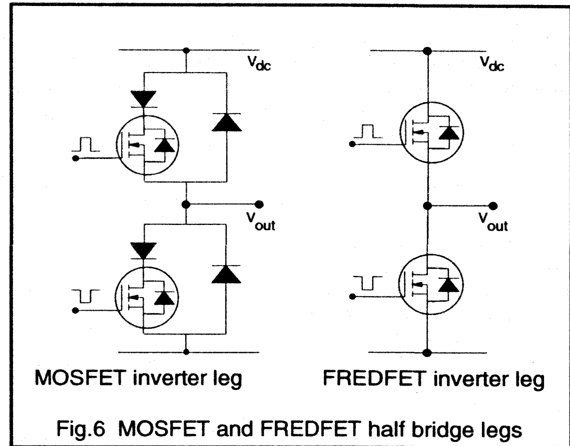


Fig.6 MOSFET and FREDFET half bridge legs

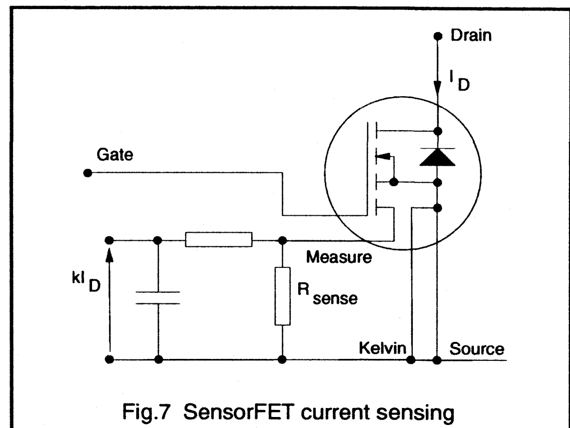


Fig.7 SensorFET current sensing

SensorFETs

Referring to Fig.2 earlier it can be noted that a current feedback signal is essential to the operation of the BDCM system. Traditionally current sensing has involved the use of either a current transformer or a series resistor in the DC link circuit. The former option is expensive and inconvenient whilst the latter option results in extra loss in the sense resistor which usually must be an accurate high power, and hence expensive, component. However with the introduction of SensorFETs as a new and important part of the PowerMOS family of devices, current sensing in inverter circuits can be simplified considerably. Using SensorFETs in BDCM inverter gives an accurate current feedback signal without any of the disadvantages associated with DC link current sensing methods.

In a SensorFET some of the many individual MOSFET cells which make up a PowerMOS device are separated out from the main source terminal and brought out to a device sense terminal. As the drain current in a MOSFET is shared equally between all the cells of the device then the ratio of the current in the sense cells to the source current is determined by the ratio of the number of sense cell to power cells. Thus using SensorFET in a motor control application allows measurement of only a fraction of the total MOSFET current in the feedback loop. The sensed current is usually filtered to remove noise spikes which occur due to capacitive coupling or reverse recovery overcurrents in the top device freewheeling diodes as shown in Fig.7. The current feedback signal is then monitored using a cheap, simple low power sensing circuit.

IGBTs

IGBTs are especially suited to higher power applications where the conduction losses of a MOSFET begin to become prohibitive. The IGBT is a power transistor which uses a combination of both bipolar and MOS technologies to give a device which has low on-state losses and is easy to drive. The IGBT is finding applications in mains-fed domestic and industrial drive markets. By careful design of the device characteristics the switching losses of an IGBT can be minimised without adversely affecting the conduction losses of the device too severely. Operation of BDCM inverters is possible at switching speeds of up to 20kHz using IGBTs.

Device selection

The first selection criterion for an inverter device is the voltage rating. Philips PowerMOS devices have excellent avalanche ruggedness capability and so are able to survive transient overvoltages which may occur in the inverter circuit. This gives the circuit designer the freedom to choose appropriately rated devices for the application without suffering from the extra device conduction losses which occur when using higher voltage grade devices. In noisy environments or where sustained overvoltages occur then some external protection circuitry will usually be required.

For low voltage and automotive applications 60V devices may be adequate. For mains-fed applications then the DC link voltage is fixed by the external mains supply. A 240V supply will, depending on the DC link filtering arrangement, give a link voltage of around 330V. Using 450V or 500V MOSFETs will allow sufficient margin for transient overvoltages to be well within the device capability.

The current rating of a device is determined by the worst case conditions that the device will experience. These will occur during start-up, overload or stall conditions and should be limited by the BDCM controller. Short circuit protection must be provided by using appropriate fusing or overcurrent trip circuitry.

In addition to the normal motor currents the inverter devices will experience additional currents due to diode reverse recovery effects. The magnitude of these overcurrents will depend on the properties of the freewheel diodes and on the switching rates used in the circuit. Turn-on overcurrents can often be greater than twice the normal load current. The peak to average current capability of MOSFETs is very good (typically 3 to 4) and so they are able to carry overcurrents for short periods of time without damage. For high power applications PowerMOS devices can easily be parallelled to give the required current ratings providing the circuit is suitably arranged in order to ensure good current sharing under both dynamic and static conditions.

Conclusions

The brushless DC motor has already become an important drive configuration for many applications across a wide range of powers and speeds. The ease of control and excellent performance of the brushless DC motors will ensure that the number of applications using them will continue to grow for the foreseeable future. The Philips range of PowerMOS devices which includes MOSFETs, FREDFETs, SensorFETs, L^2FETs and IGBTs are particularly suited for use in inverter circuits for motor controllers due to their low loss characteristics, excellent switching performance and ruggedness.

Stepper Motor Control

3.3.1 Stepper Motor Control

A stepper motor converts digital information into proportional mechanical movement; it is an electro-mechanical device whose spindle rotates in discrete steps when operated from a source that provides programmed current reversals. After the appearance of the stepper motor in applications traditionally employing digital control, the advantages of precise and rapid positioning of objects using stepper motor drive systems became more obvious and this, in turn, led to a greater variety of applications. These now include:

- paper and magnetic tape drives,
- camera iris control and film transport,
- co-ordinate plotters, printers, chart recorders and variable speed chart drives,
- medical equipment,
- fuel control, valve control and variable speed pumps,
- meters, card readers, production line pulse counters
- automatic weighing and labelling systems,
- digital to analogue converters and remote position indicating equipment.

All of these applications have one thing in common - controlled motion. Wherever controlled movement and/or positioning is necessary, the stepper motor can be used to give a fast, flexible and accurate system.

From a mechanical viewpoint, the stepper motor has simple positional control, reliability and precision. Previously, simple, mechanically operated switches often provided adequate control for many positioning systems but increased performance requirements have forced the need for a better drive systems. The advantages of stepper motor systems have been gained at the expense of controller simplicity. The combination of fast controller ICs, low cost, high power, high efficiency switches, particularly MOSFETs, and the ease of use of stepper motors has lead to their current widespread use.

The full benefit of a stepper motor can only be realised if it is correctly driven. It requires a dc supply, an electronic switch and a source of control pulses (digital information). The appropriate dc supply is directed into the motor via a power electronic switching network. In effect, the motor moves through one step for each control pulse applied to the power stage electronic switches. The angle of the step depends upon the type of motor and can be from as little as 1.8˚ to as much as 15˚. Consequently, if 24 pulses are fed to the switching network, the shaft of a motor with a 15˚ step-angle will complete one revolution. The time taken for this action is entirely a function of the rate at which control pulses are applied. These may be generated by an oscillator with adjustable frequency or from a dedicated controller IC.

Principles of operation

Stepper motors can be divided into three principle types:

- permanent magnet stepper motors
- variable reluctance stepper motors
- hybrid stepper motors.

Permanent magnet stepper motors

The step angle of a permanent magnet stepper motor depends upon the relationship between the number of magnetic poles on its stator assembly and the number of magnetic poles on its rotor. Since the latter is a cylindrical permanent magnet, the poles are fixed, and their number is limited, due to the characteristics of the magnetic material. Enlarging the magnet diameter to provide for a larger number of rotor poles results in a drastic increase in the rotor inertia. This reduces the starting capabilities of such a motor beyond practical use. With a permanent magnet rotor, only relatively large step angles can be obtained. However, the operating step angle can be reduced by using more than one stator stack along the length of the machine and then by offsetting the separate stacks.

The stator assembly comprises two or more stators, each having a coil through which current is passed to form a magnetic field. By reversing the direction of current flowing in a coil the north and south poles developed by the coils can be transposed. Reversing the current flow through successive stator coils creates a rotating magnetic field which the permanent-magnet rotor follows. Speed of rotation is thus governed by the rate at which the stator coils (and hence the electromagnetic poles) are switched and the direction of rotation by the actual switching sequence.

There are two methods by which the current flow through stator coils can be reversed and this has led to two classes of stepper motor: those designed for unipolar drive and those for bipolar drive. For ease of description, illustrations in this section which give a diagrammatic representation of a permanent magnet stepper motor show only a 2-pole rotor although it could have as many as 24: the operating principles, however, are the same.

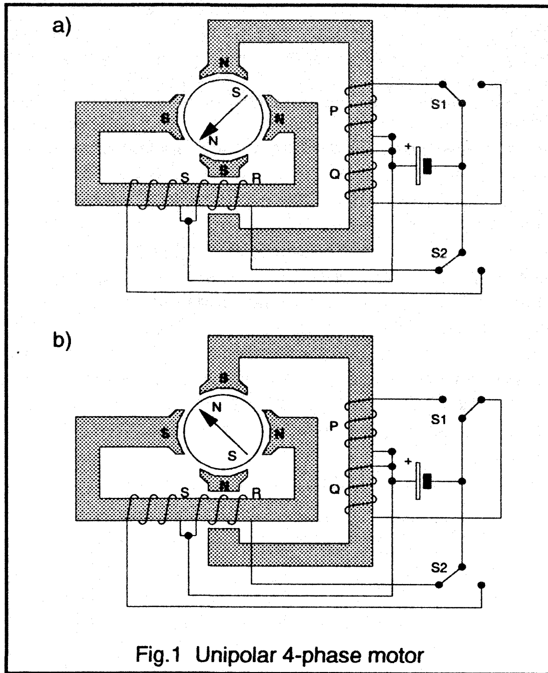


Fig.1 Unipolar 4-phase motor

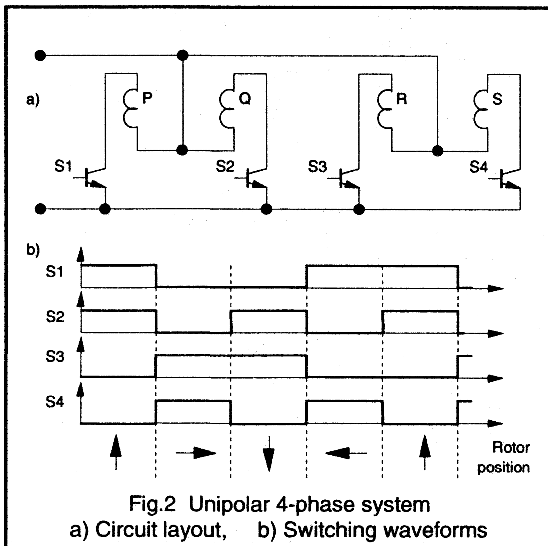


Fig.2 Unipolar 4-phase system
a) Circuit layout, b) Switching waveforms

Motors for Unipolar drive

Each stator coil of a motor designed for unipolar drive is provided with a centre-tap which is connected to one side of the supply. The direction of current flowing through a coil is then determined by the end to which the other supply line is connected via a switching device. Switching between the coil halves results in the magnetic poles of the relevant stator being reversed.

Figure 1(a) shows a 4-phase stepper motor in which phases P and R are energised. The north poles at P and R cause the rotor to align in the position indicated. If switch S1 is now operated so that phases Q and R are now energised then the stator field is repositioned and so the conditions illustrated in Fig.1(b) are obtained, ie. the rotor has moved through 90˚ to align with the stator field. From this it can be seen that by altering the switching sequence for switches S1 and S2 the rotor can be made to advance in either direction.

Figure 2(a) shows the drive configuration for a unipolar 4-phase motor. The switching sequence of the power switches is shown in Fig.2(b). Two motor phases are energised at any one time thus giving the rotation of the stator field and required stepping motion.

Motors for Bipolar drive

The stator coils of a motor designed for bipolar drive have no centre-tap. Instead of using alternate coil-halves to produce a reversal of current-flow through the stator windings, the current is now reversed through the entire coil by switching both supply lines. Operation of a motor with bipolar drive is identical to that of one with unipolar drive, and is shown in Fig.3. Here, when the polarity of current in phase P is reversed using switch S1 the stator field realigns and the rotor moves accordingly. Fig.4(a) shows the drive configuration for a bipolar 4-phase motor. The devices are always switched as pairs, i.e. S1 and S4, S2 and S3. The switching waveforms for this configuration are shown in Fig.4(b).

The advantages of using motors with bipolar drive are shown in Fig.5. This compares the performance of a unipolar motor with its bipolar equivalent. Unipolar motors develop less torque at low stepping rates than their bipolar counter-parts, although at higher stepping rates the torque developed by both types of motor is nearly the same.

The 4-phase unipolar motor shown in Fig.1 has two coils per phase which must be wound on one bobbin for each stator (bifilar winding), ie. four coils in total. Because the two coils occupy the same space as a single coil in equivalent bipolar types, the wire is thinner and coil resistance higher. Bipolar motors have only one coil per bobbin so that 2-stator motors have two coils and 4-stator motors four coils. Unipolar motors require only a simple drive circuit - only four power transistors instead of eight. Moreover, the switching time requirements are less severe for unipolar drives. For a bipolar drive, care must be taken with switching times to ensure that two opposing transistors are not switched on at the same time, thus shorting out the supply. Properly operated, bipolar windings give optimum motor performance at low to medium stepping rates.

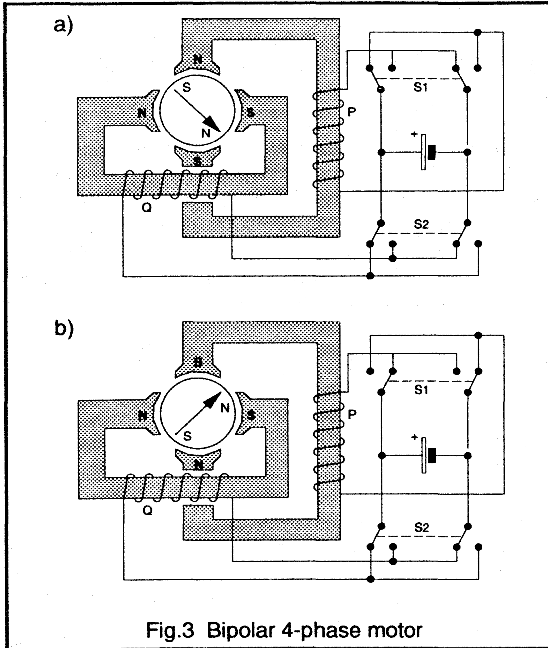


Fig.3 Bipolar 4-phase motor

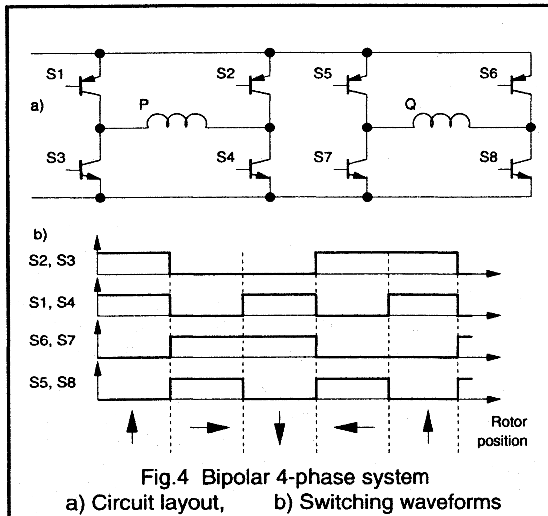


Fig.4 Bipolar 4-phase system
a) Circuit layout, b) Switching waveforms

Variable reluctance stepper motors

In a variable reluctance stepper motor the motion is achieved by using the force of attraction between a magnetised component (the stator pole excited by a controlled current) and a passive steel component (the rotor pole). As successive stator poles are energised different rotor poles are attracted towards the nearest active pole, thus giving the required stepping motion. Fig.6 shows the simplest variable reluctance motor configuration having six stator poles and four rotor poles. The rotor is simply a shaped steel shaft. The stator winding is arranged so that one stator phase winding is on each stator pole.

Figure 6(a) shows the condition when the 'A' phase of the motor is energised and rotor pole 1 is aligned with the energised winding. If stator phase 'A' is switched off and phase 'B' is switched on then rotor pole 2 (which is the nearest rotor pole to any 'B' phase pole) experiences an attractive force due to the energised 'B' phase. The rotor advances to the position shown in Fig.6(b). If, subsequentally, phase 'C' is energised then rotor pole 1 will align with the 'C' phase, as shown in Fig.6(c). The step angle of a variable reluctance motor can be reduced by having more than one set of offset rotor poles which are built up along the stack length of the machine. Different offset rotor poles align with the stator poles at each step position.

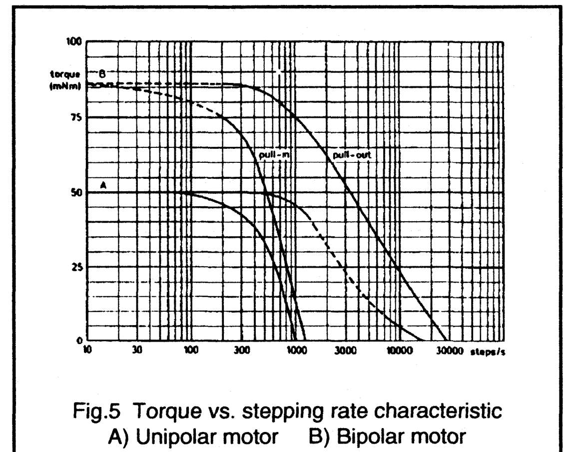


Fig.5 Torque vs. stepping rate characteristic
A) Unipolar motor B) Bipolar motor

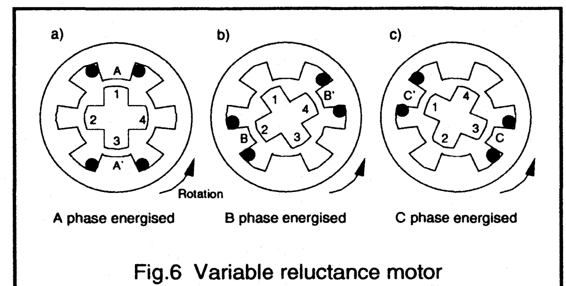


Fig.6 Variable reluctance motor

Hybrid stepper motors

The usual configuration for a hybrid stepper motor operates using the torque production methods found in both permanent magnet and variable reluctance motors. This gives a higher performance system with a low volume, and hence a low rotor inertia, and small step angles. The rotor

of a hybrid stepper motor consists of an axially aligned magnet and a pair of toothed discs, one at each end of the rotor stack. The general layout is shown in Fig.7. The teeth of the discs are misaligned with respect to each other with the result that as the stator phase windings are energised different teeth align with the stator poles, in a similar way to those in a variable reluctance motor. The addition of the permanent magnet on the rotor introduces a polarity in the way that the rotor teeth align with the stator poles. Again multi-stack motors are used to reduce the step length further. Alternative hybrid stepper motor configurations have the magnets on the stator, but operate in a broadly similar manner.

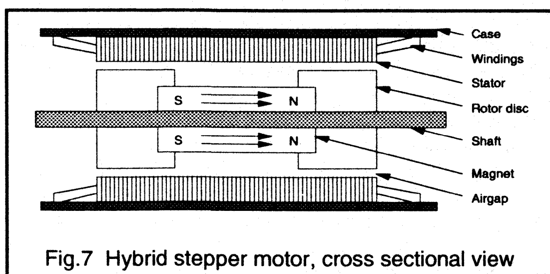


Fig.7 Hybrid stepper motor, cross sectional view

Stepper motor systems

Proper selection of the right stepper motor for a specific application calls for a thorough understanding of the characteristics of the motor and its drive circuitry. Figure 8 shows schematically the four constituent parts of a stepper motor system together with the most important aspects of each. These will be briefly considered below.

The stepper motor

Typical standard step motor angles are shown below:

Step angle	Steps per revolution
0.9°	400
1.8°	200
3.6°	100
3.75°	96
7.5°	48
15.0°	24

The no load step angle accuracy is specified for each type of motor For example, a motor having a step angle of 7.5° and will typically position to within 20' (i.e. 5%) whether the motor is made to move for 1 step or 1000 steps. The step angle error is non-cumulative and averages to zero every four steps, i.e. 360°. Every four steps the rotor returns to the same position with respect to magnetic polarity and flux paths. For this reason, when very accurate positioning is required, it is advisable to divide the required movement into multiples of four steps. This is known as the 4-step mode of operation.

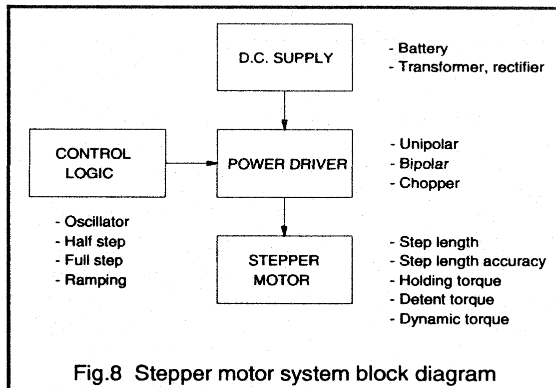


Fig.8 Stepper motor system block diagram

Torque

Three torques are used to define stepper motor operation:

Holding torque

At standstill, when energised, a certain amount of torque is required to deflect a motor by one step. This is known as the holding torque. When a torque is applied that exceeds the holding torque the motor will rotate continuously. The holding torque is normally higher than the working torque and acts as a strong brake in holding a load in position.

Detent torque

Due to their permanent magnets, hybrid stepper motors and permanent magnet stepper motors have a braking torque even when the stator windings are unenergised. This is referred to as the detent torque.

Working (dynamic) torque

The dynamic characteristics of a stepper motor are described by the curves of torque versus stepping rate. Typical curves were shown in Fig.5. The pull-in curve shows the load a motor can start and stop without losing steps when operated at a constant stepping rate. The pull-out curve shows the torque available when the motor is gradually accelerated to and decelerated from its required working speed. The area between the two curves is known as the slew range. The characteristic curves are used to define the correct motor selection for any particular application.

Overshoot

After executing each single step the rotor tends to overshoot and oscillate about its final position as shown in Fig.9(a). This is normal behaviour for any pulsed dynamic system. The actual response depends on the load and on the power input provided by the drive. The response can be modified by increasing the frictional load or by adding mechanical

damping. However, mechanical dampers such as friction discs or fluid flywheels add to system cost and complexity and so it is usually better to damp electronically.

Two methods of electronic damping are commonly used - the simplest being to delay the final pulse in an incremental pulse train such that the effective length of the final step is reduced. Alternatively, every pulse, or just the final pulse in a train, can be modified into three stages, as shown in Fig.9(b). Using this method of damping a forward pulse is applied at time t_0, a reverse pulse is applied at t_1 in order to slow the rotor down and then finally a second forward pulse is applied at t_2 which ensures the rotor comes to rest at the desired position. The accelerating torque which is developed from this final pulse is less than that for a full step and so the shaft overshoot is significantly reduced.

Multiple stepping

There are often several alternatives available in order to make a desired incremental movement. For example, a rotation of 90˚ can be reached in 6 steps of a 15˚ motor, 12 steps of 7.5˚ motor or in 50 steps of a 1.8˚ motor. Generally, a movement executed in a large number of small steps will result in less overshoot, be stiffer and more accurate than one executed in smaller number of large steps. Also there is more opportunity to control the velocity by starting slowly, accelerating to full speed and then decelerating to a standstill with minimum oscillation about the final position if small step lengths are used.

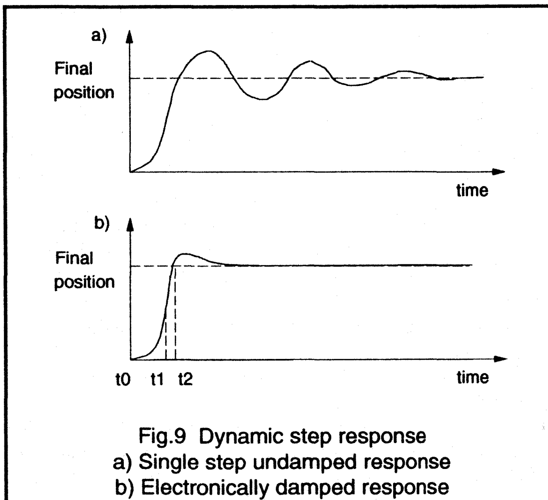


Fig.9 Dynamic step response
a) Single step undamped response
b) Electronically damped response

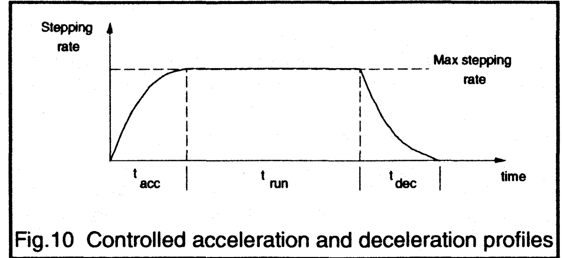


Fig.10 Controlled acceleration and deceleration profiles

A voltage controlled oscillator and charging capacitor are usually used for acceleration (or ramp) control of the motor. The RC time constant of the ramp controller is used to give different ramp rates. Fig.10 shows a typical curve of step rate against time for an incremental movement with equal acceleration and deceleration times.

Resonance

A stepper motor operated at no-load over its entire operating frequency range will exhibit resonance points that are either audible or can be detected by vibration sensors. If any are objectionable then these drive frequencies should be avoided, a softer drive used, or alternatively extra inertia or external damping added.

Drive methods

The normal drive method is the 4-step sequence mentioned above. However, other methods can be used depending on the coil configuration and the logic pattern in which the coils are switched:

Wave drive

Energising only one winding at a time is called wave excitation and produces the same position increment as the 4-step sequence. Figure 11 shows the stepping sequence for the bipolar 4-phase motor, which was discussed earlier and shown in Fig.4. Since only one winding is energised, holding torque and working torque are reduced by 30%. This can, within limits, be compensated by increasing supply voltage. The advantage of this form of drive is higher efficiency, but at the cost of reduced step accuracy.

Half-step mode

It is also possible to step a motor in a half-step sequence, thus producing half steps, for example 3.75˚ steps from a 7.5˚ motor. A possible drawback for some applications is that the holding torque is alternately strong and weak on successive motor steps. This is because on 'full' steps only one phase winding is energised whilst on the 'half' steps two stator windings are energised. Also, because current and flux paths differ on alternate steps, accuracy will be worse than when full stepping. The switching sequence for a 4-phase bipolar drive is shown in Fig.12.

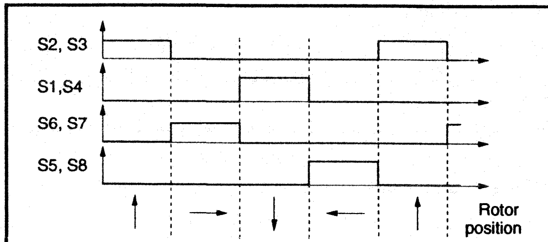


Fig.11 Wave drive switching for 4-phase bipolar stepper motor

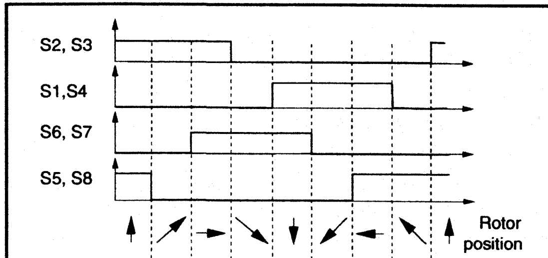


Fig.12 Half stepping switching for 4-phase bipolar stepper motor

Supply considerations

When a motor is operated at a fixed rated voltage its torque output decreases as step rate rises. This is because the increasing back EMF and the rise time of the coil current limits the power actually delivered to the motor. The effect is governed by the motor time constant (L/R). Because of their higher winding resistance unipolar motors have a better L/R ratio than their bipolar equivalents. The effect can be compensated by either increasing the power supply voltage to maintain constant current as stepping rate increases, or by increasing supply voltage by a fixed amount and adding series resistors to the circuit.

Adding series resistors to the drive circuit can improve the motor performance at high stepping rates by reducing the L/R ratio. Adding a series resistor three times the winding resistance would give a modified ratio of L/4R. Supply voltage would then have to be increased to four times the motor rated voltage to maintain rated current. The addition of the extra resistance greatly reduces the drive efficiency. If the increased power consumption is objectionable some other drive method such as a bi-level voltage supply or a chopper supply should be used.

Bi-level drive

With a bi-level drive the motor is operated below rated voltage at zero step rate (holding) and above rated voltage when stepping. It is most efficient for fixed stepping rates. The high voltage may be turned on by current sensing resistors or, as in the circuit of Fig.13, by means of the inductively generated turn-off current spikes. At zero step rate the windings are energised from the low voltage. As the windings are switched in the 4-step sequence, diodes D1, D2, D3 and D4 turn on the high voltage supply transistors S1 and S2.

Chopper drive

A chopper drive maintains current at an average level by switching the supply on until an upper current level is reached and then switching it off until a lower level is reached. A chopper drive is best suited to fast acceleration and variable frequency applications. It is more efficient than an analogue constant current regulated supply. In the chopper circuit shown in Fig.14, V+ would be typically 5 to 10 times the motor rated voltage.

Spike suppression

When windings are turned-off, high voltage spikes are induced which could damage the drive circuit if not suppressed. They are usually suppressed by a diode across each winding. A disadvantage is that torque output is reduced unless the voltage across the transistors is allowed to build up to about twice the supply voltage. The higher this voltage the faster the induced fields and currents collapse and performance is, therefore, better. For this reason a zener diode or series resistor is usually added as in Fig.15.

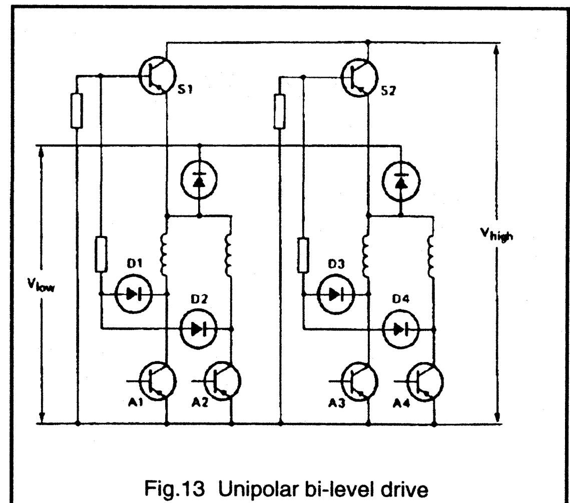


Fig.13 Unipolar bi-level drive

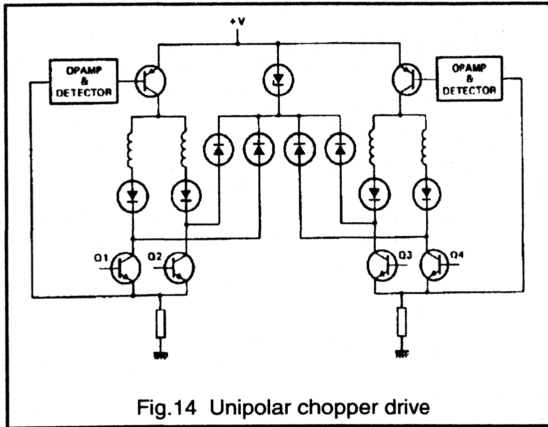


Fig.14 Unipolar chopper drive

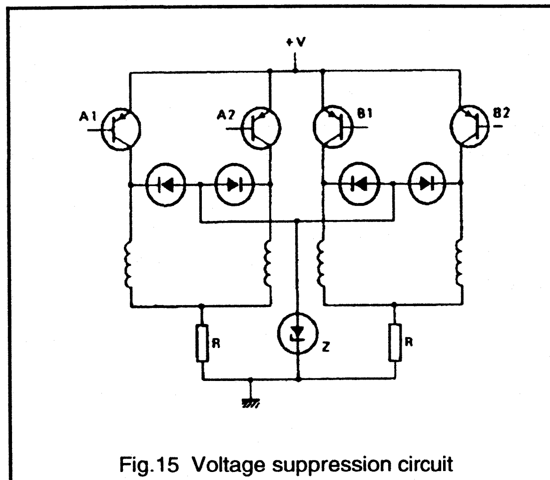


Fig.15 Voltage suppression circuit

Performance limitations

At standstill or low step rates, increasing the supply voltage produces proportionally higher torque until the motor magnetically saturates. Near saturation the motor becomes less efficient so that increased power in unjustifiable. The maximum speed of a stepper motor is limited by inductance and eddy current losses. At a certain step rate the heating effect of these losses limits any further attempt to get more speed or torque out of a motor by driving it harder.

Terminology

Detent Torque: The maximum torque that can be applied to the spindle of an unexcited motor without causing continuous rotation. *Unit:* Nm.

Deviation: The change in spindle position from the unloaded holding position when a certain torque is applied to the spindle of an excited motor. *Unit:* degrees.

Holding Torque: The maximum steady torque that can be externally applied to the spindle of an excited motor without causing continuous rotation. *Unit:* Nm.

Maximum Pull-In Rate (Speed): The maximum switching rate (speed) at which an unloaded motor can start without losing steps. *Unit:* steps/s (revs/min).

Maximum Pull Out Rate (Speed): The maximum switching rate (speed) which the unloaded motor can follow without losing steps. *Unit:* steps/s (revs/min).

Maximum Working Torque: The maximum torque that can be obtained from the motor: *Unit:* Nm.

Overshoot: The maximum amplitude of the oscillation around the final holding position of the rotor after cessation of the switching pulses *Unit:* degrees.

Permanent Overshoot: The number of steps the rotor moves after cessation of the applied switching pulses. *Unit:* steps.

Phase: Each winding connected across the supply voltage.

Pull In Rate (Speed): The maximum switching rate (speed) at which a frictionally loaded motor can start without losing steps. *Unit:* steps/s (revs/min).

Pull In Torque: The maximum switching rate (speed) which a frictionally loaded motor can follow without losing steps. *Unit:* steps/s (revs/min).

Pull Out Torque: The maximum torque that can be applied to a motor spindle when running at the pull out rate. *Unit:* Nm.

Start Range: The range of switching rates within which a motor can start without losing steps.

Step Angle: The nominal angle that the motor spindle must turn through between adjacent steps. *Unit:* degrees.

Stepping Rate: The number of step positions passed by a fixed point on the rotor per second. *Unit:* steps/s.

Slew Range: The range of switching rates within which a motor can run unidirectionally and follow the switching rate (within a certain maximum acceleration) without losing steps, but cannot start, stop or reverse.

CHAPTER 4

Televisions and Monitors

4.1 Power Devices in TV Applications (Including selection guides)

4.2 Deflection Circuit Examples

4.3 SMPS Circuit Examples

4.4 Monitor Deflection and SMPS Example

Power Devices in TV Applications (Including selection guides)

4.1.1 An Introduction To Horizontal Deflection

This report has been divided into three sections

Section 1: This section explains the fundamentals of horizontal deflection. This is done by discussing the operation of a circuit which simulates a practical horizontal deflection circuit. It explains how the circuit produces the characteristic deflection waveforms, and why these waveforms are needed to write the picture information on the screen of a television set.

Section 2: This section is the main body of the report. It explains the processes of east west correction, S correction and linearity correction. In logical stages, it explains how the horizontal deflection circuit is built up.

Section 3: This section shows how the requirements for both of the diodes in the diode modulator follow from the operation of the deflection circuit.

High voltage transistor requirements are explained in the report, "BU2508A, a new deflection transistor".

Section 1 deflection circuit

The horizontal deflection test circuit used to assess Philips deflection transistors and diodes is shown below. Lc represents the horizontal deflection coils.

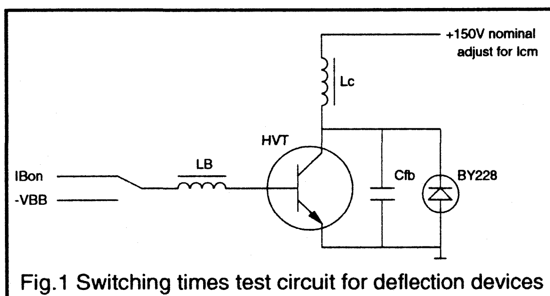


Fig.1 Switching times test circuit for deflection devices

This circuit is a simplification of a practical horizontal deflection circuit. It can be used to produce the voltage and current waveforms seen by both the transistor and the diode in a real horizontal deflection circuit. It is therefore very useful as a test circuit for switching times and power dissipation.

The corresponding waveforms are shown in Fig.2.

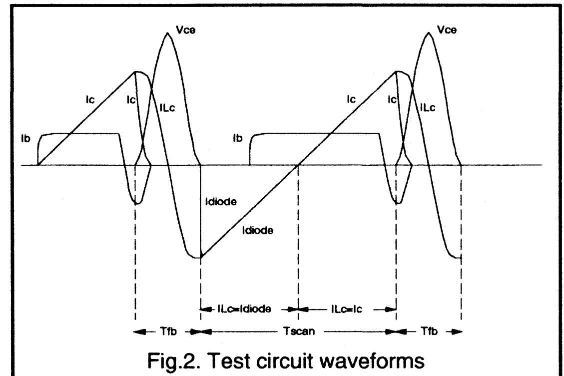


Fig.2. Test circuit waveforms

Briefly going through one cycle of operation, the sequence of events is as follows. (This can be followed through on the waveforms shown in Fig.3, by starting on the left and following the stages numbered 1 to 8).

1. Turn on the high voltage transistor, HVT, by applying a positive current drive to the base. The voltage on the collector is now approximately 0.5 Volts because the device is fully on. This means that the voltage across the coil, Lc, is the full line voltage; in this case 150 Volts.

2. According to the law, V = L * dI/dt, the current in the coil Lc will now start to rise with a gradient given by 150V/Lc. This portion of the coil current (ILc), is the sawtooth portion of the collector current in the transistor (Ic).

3. Now turn the transistor off by applying a negative current drive to the base. Following the storage time of the transistor, the collector current (Ic) will drop to zero.

4. The current in Lc (ILc) is still flowing! This current, typically 4.5 Amps for testing the high voltage transistor BU508A, cannot flow through the transistor anymore, nor can it flow through the reverse biased diode, BY228. It therefore flows into the flyback capacitor, Cfb, and so the capacitor voltage rises as ILc falls. Because Cfb is connected across the transistor, the rise in capacitor voltage is seen as a rise in Vce.

Lc will transfer all its energy to Cfb. The capacitor voltage reaches its peak value, typically 1200 Volts, at the point where ILc crosses zero.

5. Now we have a situation where there is zero energy in Lc but there is a very large voltage across it. So ILc will rise, and since this current is supplied by Cfb, the voltage across Cfb falls. This is of course a resonant LC circuit and essentially it is energy which is flowing, first from the

inductor, Lc, to the capacitor, Cfb, and then from the capacitor, Cfb, to the inductor, Lc. Note that the current in Lc is now flowing in the opposite direction to what it was previously. It is therefore represented as a negative current.

6. This resonance would continue, with the coil current and the capacitor voltage following sinusoidal paths, were it not for the diode, BY228. When the capacitor voltage starts to go negative the diode becomes forward biased and effectively clamps the capacitor voltage to approximately -1.5 Volts. This also clamps the voltage across Lc to approximately the same value as it was when the transistor was conducting, ie the line voltage (150 Volts). Note that the coil current is now being conducted by the diode, and hence ILc = Idiode.

7. So we have again a current ramp in Lc with a dI/dt equal to 150/Lc. This current starts with a value equal to the value it had at the end of the transistor on time (neglecting circuit losses). It is, however, flowing in the opposite (negative) direction and so the positive dI/dt will bring it back towards zero.

8. Before ILc actually reaches zero, we reapply the base drive to the transistor. This means that when ILc does reach zero, we arrive back at the same conditions we had at the beginning of stage 1: The transistor is on, the current in Lc is zero and the voltage across Lc is the line voltage (150 Volts).

Now let us consider how these waveforms are put to practical use in a television.

In a television set, or a computer monitor, the picture information is written onto the screen one line at a time. Each of these horizontal lines of picture information is written onto the screen by scanning the screen from left to right with an electron beam. This electron beam is produced by a gun situated at the back of the tube, and it is accelerated towards the screen by a high potential (typically 25 kV). The beam is deflected from left to right magnetically, by varying the current in a set of horizontal deflection coils positioned between the gun and the screen.

The screen is phosphor coated, and when the high energy electron beam strikes the phosphor coating the phosphor gives off visible light. The density of electrons in the electron beam can be varied: phosphor brightness depends on beam density, and so the instantaneous brightness of the scanning spot can be varied at a fast rate as each line of picture information is written onto the screen. A set of vertical deflection coils deflect the beam vertically at the end of each horizontal scan and so lines of picture information can be built up, one after the other. The vertical deflection frequency (or *field rate*) for UK sets is 50 Hz (alternate line scanning, giving 25 complete screens of information per second). This high fequency ensures that the display is flicker free.

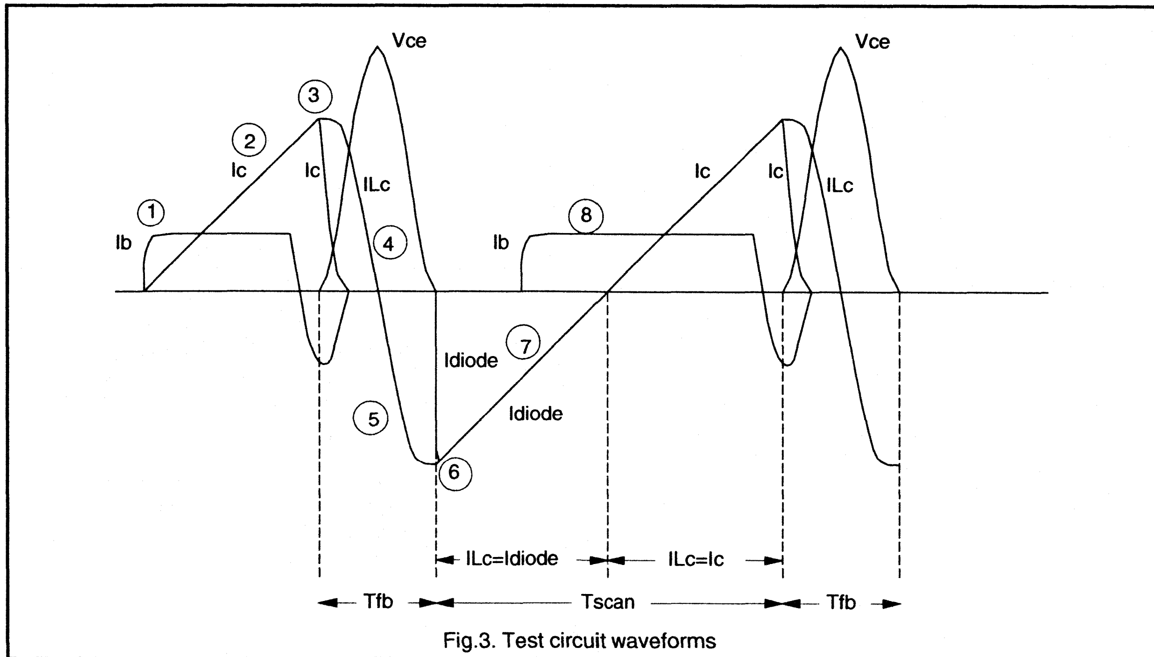


Fig.3. Test circuit waveforms

With no current in the horizontal deflection coils, the magnetic field between them is zero and so the electron beam hits the centre of the screen. With a negative current in the coils, the resultant magnetic field deflects the electron beam to the left side of the screen. With a positive coil current the deflection is to the right.

Now look at the characteristic deflection waveforms. The current ILc represents the current in the horizontal deflection coils. During the period where the current in the deflection coils is ramping linearly from its peak negative value to its peak positive value, the electron beam is scanning the screen from left to right. This is the scan time, Tscan. During the period where the horizontal deflection coil current flows into the flyback capacitor, and then back into the coil (the half cosine curve at the end of the scan period), the electron beam is rapidly moving from the right side of the screen to the left. This is called the flyback period, Tfb, and no information is written onto the screen during this part of the cycle.

Section 2 correction circuits

The simplified deflection circuit shown in Fig.1 can be redrawn as shown in Fig.4. where Lc is the horizontal deflection yoke and Cs is charged to the line voltage (150V).

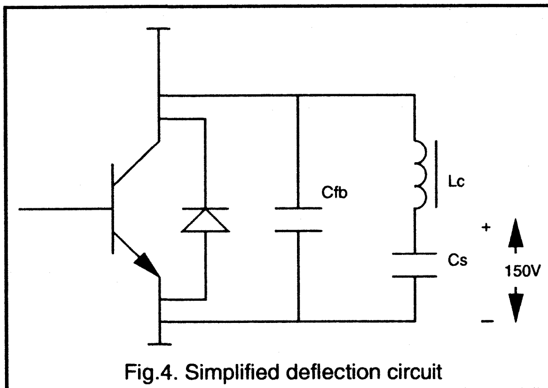


Fig.4. Simplified deflection circuit

The advantage of this arrangement is that, by carefully selecting the value of Cs, one form of picture distortion is corrected for as follows.

The front of the TV tube is flat, rather than curved, and so during each horizontal scan the electron beam travels a greater distance to the edges of the screen than it does to the middle. A linear deflection coil current would tend to over deflect the beam as it travelled towards the edges of the screen. This would result in a set of 'equidistant' lines appearing on the screen as shown in Fig.5.

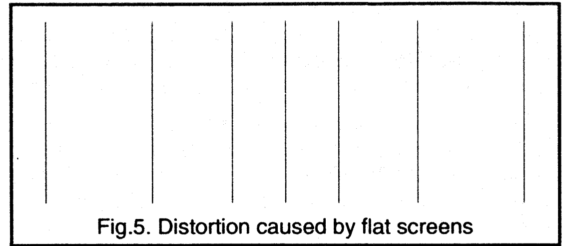


Fig.5. Distortion caused by flat screens

The voltage on the capacitor, Cs, will be modulated by the deflection coil current, ILc. When the diode is in forward conduction and the current in Lc is 'negative', the voltage on Cs will rise as Cs becomes more charged. When the transistor is conducting and the current in Lc is 'positive', the voltage on Cs will drop as Cs discharges. This is shown in Fig.6.

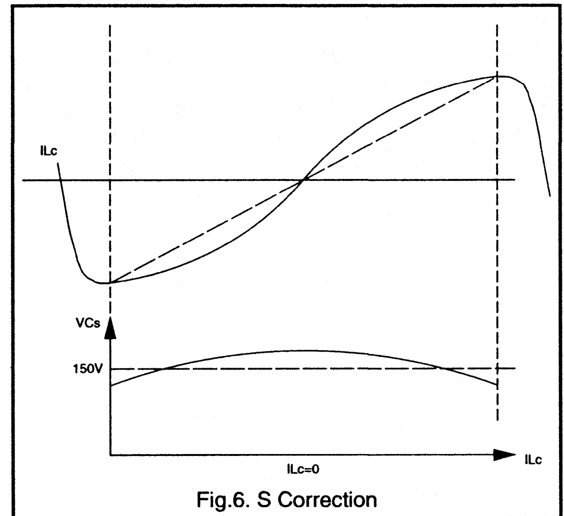


Fig.6. S Correction

This will give an S shape to the current ramp in the deflection coils which corrects for the path difference between the centre and the edge of a flat screen tube. Hence the value of the capacitor, Cs, is quite critical. Cs is known as the S correction capacitor.

However, this is not the only source of picture distortion that must be corrected for. The voltage across the deflection coil is also modulated by the voltage drop across the series resistance of the coil. This is shown in Fig.7.

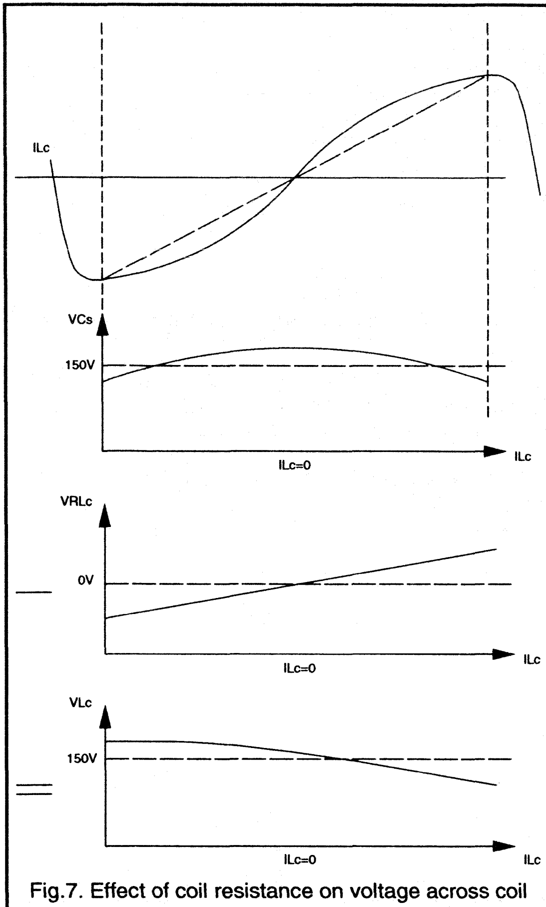


Fig.7. Effect of coil resistance on voltage across coil

VRLc is the voltage drop across the resistive component of Lc. Subtracting this from the voltage across Cs (VCs) gives the voltage across the inductive component on the deflection coils (VLc).

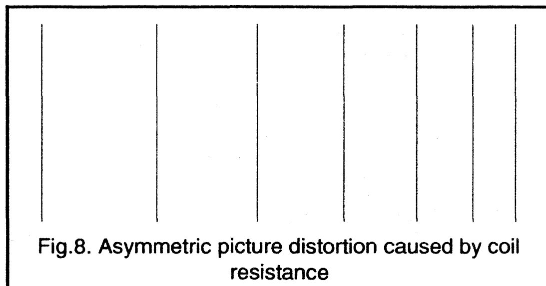


Fig.8. Asymmetric picture distortion caused by coil resistance

This parasitic resistance (RLc) causes an asymmetric picture distortion. A set of 'equidistant' vertical lines would appear on the screen as shown in Fig.8. The voltage across the coils is falling as the beam scans the screen from left to right. The beam therefore travels more slowly towards the right side of the screen and the lines are drawn closer together.

To compensate for the voltage drop across the parasitic coil resistance we need a component with a negative resistance to place in series with the coil. The characteristics of a negative resistance are shown in Fig.9.

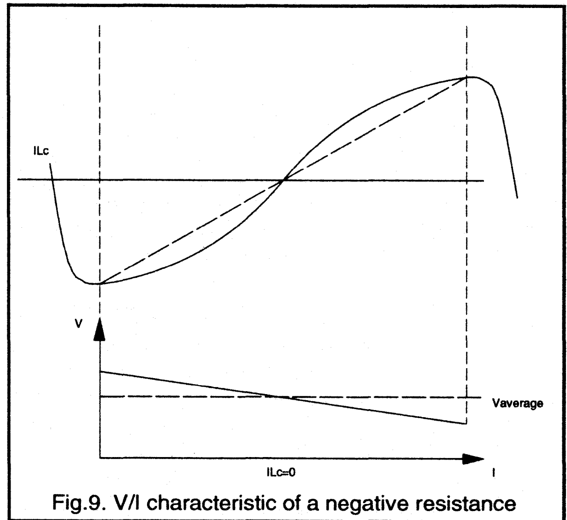


Fig.9. V/I characteristic of a negative resistance

This negative resistor effect is mimicked by using a saturable inductance, Lsat, in series with the deflection coils as shown in Fig.10.

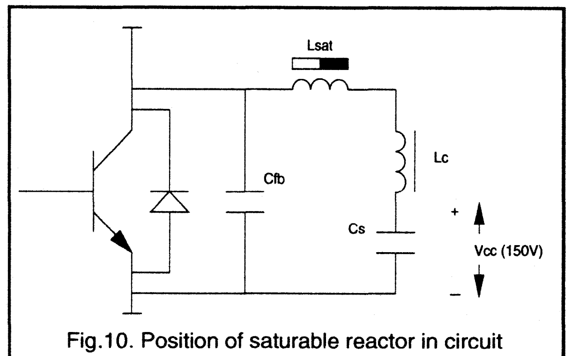


Fig.10. Position of saturable reactor in circuit

This very neat solution works as follows:

For an inductor with a low saturation current , the relationship between inductance and current is as shown in Fig.11. As the current is increased much above zero, the core saturates and so the inductance drops. This happens if the current is conducted in either direction.

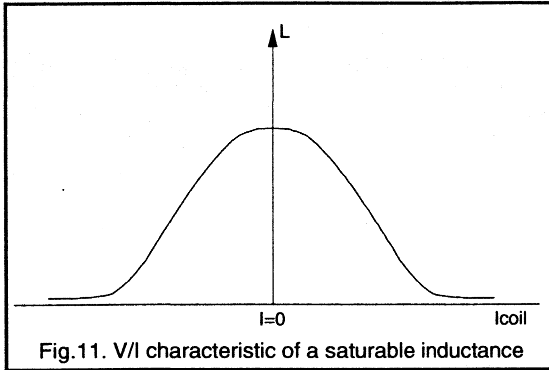


Fig.11. V/I characteristic of a saturable inductance

By taking a saturable inductance and premagnetising the core, we add a DC bias to this characteristic as shown in Fig.12.

Since Lsat has a much lower inductance than Lc, the dI/dt through Lsat is governed by the deflection coils, and is therefore dILc/dt. The voltage drop across Lsat is therefore given by V=Lsat*dILc/dt. During the scan time, Tscan, dILc/dt is approximately constant in value, and so the voltage/current characteristics of Lsat during the scan time are is shown in Fig.13.

This is the characteristic we required (see Fig.9.) and so the voltage developed across Lsat, the linearity correction coil, compensates for the series resistance of the deflection coils.

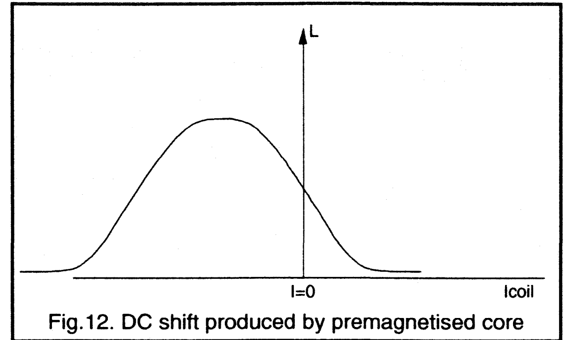


Fig.12. DC shift produced by premagnetised core

So the circuit shown in Fig.10 now gives the desired deflection waveforms. The electron beam scans the screen at a uniform rate on each horizontal scan.

However, the circuit is not lossless and unless Cs is kept topped up Vcc will gradually decay. To prevent this from happening we add a voltage supply as shown in Fig.14.

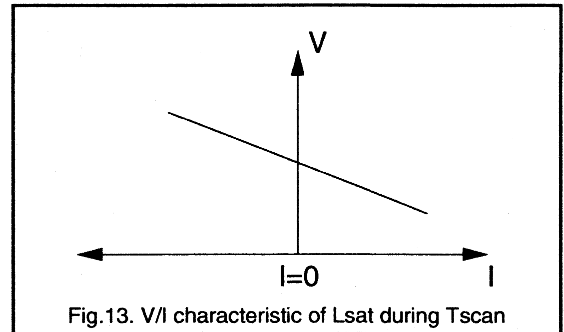


Fig.13. V/I characteristic of Lsat during Tscan

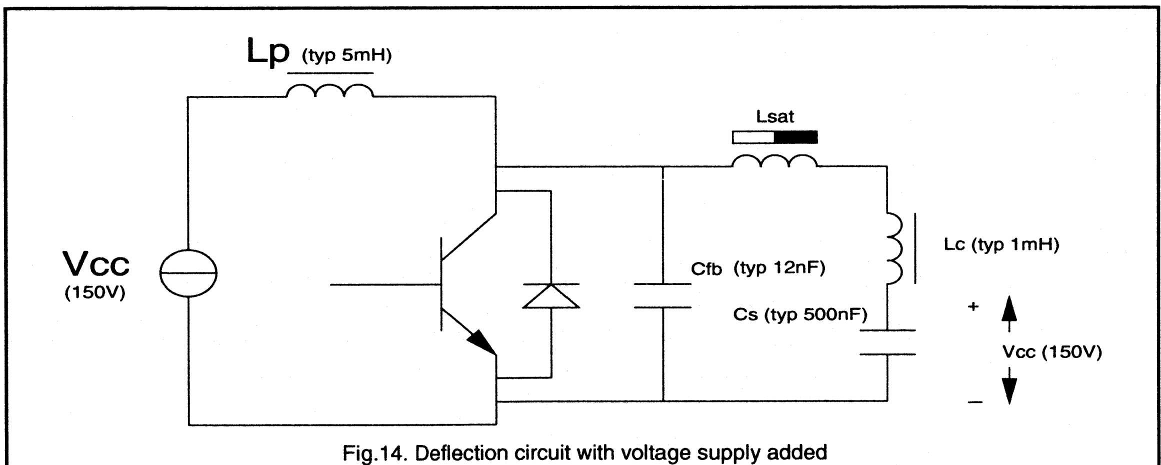


Fig.14. Deflection circuit with voltage supply added

The average voltage across Lc *must* be zero. A DC voltage across Lc would generate a DC current which would correct for the DC voltage by charging or discharging Cs. So Cs is charged to Vcc by the self corrective action of the circuit. Applying Vcc directly to Cs would result in a DC current component through the deflection coils with a consequent picture shift to the right. Applying Vcc to Cs via the deflection coils overcomes this.

The large choke inductance, Lp, in series with the Vcc supply is necessary to prevent an enormous increase in the current through the power switch. Without it the Vcc supply would be shorted out every time the transistor was turned on. Typically the arrangement shown will result in a 20% increase in the current through the power switch and the power diode.

So to recap on the circuit so far: the series resistance of the deflection coils is compensated for by the linearity correction coil, Lsat, and the varying length of the electron beam path, as the beam scans the screen from left to right, is compensated for by the S correction capacitor, Cs. This capacitor modulates the voltage across the deflection coils during each horizontal scan, modulating the magnetic field ramp between them, and thus keeping the speed at which the electron beam scans the screen constant.

However, as the picture information is written onto the screen, by writing one line of information after another, a further variation in the length of the beam path is introduced as the beam scans the screen from top to bottom. The length of the beam path to the edge of the screen is shorter when the central lines of picture information are being written than it is when the lines at the top or the bottom of the screen are being written.

This means that a higher peak magnetic field is required to deflect the beam to the screen edges when the beam is writing the central lines of picture information, than that required to deflect the beam to the screen edges when the lines of picture information at the top and bottom of the screen are being written.

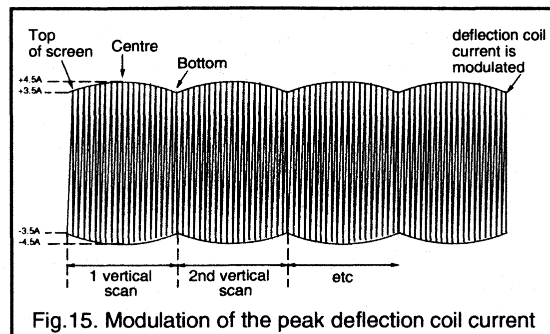


Fig.15. Modulation of the peak deflection coil current

This requires increasing the peak deflection coil current gradually over the first half of each vertical scan, and then reducing it gradually over the later half of each vertical scan (see Fig.15.). This is done by modulating the voltage across the deflection coils. This process is known as 'east west correction'.

The line voltage, Vcc, is supplied by a winding on the SMPS transformer. This voltage is regulated by the SMPS and during the operation of the TV set it is constant.

In order to achieve the required modulation of the voltage across the deflection coils, a simple linear regulator could be added in series with Lp. One disadvantage of this solution is that it increases the circuit losses.

In addition to this problem, there is the problem that the 5mH series inductance is not simply a choke. It is in fact the primary winding of a flyback transformer which has a number of secondary windings including the E.H.T. voltage supply for the tube. This 5mH inductor is in fact the primary winding of the line output transformer.

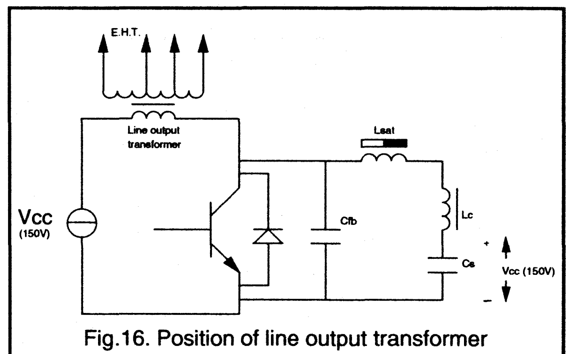


Fig.16. Position of line output transformer

A lot of power can be drawn from the line output transformer without affecting the deflection.

In order to keep the secondary windings of the line output transformer at a fixed voltage, we need to keep the voltage across the primary winding fixed. Therefore a linear regulator in series with Vcc is definitely not allowed.

The solution is to put a dummy deflection circuit in series with the real deflection circuit. This dummy deflection circuit has its own voltage supply, Vmod (see Fig.17.).

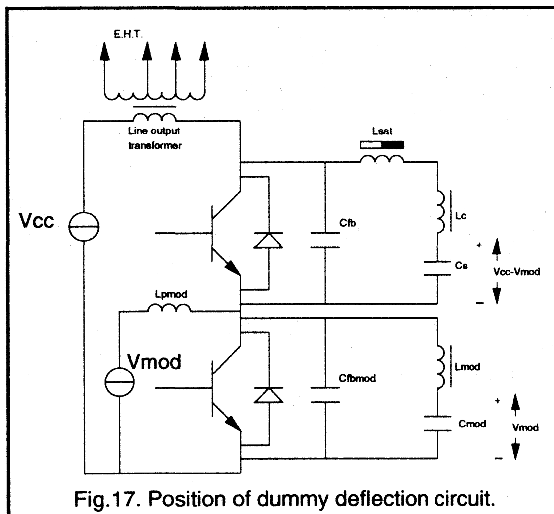


Fig.17. Position of dummy deflection circuit.

The two deflection circuits operate in direct synchronisation. Vmod is a voltage between zero and 30 Volts. Thus we can vary the voltage across the real deflection circuit without varying the voltage across the primary of the line output transformer.

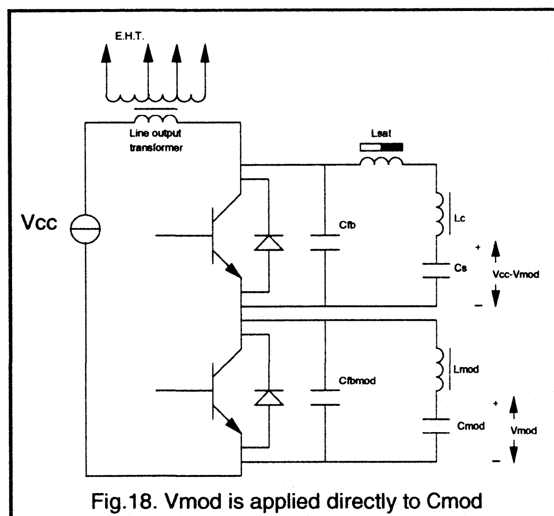


Fig.18. Vmod is applied directly to Cmod

For proper flyback tuning, the upper and lower deflection circuits and the line output transformer must be tuned to the same flyback frequency. The two deflection circuits are tuned through careful selection of the flyback capacitors. In the case of the line output transformer, the capacitance of the windings provides the necessary capacitance (typically 2 nF) for correct tuning.

Since Lmod is only an inductor and not a real deflection component, a net DC current through it is not a problem. Therefore we can apply Vmod directly to Cmod and this way reduce the component count by Lpmod (see Fig.18.).

Lmod is a quarter of the value of Lc. Cfbmod is four times as big as Cfb. Cmod is not critical as long as it is large enough to supply the required energy.

Suppose there is no voltage supplied externally to Cmod. The voltage, Vcc, will split according to the ratio of the impedances of the two circuits. In fact the Vcc will split according to the ratio of the two flyback capacitors, Cfb and Cfbmod, as shown in Fig.19.

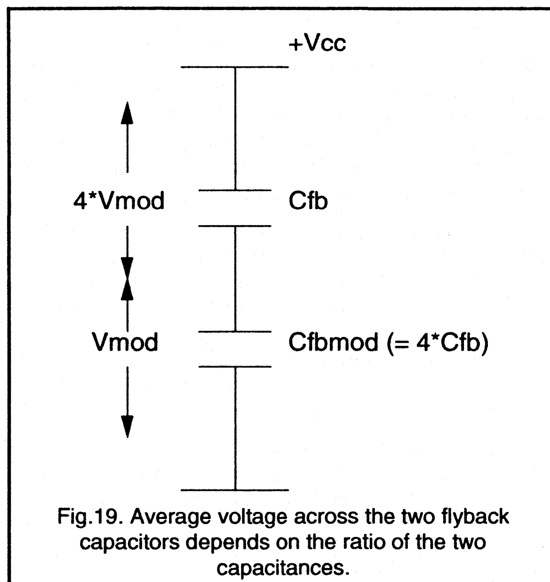


Fig.19. Average voltage across the two flyback capacitors depends on the ratio of the two capacitances.

Therefore the average voltage across Cfbmod will automatically be 30 Volts (for Vcc = 150 Volts) if no external voltages are applied to the dummy circuit. Consequently Cmod will become charged to 30 Volts. The two deflection circuits are always operating in direct synchronisation. Under the condition where Vmod is 30 Volts the currents in the two circuits would also be equal.

The range of Vmod required is 0 Volts to 30 Volts. To reduce the voltage Vmod below 30 Volts we only need to draw current from Cmod. We never need to supply current to Cmod externally. This is the arrangement used in practice.

To sink current from Cmod we just need to add a linear regulator between anode and cathode as shown in Fig.20.

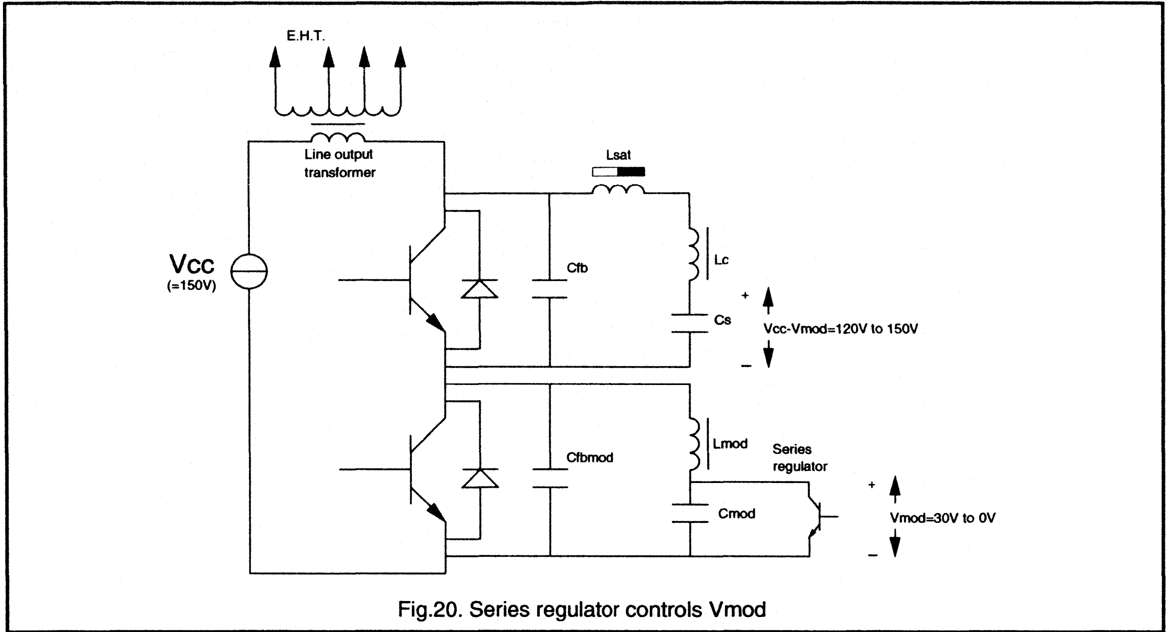


Fig.20. Series regulator controls Vmod

This circuit can be redrawn more tidily as shown in Fig.21

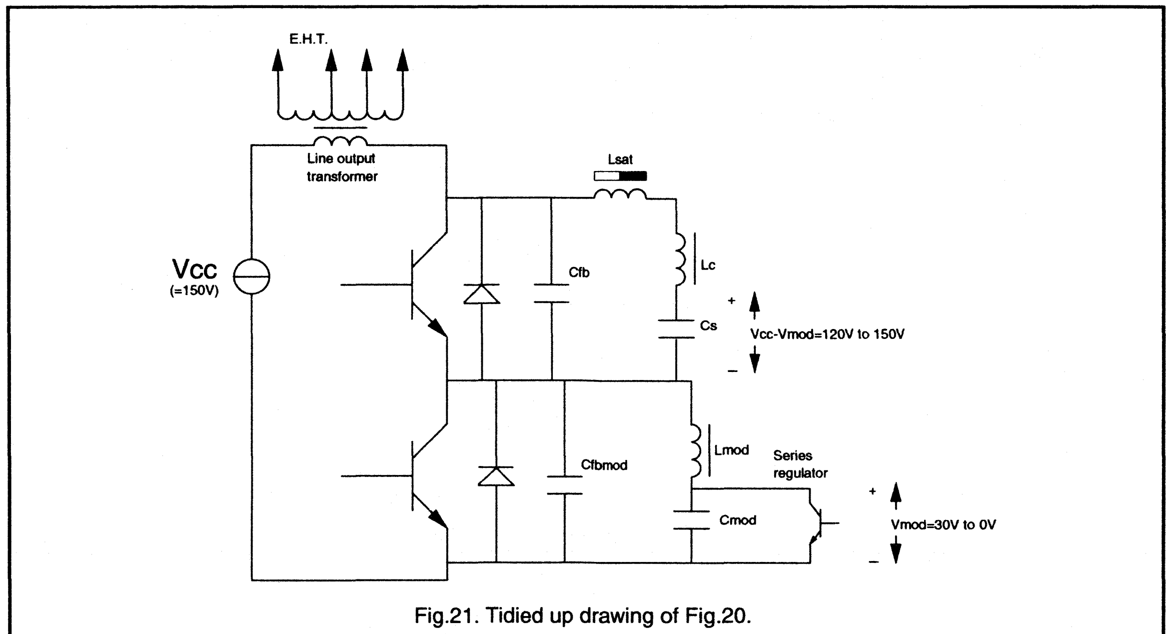


Fig.21. Tidied up drawing of Fig.20.

The two transistors are switching in perfect synchronisation and so this circuit can be replaced by the circuit shown in Fig.22. This arrangement makes no difference to the operation of the circuit.

Fig.22. The diode modulator circuit

In a 16 kHz deflection circuit for a television set, the circuit in Fig.22., known as the diode modulator, might well look like the circuit shown in Fig.23.

Fig.23. The diode modulator for 16 kHz TV deflection

Section 3: diode requirements

This section explains the requirements for both diodes in the diode modulator.

1. Upper diode.

Firstly consider the voltage requirements. In this respect, the worst case conditions for the upper diode are when Vmod = 0 Volts. Under these conditions the upper diode must support the full flyback voltage. Therefore the peak voltage rating on the upper diode must match the BVCES rating of the transistor.

Now consider the current requirements. With no circuit losses, the current in the diode and the transistor are as shown in Fig.24. where Ic is the transistor current and Idiode is the diode current. 80% of this current flows in the deflection coils and 20% flows in the line output transformer primary.

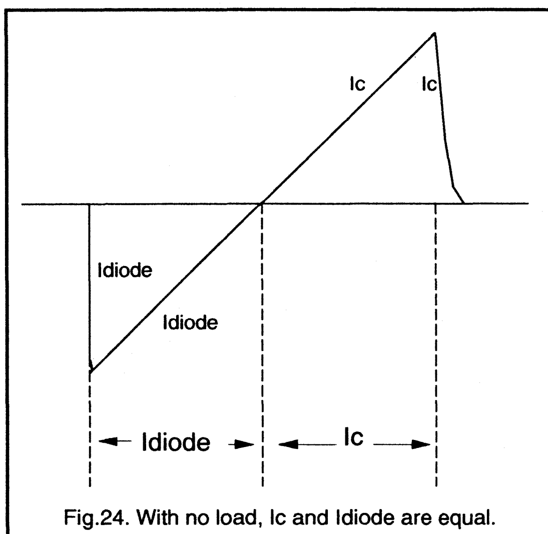


Fig.24. With no load, Ic and Idiode are equal.

With circuit losses included, the transistor current will exceed the diode current. Circuit losses constitute a DC component to the waveform shown in Fig.24. The loading on the line output transformer constitutes a further DC component, increasing the transistor current and reducing the diode current still further. This is shown in Fig.25.

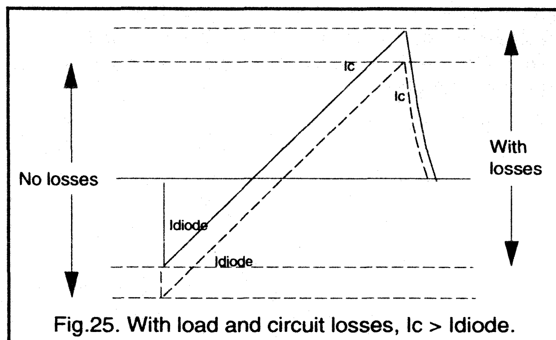


Fig.25. With load and circuit losses, Ic > Idiode.

For example, for a current which is 12 Amps peak to peak, 10 Amps of this is deflection current and 2 Amps of this is line output transformer current. With no load, the peak diode current would be equal to the peak transistor current, ie both would equal 6 Amps. However, the line output transformer requires 1 Amp DC in order to power the secondary windings. This makes the peak diode current 5 Amps and the peak transistor current 7 Amps. These are practical values for a 32 kHz black line (ie EHT = 30 kV) TV set.

NOTE 1: The deflection test circuit shown in Fig.1, at the very beginning of this report, is a worst case test circuit for the top diode.

NOTE 2: The diode must conduct the full current *immediately* after the flyback period. Until the forward voltage of the diode has recovered to less than 5 Volts the horizontal scan cannot commence (the voltage across the deflection coils would be non linear and therefore cause picture distortion). For a 32 kHz set the diode must therefore recover to less than 5 Volts in under 0.5 us.

2. Lower diode.

First consider the voltage requirements. The worst case condition for the top diode is when the flyback voltage is split between the two diodes in the ratio 5:0. The worst case condition for the lower diode is when the flyback voltage is split between the two diodes in the ratio 4:1 (ie when Vmod is its maximum value of 30 Volts). The voltage rating on the lower diode is therefore usually given as one fifth of the rating of the top diode. So if the rating on the transistor is 1500 Volts, the rating on the top diode is 1500 Volts and the rating on the bottom diode is 300 Volts.

However, in circuits which are not protected against peak conditions during flashover, the voltage on the lower diode could exceed the expected peak value, and so up to 600 Volts for the lower diode could be the requirement for these applications.

Now consider the current requirements. The lower diode must take the same current as the horizontal deflection coil (see Fig.26.) and so its current requirement is the same as that of the top diode.

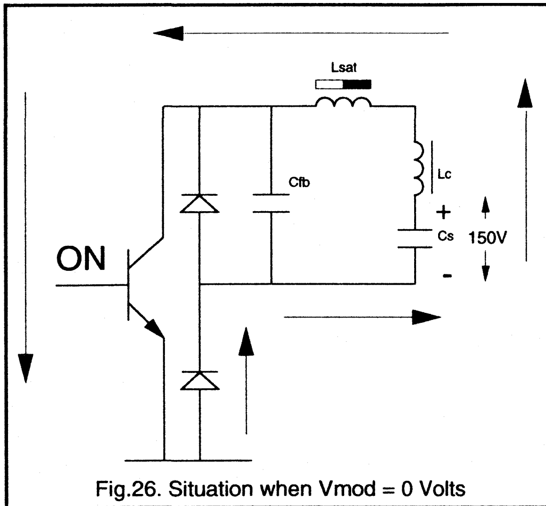


Fig.26. Situation when Vmod = 0 Volts

NOTE 1: As shown in Fig.26., the lower diode is conducting its peak current immediately *before* the flyback period. Therefore the *reverse* recovery of the lower diode must be very fast.

Further reading

An analysis of several diode modulator arrangements is given in Philips Technical Publication 201, "Drive circuits for 45AX", by D.Teuling and T.Zegers.

The requirements for horizontal deflection transistors is explained in the chapter, "BU2508A, a new deflection transistor".

4.1.2 BU2508A, a new deflection transistor

The BU2508A is a significant addition to the family of Philips Components 1500V power bipolar transistors. Without any circuit modifications the BU2508A can replace the S2000A, 2SD1577 and BU508A. The BU2508A also offers the benefits of enhanced performance. Optimised diffusion processes give the BU2508A superior switching performance and increased working gain. More importantly, the BU2508A has exceptional tolerance to variations in base drive and collector current load. Analysis of the entire product spread has shown that this leads to an enormous reduction in the worst case dissipation seen in practical applications.

Main specification points

The maximum voltage, current and power ratings of the BU2508A are identical to those of the BU508A type devices. The improvements made in the BU2508A specification are an increase in the minimum working gain, an increase in the emitter base breakdown voltage, and reduced storage and fall times. However the data sheet in itself does not reflect the area of most significant improvement; namely the much reduced worst case dissipation. Table 1 compares the BU2508A data with that of a standard deflection device.

SYMBOL	BU508A	BU2508A	UNIT
VCES	1500	1500	V
VCEO	700	700	V
ICsat	4.5	4.5	A
hFEsat	2.25	2.7	
VCEsat	1	1	V
BVEBO	6	7.5	V
ts	6.5	5	µs
tf	0.7	0.4	µs
@ ICM	4.5	4.5	A
IB(on)	1.4	1.1	A
PTOTmax	125	125	W

Table 1. BU2508A data compared with BU508A data

Dynamic testing

The key application area for the BU2508A is in the horizontal deflection units of large television sets. Because of this the BU2508A, like all Philips 1500V power bipolar transistors, is assessed in a switching test circuit designed to simulate the most demanding running conditions of a 16 kHz horizontal deflection unit. The horizontal deflection coils, which form the major part of the collector load, are represented in the test circuit by the 1 mH inductance Lc.

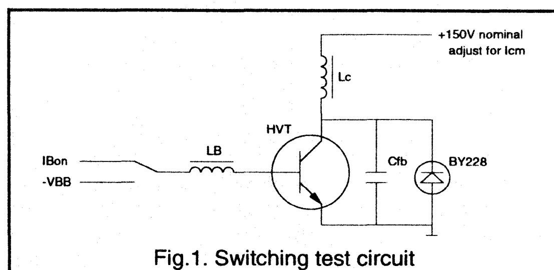


Fig.1. Switching test circuit

This circuit generates the characteristic deflection waveforms from which the storage time, fall time and power dissipation of the device can be measured.

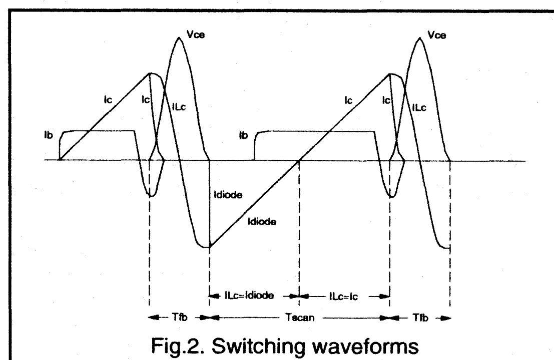


Fig.2. Switching waveforms

Causes of dissipation

Looking at the switching waveforms one can see that during the turn off of the device there is a high collector emitter voltage whilst there is also a high collector current and this results in power dissipation in the device. The turn off portion of the waveforms is shown in more detail in Fig.3. In a deflection circuit it is turn off losses which make up the most significant contribution to overall device losses, turn on and off state losses being negligible whilst on state losses are typically less than 0.5 Watt.

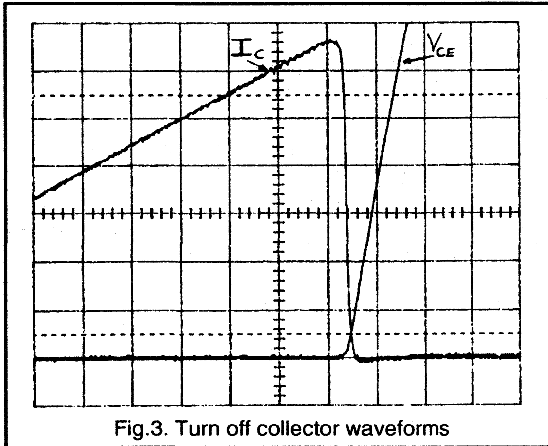


Fig.3. Turn off collector waveforms

Turn off losses for a given device switching a given collector current load are very much drive dependent, optimum drive being that which results in the minimum turn off loss. If the base drive is increased above this optimum value then the overdrive results in the appearance of a collector current tail at turn off. If the base drive is reduced below this optimum value then the underdrive causes the device to come out of saturation prematurely ie when the collector current is at maximum. The effect of both underdrive and overdrive on the device is increased device dissipation and hence increased junction temperature.

'Bathtub' curves

A plot of base current, IB, against turn off dissipation, Eoff, for one BU2508A measured in the switching test circuit at a peak collector current of 4.5 A gives the characteristic bathtub shape shown in Fig.4. From this curve the tolerance to base drive variations can be assessed.

On the far left of the curve, at low I_B values, the device is severely underdriven resulting in a high turn off dissipation. As the base drive is increased the degree of underdrive is reduced and the device remains in saturation for a larger proportion of its on time. This is the reason for the initial decrease in Eoff with increasing I_B seen in the bathtub curve. Eventually the optimum drive is reached and the turn off dissipation, Eoff, is at its minimum value. Increasing the base drive still further results in overdrive and the appearance of a collector current tail at turn off. The result of this, as can be seen in the bathtub curve, is increasing turn off losses with increasing I_B.

However, in a horizontal deflection circuit the collector current is not constant in value. Variations in coil current and hence collector current are necessary to prevent picture distortion. In addition to this in many sets the deflection device is loaded by auxiliary windings, including the EHT, and must therefore supply their varying needs

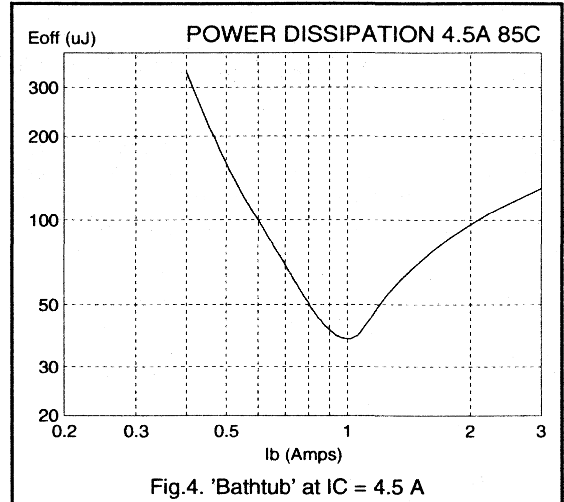


Fig.4. 'Bathtub' at IC = 4.5 A

also. For this reason the dissipation for the same range of I_B values is assessed for collector currents of 3.5 A and 4.5 A (see Fig.5). The worst case dissipation under either collector current load is the important parameter as this represents the worst dissipation that would occur with a given base drive for a collector current varying in value between 3.5 A and 4.5 A.

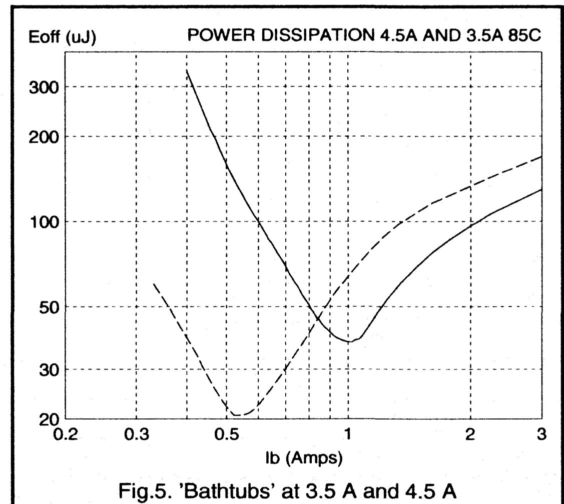


Fig.5. 'Bathtubs' at 3.5 A and 4.5 A

This represents the dissipation performance for one device. The real measure of performance is to take the worst case dissipation for the expected product spread for collector current values of 3.5 A and 4.5 A. This will in fact be the worst case underdrive seen at 4.5 A and the worst case overdrive seen at 3.5 A.

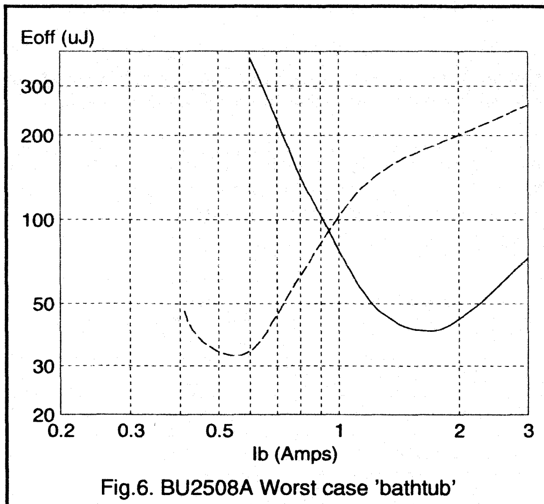


Fig.6. BU2508A Worst case 'bathtub'

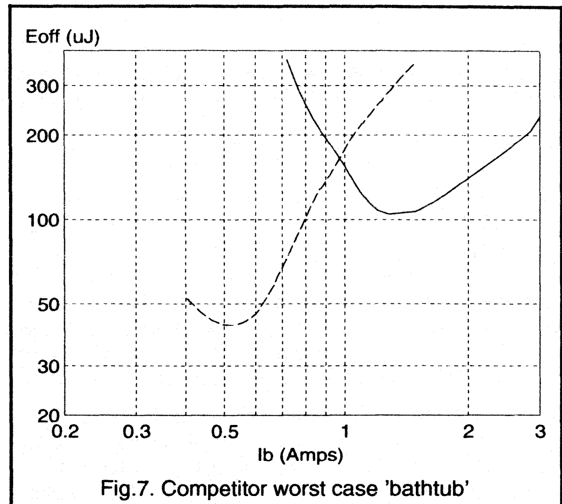


Fig.7. Competitor worst case 'bathtub'

The curve shown in Fig.6 shows the real tolerance of the BU2508A to base drive and collector current load variations because it shows the worst case dissipation of the device for a range of I_B values, and a collector current of between 3.5 A and 4.5 A, taking the entire product spread into account. This worst case performance was compared with that of our major competitors. The best competitor performance seen was that indicated in Fig.7, clearly inferior to the BU2508A.

Practical analysis in television receivers confirmed that the BU2508A had a lower worst case dissipation.

Conclusions

The BU2508A is a direct plug in replacement for the S2000A, 2SD1577 and BU508A requiring no circuit modifications in order to obtain the benefits of enhanced performance. This has been achieved through optimisation of diffusion processes which give the BU2508A exceptional tolerance to base drive and collector current load variations over the entire product spread. This results in a much reduced worse case dissipation in practical applications. Reduced dissipation, improved switching and increased minimum working gain also enable the BU2508A to access more demanding applications requiring a 1500 V capability.

4.1.3 Philips high voltage transistors for television applications

This section is divided into two sections

Section 1: This section deals with choosing the optimum transistor for the SMPS of the television. The relevant MOSFETs and high voltage transistors are reviewed, selection procedures are suggested and finally a selection table with suitable devices for various throughput powers is given. More information on designing power supplies with high voltage transistors is given in the report, "The power supply designers guide to high voltage transistors".

Section 2: This section deals with choosing the optimum transistor for the horizontal deflection stage of the television. To begin with the device requirements are considered. Following this the relevant high voltage transistors for 16 kHz and 32 kHz systems are reviewed and their capabilities discussed. This section also gives an introduction to the new high current 32 kHz deflection transistors BU2520 and BU2525, designed to meet the requirements of todays new developments in large screen colour television.

Section 1: transistors for TV SMPS

The vast majority of television switch mode power supplies are required to generate a 150 Volt supply for the line deflection stage, together with a number of lower voltage outputs for audio, small signal etc. By far the easiest and most cost effective way of fulfilling these requirements is to use a flyback topology. Discontinuous mode operation is generally preferred because it offers easier control and smaller transformer sizes than continuous mode.

The peak voltage across the switching transistor in a flyback converter is twice the peak DC link voltage *plus* an overshoot voltage which is dependant on the transformer leakage inductance and the snubber capacitance. Thus for a given mains input voltage there is a minimum voltage requirement on the transistor. Increasing the transformer leakage and/or reducing the snubber capacitance will increase the minimum voltage requirement on the transistor.

a) Power MOSFETs

110/120 Volt mains applications therefore require a voltage rating of 400 Volts. For these applications the power MOSFET is now used almost exclusively, and it is gaining popularity as the switching device for 220/240 Volt mains applications where an 800 Volt device is generally required, although some users have found that they can accept a 600 Volt device by designing their supplies for minimum drain source voltage.

Philips have a very comprehensive range of power MOSFET devices. The main parameters of the MOSFET devices most applicable to TV SMPS applications are summarised in Table 1.

Part Number	BV_{DSS}	R_{DSON}	@ I_D
BUK454-400B	400 V	1.8 Ω	1.5 A
BUK455-400B	400 V	1.0 Ω	2.5 A
BUK437-400B	400 V	0.5 Ω	6.5 A
BUK454-800A	800 V	6.0 Ω	1.0 A
BUK456-800A	800 V	3.0 Ω	1.5 A
BUK438-800B	800 V	2.0 Ω	4.0 A
BUK438-800A	800 V	1.5 Ω	4.0 A

Table 1. The main Philips PowerMOS transistors for TV SMPS applications

The BV_{DSS} value is the maximum voltage rating of the MOSFET.
The R_{DSON} value is the maximum on resistance of the MOSFET at the specified drain current, I_D.

b) Bipolar transistors

220/240 Volt mains driven flyback converters generally use 1000 Volt bipolar transistors. The BUX85, BUT11A, BUT18A, BUT12A and BUW13A are ideal for these applications. The full voltage capability of the transistor can be used as the limit under worst case conditions but it must never be exceeded. In circuits where the transformer leakage inductance is high, and voltages in excess of 1000 Volts can occur, a device with a higher voltage rating is required. The BU903 and BU603 have a peak voltage rating of 1350 Volts and are ideal for these applications.

The $V_{CESMmax}$ value is the maximum voltage rating of the transistor when the base contact is at a potential lower than or equal to the potential at the emitter contact.
The V_{CEOmax} value is the maximum voltage rating of the transistor when the base contact is at a higher potential than the emitter contact.
The h_{fesat} value is the minimum high current gain of the transistor, measured at the specified collector current I_{Csat}.
The V_{CEsat} value is the maximum collector emitter saturation voltage of the transistor, measured at a collector current of I_{Csat} and a base current of I_{Csat}/h_{fesat}.

The main parameters of these devices are summarised in Table 2.

Part Number	$V_{CESMmax}$	V_{CEOmax}	I_{Csat}	h_{fesat}	V_{CEsat}
BUX85	1000 V	450 V	1 A	5	1.0 V
BUT11A	1000 V	450 V	2.5 A	5	1.5 V
BUT18A	1000 V	450 V	4 A	5	1.5 V
BUT12A	1000 V	450 V	5 A	5	1.5 V
BUW13A	1000 V	450 V	8 A	5	1.5 V
BU603	1350 V	550 V	2 A	6	2 V
BU903	1350 V	550 V	3.2 A	6	2 V

Table 2. The main Philips HVTs for TV SMPS applications

c) Selection procedures

The first requirement to be met is that the peak voltage and current values are within the ratings of the device. For a flyback converter the peak voltage and current values experienced by the power switch are given by the equations in table 3.

Peak voltage across the device	$(2 \times V_{s(max)}) + \sigma$
Peak device current	$2 \times \frac{P_{th}}{\delta_m \times V_{s(min)}}$

Table 3. Peak voltage and current a in flyback converter.

where:

$V_{s(max)}$ = maximum dc link voltage
σ = voltage overshoot due to transformer leakage
$V_{s(min)}$ = minimum dc link voltage
P_{th} = throughput power of SMPS
δ_m = maximum duty cycle of SMPS

MOSFET or bipolar?

The main factors influencing this decision are ease of drive and cost, given the limitation on percentage of throughput power which can be dissipated in the power switch. MOSFETs require lower drive energy and less complicated drive circuitry. They also have negligible switching losses (below 50 kHz). However, large chip sizes are required in order to keep on state losses low (especially as breakdown voltage is increased). Thus the larger chip size of the MOSFET is traded off against its capacity for cheaper and easier drive circuitry and higher switching frequencies.

For 110/120 Volt mains driven TV power supplies the 400 Volt MOSFET dominates. At 220/240 Volts the bipolar transistor dominates although the 800 Volt MOSFET is gaining popularity.

Which MOSFET?

The optimum MOSFET for a given circuit can be chosen on the basis that the device dissipation must not exceed a certain percentage of throughput power. Using this as a selection criterion, and assuming negligible switching losses, the maximum throughput power which a given MOSFET is capable of switching is calculated using the equation;

$$P_{th(max)} = \frac{3 \times \tau \times V_{s(min)}^2 \times \delta_{max}}{4 \times R_{ds(125C)}}$$

where:

$P_{th(max)}$ = maximum throughput power
δ_{max} = maximum duty cycle
τ = required transistor loss (expressed as a fraction of $P_{th(max)}$)
$R_{ds(125C)}$ = R_{dson} at 125˚C
$V_{s(min)}$ = minimum dc link voltage

A transistor loss which is 5 % of throughput power gives a good compromise between device cost, circuit efficiency and heatsink size (ie $\tau = 0.05$)

Note that the R_{dson} value to be used in the calculation is the R_{dson} at 125˚C (a practical value for junction temperature during normal running). The R_{dson} specified in the device data is measured at 25˚C. As junction temperature is increased the R_{dson} increases, increasing the on state losses of the MOSFET. This is shown in Fig 1.

For 400 Volt MOSFETs $R_{ds(125C)} = 1.98 \times R_{ds(25C)}$, where $R_{ds(25C)}$ is the R_{dson} value given in device data.

For 800 Volt MOSFETs $R_{ds(125C)} = 2.11 \times R_{ds(25C)}$.

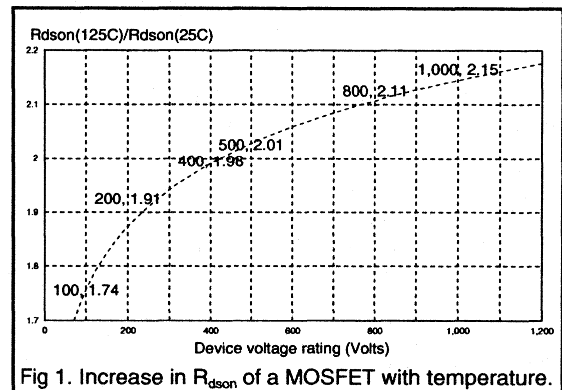


Fig 1. Increase in R_{dson} of a MOSFET with temperature.

Which bipolar?

For maximum utilisation of a bipolar transistor it should be run up to its I_{Csat}. This gives a good compromise between cost, drive requirements and switching losses. Using this as a selection criterion the maximum throughput power which a given bipolar transistor is capable of switching is calculated using the equation;

$$P_{th(max)} = \delta_{max} \times V_{s(min)} \times \frac{I_{Csat}}{2}$$

where: $P_{th(max)}$ = maximum throughput power
δ_{max} = maximum duty cycle
$V_{s(min)}$ = minimum dc link voltage
I_{Csat} = I_{Csat} in transistor data

d) Selection table

Using the selection procedures just discussed, and the device data given in this report, the following selection table of suitable devices for flyback converters of various throughput powers has been constructed.

	Mains input	
Throughput Power	**110/120 Volts (ac)**	**220/240 Volts (ac)**
50 W	BUK454-400B	BUK454-800A BUX85
100 W	BUK455-400B	BUK456-800A BUT11A/BU603
120 W	BUK437-400B	BUK438-800B BUT11A
150 W	BUK437-400B	BUK438-800B BUT18A/BU903
200 W	BUK437-400B	BUK438-800A BUT12A/BUW13A

Section 2: transistors for tv horizontal deflection

In a standard (ie C.R.T.) television system, picture information is written onto the screen by scanning the screen with an electron beam. Horizontal and vertical deflection of this beam is achieved by varying the magnetic field between two separate sets of deflection coils positioned between the electron gun and the screen.

The various broadcasting standards which currently exist use a horizontal deflection frequency of around 16 kHz. High definition television (H.D.T.V.) will make use of higher horizontal deflection frequencies in order to improve picture resolution. These systems propose to use a horizontal deflection frequency of around 32 kHz.

The vertical deflection is much lower in frequency (50 or 60 Hz) and will not be discussed as this uses lower power devices (typically 150 V / 0.5 A).

a) Voltage and current requirements

For a given scan frequency and deflection angle, the voltage and current requirements of the horizontal deflection transistor are not fixed. However, the suitable transistors are all linked by the relationship;

$$I_{Csat} \times V_{CESMmax} = constant$$

The derivation of this law is as follows:

The horizontal deflection angle covered in a given time is proportional to the magnetic field sweep between the horizontal deflection coils. This is in turn proportional to the product of the number of turns on the deflection coils and the peak to peak current. The average current in the deflection coils is zero and hence the peak positive current in the coils is half the peak to peak current. These relationships yield the following equation;

$$B \propto n \times I$$

where:

B = magnetic field sweep between the horizontal deflection coils
n = number of turns on the horizontal deflection coils
I = peak positive current in the horizontal deflection coils

The inductance of the horizontal deflection coils, L, is proportional to the square of the number of turns, ie

$$L \propto n^2$$

Combining these two equations gives

$$B^2 \propto L \times I^2$$

and so for a given deflection angle and horizontal scan frequency, and therefore a given B, L x I^2 is a constant.

For a given deflection frequency the flyback time is also fixed. Flyback time is related to the deflection coil inductance, L, and the flyback capacitance, C, by the equation

$$t_{fb} \propto \sqrt{L \times C}$$

Therefore L x C is a constant.

During the flyback period the energy in the deflection coils ($0.5LI^2$) is transferred to the flyback capacitor and so the voltage across the flyback capacitor rises. Assuming energy is conserved during this transfer, the increase in voltage across the flyback capacitor, δV, is given by

$$\frac{1}{2}\times L\times I^2=\frac{1}{2}\times C\times \delta V^2$$

So, if LI^2 is a constant then $C\delta V^2$ is a constant also. Therefore $LC(I\delta V)^2$ is a constant.

Since L x C is a constant we now have the relationship

$$\delta V\times I=constant$$

δV is the voltage rise across the flyback capacitor due to the energy transferred from the deflection coils during the flyback period. The peak voltage across the flyback capacitor, V_{peak}, is given by

$$V_{peak}=\delta V+V_{CC}$$

where: V_{CC} = line voltage (typically +150 V)

The flyback capacitor is positioned across the collector emitter of the horizontal deflection transistor. Therefore the peak voltage across the flyback capacitor is also the peak voltage across the collector emitter of the deflection transistor.

In order to protect the transistor against overload conditions (eg flashover) a good design practice is to allow V_{peak} to be 80% of the $V_{CESMmax}$ rating of the device. V_{CC} is generally around 10% of the $V_{CESMmax}$ rating of the transistor (in order to obtain the correct ratio of scan time to flyback time). This gives

$$V_{CESMmax}=1.4\times\delta V$$

The positive current in the horizontal deflection coils is conducted by the horizontal deflection transistor. However this is not the peak current in the transistor. The transistor is normally also required to conduct the current in the primary of the line output transformer. Typically this will increase the peak current in the deflection transistor by 40%. For optimum deflection circuit design the peak current in the transistor will be its I_{Csat} rating, ie

$$I_{Csat}=1.4\times I$$

Therefore for a given deflection angle and a given horizontal scan frequency the horizontal deflection circuit can be designed around any one of a number of devices. However the suitable devices are all linked by the equation

$$I_{Csat}\times V_{CESMmax}=constant$$

Summary

For a given horizontal deflection angle and a given horizontal scan frequency

$$V_{CESMmax}=1.4\times\delta V$$

$$I_{Csat}=1.4\times I$$

$$I_{Csat}\times V_{CESMmax}=constant$$

$$L\times I^2=C\times\delta V^2=constant$$

where:

$V_{CESMmax}$ = maximum voltage rating of the horizontal deflection transistor
I_{Csat} = I_{Csat} rating of the horizontal deflection transistor
δV = voltage rise on the flyback capacitor due to the energy transfer from the horizontal deflection coils
I = peak positive current in the horizontal deflection coils
L = inductance of the horizontal deflection coils
C = value of flyback capacitance

This assumes a peak forward current in the line output transformer which is 40% of the peak positive current in the horizontal deflection coils, a line voltage which is 10% of the $V_{CESMmax}$ rating of the horizontal deflection transistor, a peak voltage across the horizontal deflection transistor during normal running which is 80% of its maximum rating and a peak current in the horizontal deflection transistor during normal running which is equal to its I_{Csat} rating.

b) Switching and dissipation requirements

For a given deflection frequency the minimum on time of the transistor is well defined. For 16 kHz systems the transistor on time is not less than 26 µs and for 32 kHz systems it is not less than 13 µs. This enables the required storage time of the transistor to be well defined also. For 16 kHz systems a maximum storage time of 6.5 µs is the typical requirement. For 32 kHz systems the required maximum storage time is typically 4.0 µs. For higher frequencies the required maximum storage time is reduced still further.

Storage time in the circuit can always be reduced by turning the transistor off harder. However this eventually leads to a collector current tail at turn off and as a consequence the turn off dissipation increases. Turn off dissipation accounts for the bulk of the losses in a deflection transistor and it is crucial that this is kept to a minimum. The deflection transistor must be tolerant to drive and load variations if it is to achieve a low turn off dissipation because the east west correction on larger screen television sets means that circuit conditions are not constant. Turn off can be optimised during the design phase by ensuring that the peak reverse base current is roughly half of the peak collector current and the negative base drive voltage is between 2 and 5 volts.

Turn on performance is not a critical issue in deflection circuits. At turn on of the deflection transistor the collector current is low, the collector voltage is low and therefore the dissipation is low. The actual turn on performance of the transistor has a negligible effect.

c) Transistors for horizontal deflection circuits

The deflection circuit must satisfy any specified cost, efficiency and EMC requirements before it can be called acceptable. A very high voltage deflection transistor would allow a lower deflection coil current to be used, reducing the level of EM radiation from the deflection coils, but it would require a higher line voltage and it would also result in higher switching losses in the transistor. A very high deflection coil current would allow a lower voltage deflection transistor to be used and a lower line voltage. This would also yield lower switching losses in the deflection transistor. However high currents in the deflection coils could lead to EMC problems, and the need to keep the resistive losses in the coils low would mean that thicker wire would have to be used for the windings. Above a certain point the skin depth effect makes it necessary to use litz wire.

For 16 kHz and 32 kHz applications the 1500 Volt bipolar transistor has become the designers first choice. Many 16 kHz systems could work well using 1000 Volt devices. This would also mean using a lower deflection coil inductance and a lower line voltage. However, it would appear that 1500 Volts has been adopted as the 'standard', certainly up to 32 kHz. The collector currents involved range from 2 Amps peak to 8 Amps peak, depending on the deflection angle, the EHT energy and the horizontal scan frequency. The transistors for 16 kHz and 32 kHz applications are now considered.

16 kHz applications

Table 4 gives the 1500 Volt transistors for 16 kHz television deflection systems and a summary of their main characteristics.

Part Number	$V_{CESMmax}$	I_{Csat}	Main Application
BU505	1500V	2A	Monochrome sets
BU506	1500V	3A	90° Colour sets (up to 21")
BU508A	1500V	4.5A	110° Colour sets (above 21")
BU2508A	1500V	4.5A	110° Colour sets
BU2520A	1500V	6A	110° Colour sets

Table 4. Transistors for 16 kHz TV deflection

All of the above types are available in isolated encapsulations (F pack), removing the need for a mica spacer to be used between device and heatsink. They are also all available as D types ie with a built in damper diode.

The BU2508A family is a recent addition to the range of Philips deflection transistors. Far from being just another 1500 Volt transistor, the BU2508A has been specifically designed for horizontal deflection. Through targeting the device for this very specialised application it has been possible to achieve a dissipation performance in deflection circuits which is exceptional. More details are given in the report, "BU2508A, a new transistor for horizontal deflection".

The BU2520A family uses the superior technology of the BU2508A family but applies it to a larger chip area. The BU2508A family has a gain of 5 at 5 Volts V_{CE} and 4 Amps I_C. The BU2520A family has a gain of 5 at 5 Volts V_{CE} and 6 Amps I_C. This gives designers working on large colour television sets a high gain deflection transistor with a high current capability. The high gain reduces the forward base drive energy requirements. The high current capability enables the energy which is drawn from the line output transformer to be increased. Using one of the BU2520A family therefore allows the EHT energy to be increased for brighter pictures (a feature of new 'black line' tubes) without having to increase the forward base drive energy to the deflection transistor.

32 kHz applications

Table 5 gives the 1500 Volt transistors for 32 kHz deflection systems and a summary of their main characteristics.

Part Number	$V_{CESMmax}$	I_{Csat}	Main Application
BU2508A	1500V	4A	Monochrome
BU2520A	1500V	6A	90° Colour sets
BU2525A	1500V	8A	110° Colour sets

Table 5. Transistors for 32 kHz deflection

Whilst 32 kHz monochrome televisions are unlikely to materialise, even in the distant future, monochrome VGA monitors running at 31.5 kHz up to 48 kHz ('super VGA') are very common and the BU2508A is an excellent choice for these applications.

The immediate demand is for large screen, ie 110° deflection angle, colour sets. Top of the range 32 kHz models will have 16 x 9 aspect ratio tubes and increased EHT voltage for brighter pictures, from 25 kV up to 30 kV. The BU2525A with its 8 Amps capability (at $V_{CE} \leq 5V$ and I_B = 1.6 Amps) has been designed to meet the needs of these applications. In addition to this very impressive electrical specification, the BU2525A offers the advantage of being available in a standard SOT199 encapsulation.

Deflection Circuit Examples

4.2.1 Application information for the 16 kHz black line picture tube A66EAK022X11 and A59EAK022X11

With the introduction of the black line picture tubes new drive circuits are required. To have full benefits, the EHT voltage and beam current must be increased. This report describes the horizontal deflection and EHT generation. Some hints for vertical deflection and video amplifiers are given as well.

Summary

This report describes the horizontal deflection circuitry of the black line picture tube A66EAK022X11 and A59EAK022X11. To take full advantage of this new tube it must be driven at 27.5kV @ 1.3mA. This implies that in an ordinary combined EHT and deflection stage in the not loaded condition the high voltage increases to about 29.5kV. The main change to this circuit compared with existing circuits is the line output transformer (AT2077/34) uses four layer DSB technology.
For the vertical deflection a minor modification on PCALE report ETV8831 is given.
The video output stage suited to this tube is described in PCALE report ETV8811.

1. Introduction

One step in improving picture quality is the introduction of the black line picture tube. With this tube daytime TV viewing with a bright high contrast picture becomes possible. To achieve this the picture tube is provided with a dark screen and increased EHT power capability by means of an invar shadow mask.

When the 45AX black line picture tube is compared with the existing 45AX tubes the following modifications in the application must be made.

-Increase of the EHT power to 27.5kV @ 1.8mA beam current.

-Increase of the cut off voltage to 160V.

To cope with this high EHT power demand, a new line output transformer has been developed (AT2077/34). The main part of this report is dedicated to the horizontal deflection. For supply, vertical deflection and video amplifier details reference will be made to other reports.

Special care is taken to suppress certain geometrical picture distortions which otherwise would become noticeable at the increased levels of dynamic EHT load variations. Those distortions are the result of oscillations in the line output stage.

All measurements and circuits are based and tested on the 66FS picture tube. Since the 59FS tube is electrically identical to the 66FS tube this circuit is also suited for the 59FS picture tube. With some minor circuit modifications (component values) this circuit is also suited for 33" picture tubes.

2. Circuit description

The horizontal deflection board is built up of four major parts, see Fig.2.1.

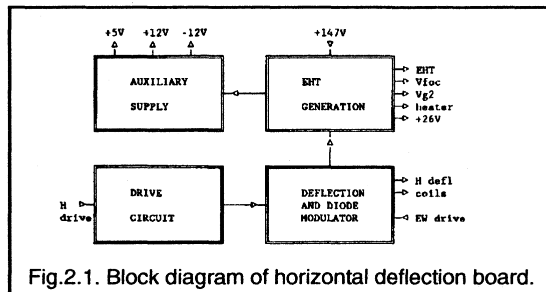


Fig.2.1. Block diagram of horizontal deflection board.

In high end TV sets a lot of low voltage supply current is required. In this design a separate transformer in parallel to the line output transformer is foreseen for the generation of these auxiliary supplies. In applications where this auxiliary power is not required this part can be omitted by simply leaving out the additional transformer. The other parts of this horizontal deflection are more or less classic.

2.1 Drive circuit

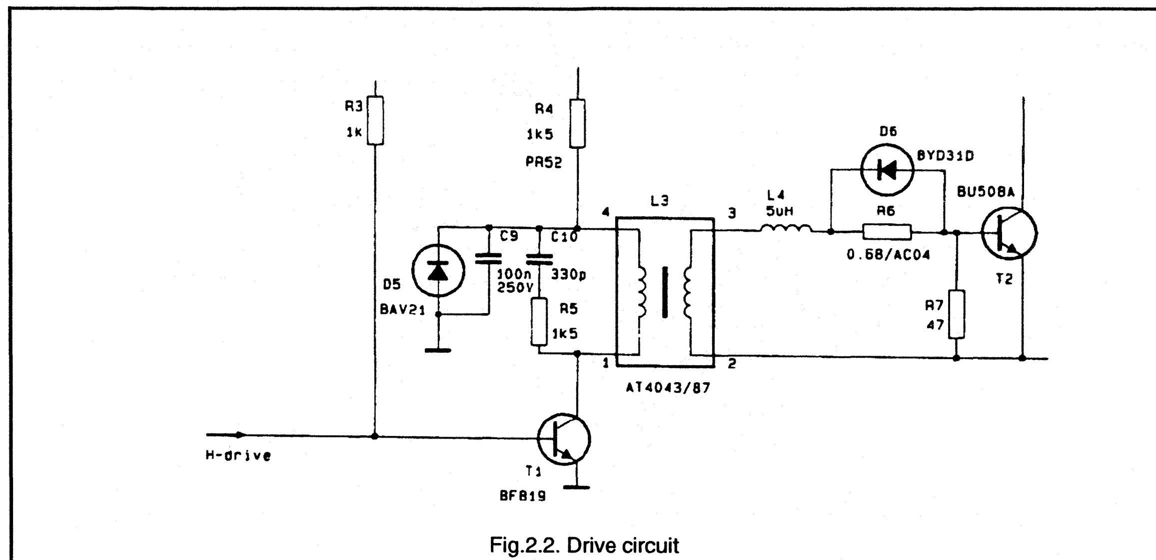


Fig.2.2. Drive circuit

The horizontal drive circuit is a classical transformer coupled inverting driver stage. When driver transistor T1 is conducting energy is stored in the transformer. When T1 is turned off the magnetising current continues to flow in the secondary side of the transformer thus turning on the deflection transistor. At this time the voltage on the secondary side of the driver transformer is positive (V_{BE}+I_BxR6). When the driver transistor turns on again this secondary voltage reverses and will start to turn off the deflection transistor. At the same time energy is stored in the transformer again.

During this turn off action the forward base drive current decreases with a controlled dI/dt, thereby removing the stored charge from deflection transistor. The dI/dt depends on the negative secondary voltage and the leakage inductance. As a rule of thumb, the deflection transistor stops conducting when its negative base current is about half the collector peak current.

To prevent the deflection transistor from turning on during flyback due to parasitic ringing on the secondary side of the driver transformer a damper resistor is connected in parallel with the base emitter junction of the deflection transistor.

Also at the primary side of the driver transformer a damper network is added (R5 & C10) to limit the peak voltage on the driver transistor.

D5 is added for those applications where in the standby mode the deflection stage is turned off by means of continuous conduction of the driver transistor. The explanation is as follows:

When T1 is suddenly made to conduct continuously, a low frequency oscillation will occur in C9 and the primary of L3. As soon as the voltage at pin 4 of L3 becomes negative T2 starts conducting until the driver transformer is demagnetised. This will cause an extremely high collector current surge. D5 prevents pin 4 of L3 going negative and so this fault condition is avoided. For those applications where this condition cannot occur, D5 can be omitted.

2.2 Deflection circuit

The horizontal deflection stage contains the diode modulator which not only provides EW raster correction but also inner pincushion correction, picture width adjustment and EHT compensation.
It is not easy to achieve optimum scan linearity over the whole screen. Either the linearity inside the PAL test circle is good and outside the circle the performance is poor, or the average performance over the whole screen is good but inside the test circle deviation is visible.
In this application the S-correction capacitors C15 and C16 are balanced in such a way that a good compromise for the scan linearity is achieved.

Fig.2.3. Deflection circuit

As already stated in the introduction, due to high beam current in combined EHT and deflection stages picture distortions will occur.

One of these effects is the so called crosshatch "noses", visible as horizontal phase ringing just below each horizontal white line. During a bright horizontal line the EHT at the picture tube decreases. In the next flyback the picture tube capacitor is recharged by the line output transformer. This energy is taken from the S-correction capacitor, which must be recharged via the primary winding of the line output transformer. This action has a resonance of a few kHz and thus oscillation is visible at the screen.

To avoid this a dip rectifier is connected in parallel with the S-correction capacitor (D9, C14, R8). The energy taken from the S-correction capacitor can now be recharged by C14.

Another geometry distortion is the "Krückstockeffekt". Due to trapezium correction the EW-drive signal applied to L6 can be discontinuous. This will cause amplitude ringing at the top of the screen. An effective way to damp this ringing is a resistor in series with the EW-injection coil.

The consequence of the above mentioned measures is that the drive reserve of the diode modulator has decreased. To compensate for this a separate winding of the line output transformer is connected in series with the deflection coils.

2.3 EHT generation

For an optimum performance the black line picture tube must be driven at an increased EHT of 27.5kV @ $1.3mA_{av}$. This implies that the EHT in the no load condition will be about 29.5kV.
To generate this increased EHT a newly designed line output transformer is used with a 4-layer diode split EHT section. From an integrated potentiometer the adjustable focus and grid 2 voltages are taken.

Also the frame supply voltage (26V) and video supply voltage (180V) are taken from the line output transformer. The auxiliary windings of this transformer can be connected rather freely so that a diverse range of auxiliary supplies can be obtained. The only restriction is that the RMS value of the current in a given winding may not exceed 2A (target value).
Furthermore the supply current for the heater is obtained from this transformer just like the Φ2 feedback pulse (positive) and a (negative) pulse to synchronise the SMPS.

2.4 Auxiliary supply

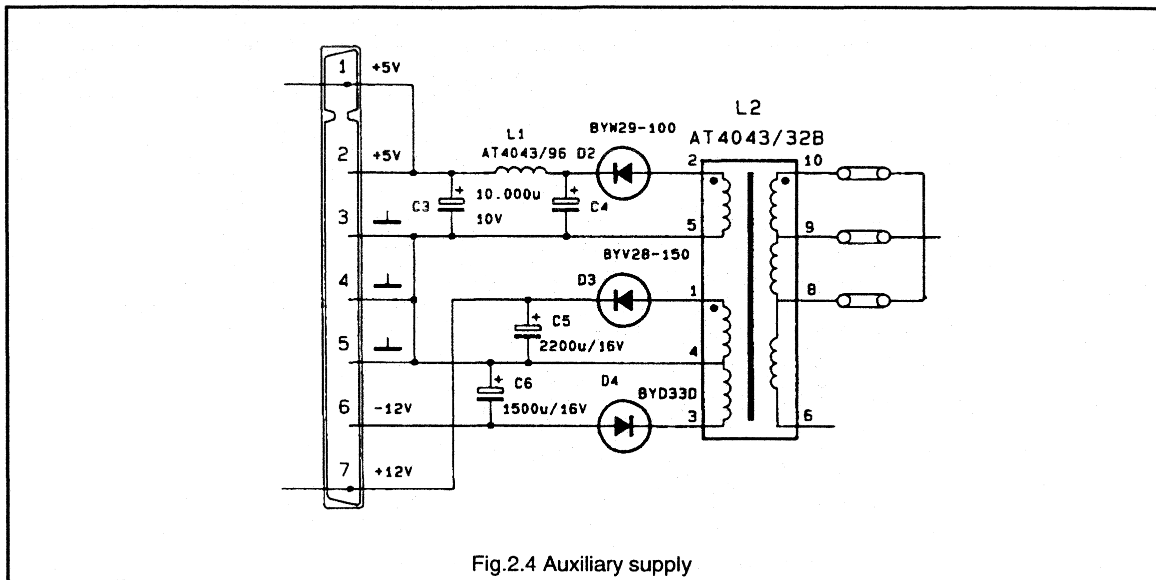


Fig.2.4 Auxiliary supply

When more auxiliary power than can be handled by the line output transformer is required, an auxiliary supply transformer as depicted in Fig.2.4 is a good alternative. Such an extra transformer in parallel with the primary winding of the line output transformer is an efficient way to generate low voltage high current supplies. As the transformer is optimised for this purpose no additional stabilisation is required.

Due to the high inductance of the primary winding no influence on the collector current is noticeable. Output voltages are very close to the target values (fine adjustment with primary taps) and have low Ri (HT line is stabilised).

2.5 Additional circuit information

12V supply:
The SMPS used in this concept delivers 16V unstabilised. This needs to be regulated to supply the sync processing IC which operates at 12V. This regulation can be done on the sync processing board or the horizontal deflection board since this also acts as a power distribution board.

Tuning voltage:
The tuning voltage is created simply by means of a series resistor R1 and a 30V reference diode located at the tuning board.

EHT compensation:
For proper picture performance it is essential that EHT information is available to compensate picture width and height for EHT variations. For this reason the aquadag is connected to the foot point of the line output transformer. This point is connected to ground by C18 and to the 26V by a non linear resistor network (R12, D11, R13, R14). This network is designed in such a way that it matches with the non linear impedance of the line output transformer and C18 matches with the picture tube capacitance. Thus the voltage available at the foot point of the line output transformer is a good representation of the EHT variation. This EHT information is sent to the geometry processor TDA8433.
This information can also be used for beam current limiting. It must then be fed to the video processor for contrast/brightness reduction.

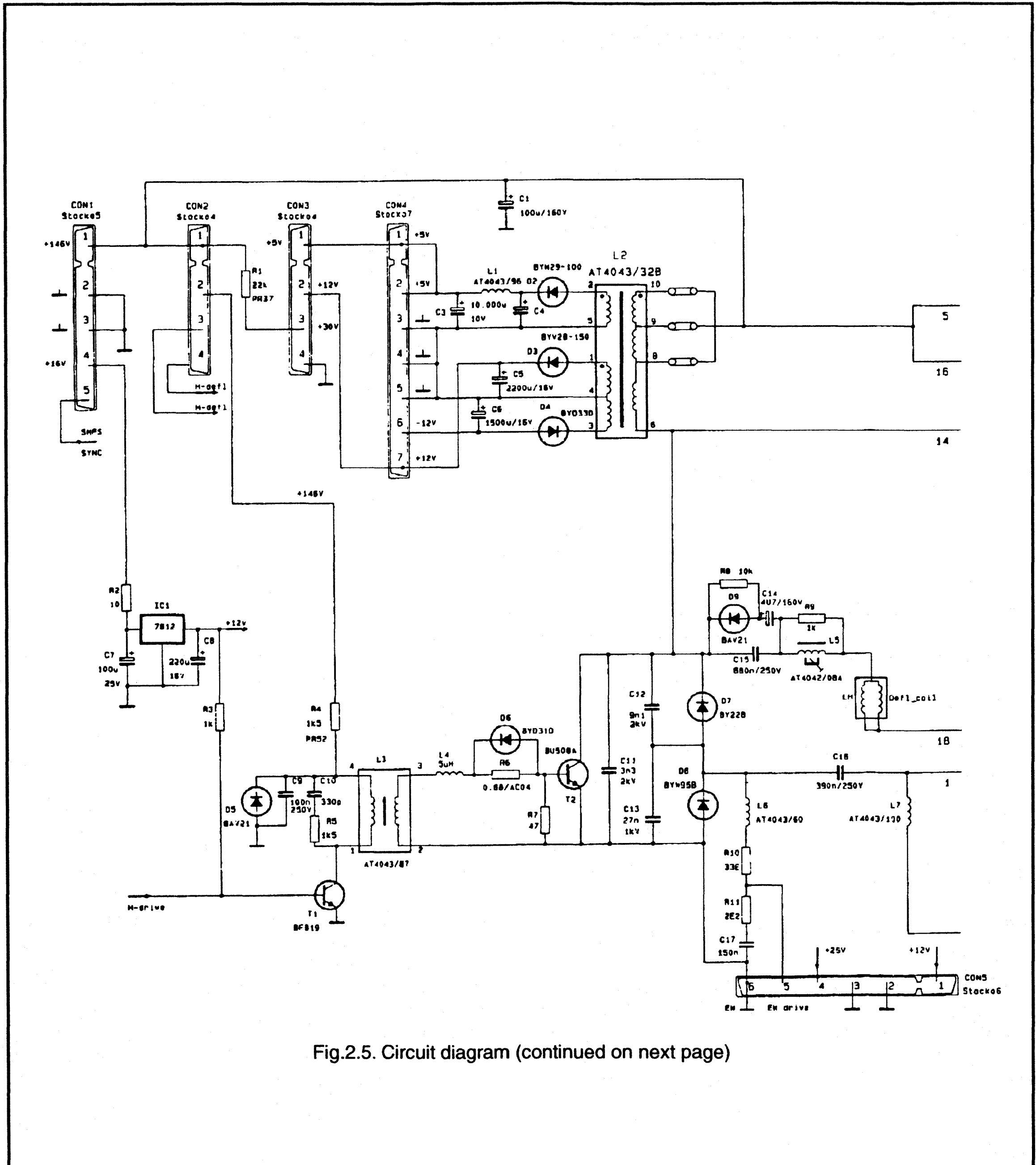


Fig.2.5. Circuit diagram (continued on next page)

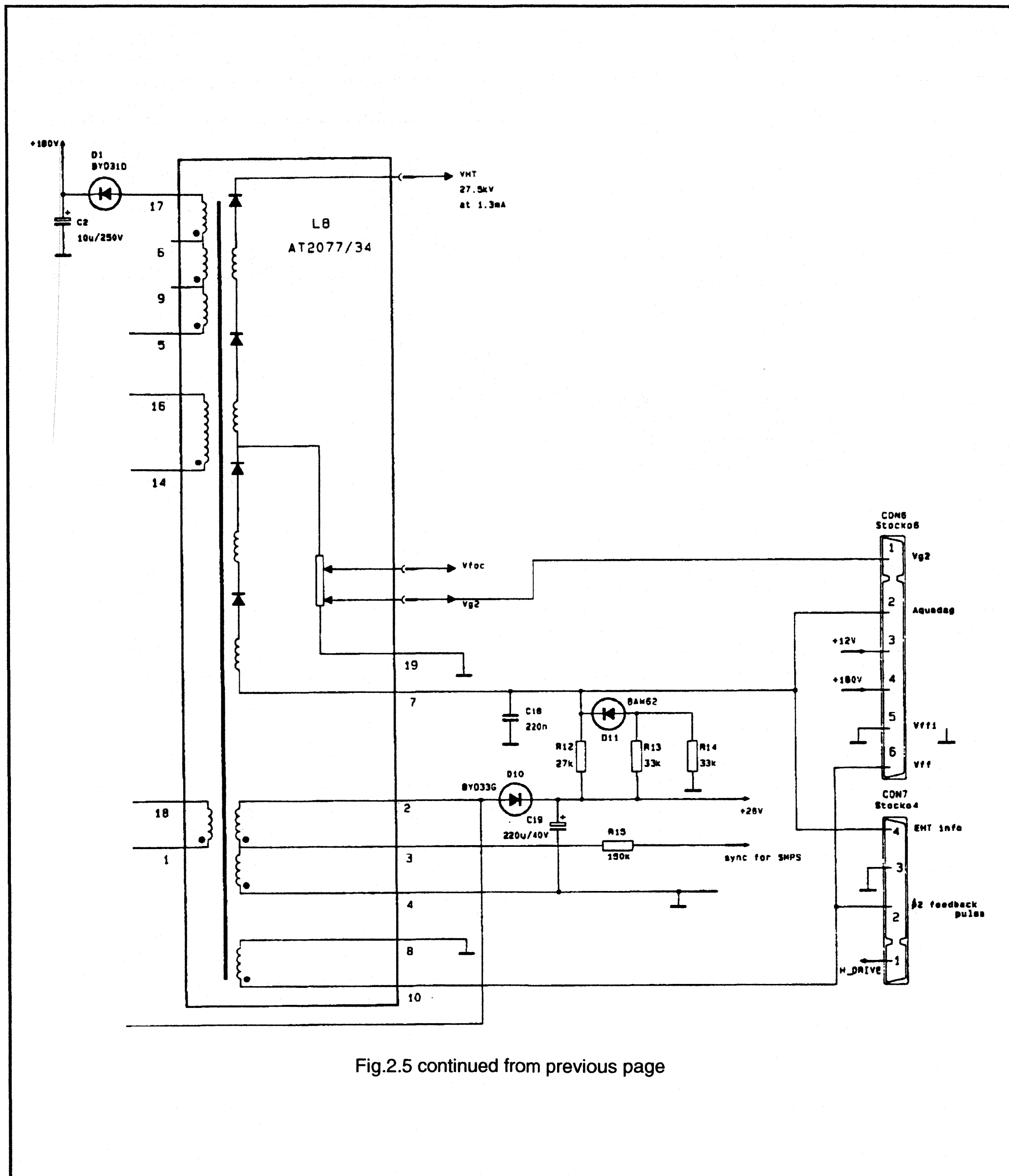
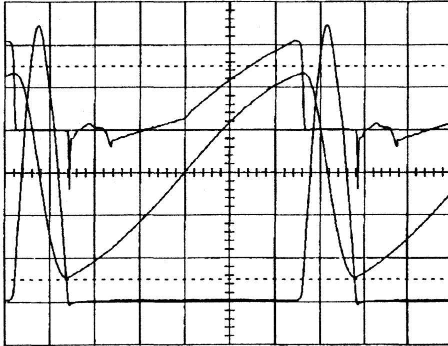


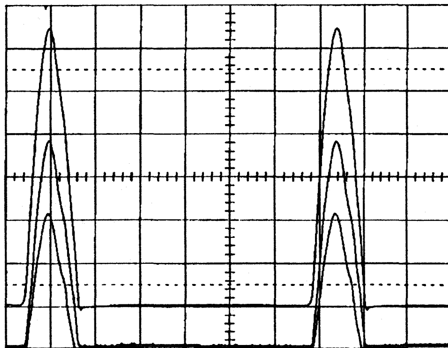
Fig.2.5 continued from previous page

3. Oscillograms

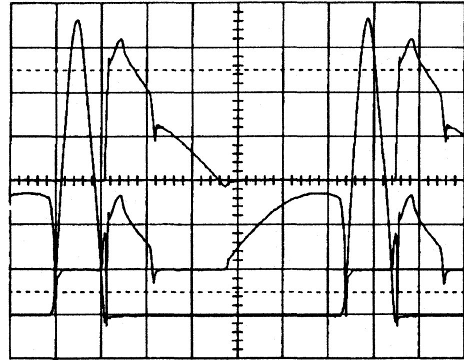


Oscillogram 1:
In this oscillogram the lower trace is the voltage across the deflection transistor (200V/div). The middle trace is the current in the horizontal deflection coil (1A/div). The upper trace is the collector current in the deflection transistor (2A/div). (x=10µs/div).

Remarks:
At the end of flyback there is a negative overshoot at the collector voltage. This is caused by the relative slow forward recovery of the efficiency diode. A part of this current is reverse conducted by the deflection transistor. About 12µs after the start of the scan the deflection transistor is turned on and starts reverse conducting and takes over a part of the current in the efficiency diodes. See also oscillogram 3.

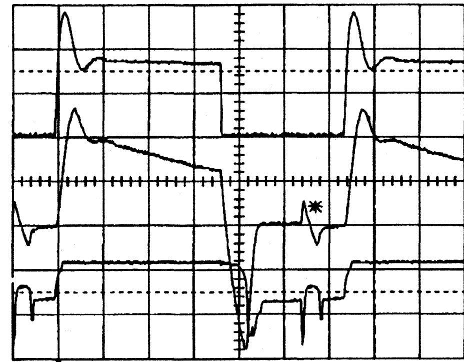


Oscillogram 2:
The upper trace is the voltage across the deflection transistor (200V/div). The lower two traces are the minimum and maximum voltage in the diode modulator (cathode D8) with nominal EW and amplitude settings (50V/div). (x=10µs/div).



Oscillogram 3:
In the upper trace the current in the upper efficiency diode is given (1A/div). The middle trace is the current in the lower efficiency diode (1A/div) (x=10µs/div).

Remarks:
12 µs after the start of the scan the deflection transistor is turned on. Current in the efficiency diode is than taken over by the deflection transistor. See also oscillogram 1.



Oscillogram 4:
In the upper trace the collector voltage of the driver transistor is shown (100V/div). The middle trace is the base drive current of the deflection transistor (1A/div). The lower trace is the base emitter voltage of the deflection transistor (5V/div). (x=10µs/div).

Remarks:
The overshoot at the collector voltage of the driver transistor is damped by R5 and C10. The current spike in the base drive current (marked with *) is the reverse conduction of the deflection transistor during the forward recovery of the efficiency diodes. See also oscillogram 1.

4. Vertical deflection, sync and geometry control

The vertical deflection, synch and geometry control circuits are based on an existing PCALE report (ref 3). Because for this application another tube and line output transformer are used some minor modifications are required (component values). See Fig.4.1.

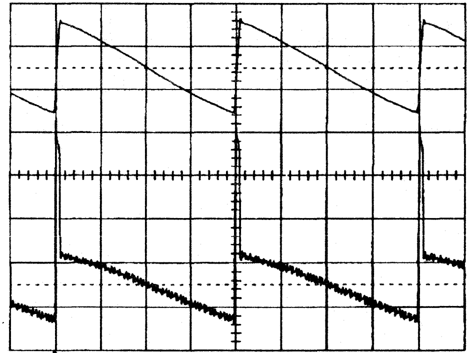
- Due to the increase deflection current the vertical feedback resistor must be decreased. One of the 2.2Ω resistors becomes 1 Ω.

- Due to the increased beam current the EHT compensation network at pin 24 of the TDA8433 needs to be modified; 120kΩ → 100kΩ, 82kΩ → 150kΩ, 27kΩ → 33kΩ, 68 nF → 10 nF.

- For additional phase shift pin 14 of the TDA2579 is biased with a current from a negative voltage source (rectified from the Φ_2 feedback pulse). While this feedback pulse is smaller than in the original circuit, the 240 kΩ resistor must be increased to 1.2MΩ.

Orientation values for the TDA8433 register settings are:

reg	hex
00	25
01	5A
02	07
03	2C
04	2B
05	16
06	16
07	15
08	22
09	21
0A	21
0B	0F
0F	04



Oscillogram 5:
Vertical deflection current (1A/div) and the output voltage (pin 5) of TDA3654 (10V/div). (x=5ms/div).

Remarks:
The noise on the output voltage is cross talk from the line deflection coils.

5. Video amplifiers

The gun of this picture tube is redesigned and has its optimum performance at a cut off voltage V_{CO}=160V. This implies that the video supply voltage should be at least 20V higher, so V_{video}>180V.
A video amplifier very well suited for this purpose is the TDA6100.

The RMS voltage of the heater winding of the line output transformer is V_{10}=7.35V_{RMS}, so a series resistor must be used (3.9 Ω 400mW).

6. References

Information from this section was extracted from "Application information for the 16 kHz black line picture tube A66EAK022X11 and A59EAK022X11"; ETV89010 by Han Misdom.

1."Some aspects of the diode modulator"; EDS7805 by C.H.J. Bergmans.

2."A synchronous 200W Switched Mode Power Supply intended for 32kHz TV"; ETV89009 by Henk Simons.

3."Deflection processor TDA8433 with I²C-bus control"; ETV8831 by D.J.A. Teuling

4."Application of the TDA6100 video output stage"; ETV8811 by D.J.A. Teuling

Fig.4.1. Vertical deflection, sync and geometry control

4.2.2 32kHz/100Hz deflection circuits for the 66FS Black Line picture tube A66EAK22X42

This report contains a description of deflection circuitry (horizontal 32kHz, vertical 50-120Hz) for the 66FS picture tube A66EAK22X42. This design is intended for flicker free TV applications. Provision is made to supply the power for the frequency conversion box.

Summary

The 66FS picture tube is compatible but not identical with the types of the 45AX range. To obtain the typical Black line high contrast and high brightness, the beam current and EHT must be increased at nominal operating conditions. This higher EHT also improves the spot quality. The deflection current is increased because of the higher EHT and reduced sensitivity of the deflection unit.

In comparison with laboratory report ETV8713 describing deflection circuits for 45AX, most modifications are found in the horizontal deflection stage. To generate the increased EHT power a new line output transformer with a four layer EHT coil is used. To handle the higher deflection currents two transistors are used in parallel and also two flyback capacitors are used. We have also taken the opportunity to introduce the TDA8433. This deflection processor -in BiMos technology- is the successor of the TDA8432.

The vertical deflection stage is redesigned in such a way that vertical shift signals can be inserted without bouncing effects. The insertion of vertical shift signals is necessary in 100 Hz operation for a proper interlace.

1. Introduction

In this report a description is given of double line and frame frequency (32kHz; 100 Hz) deflection circuits for the 66FS picture tube A66EAK22X42. The report is based on report ETV/8906, describing these circuits for the 78FS picture tube [1]. By changing some component values the PC board for the 78FS can also be applied to drive the picture tube A66EAK22X42. In the line output stage the new type output transistor BU2508 is used.

2. General description

2.1 Block diagram

The block diagram is given in Fig.2.1. The main interconnections are given as well. The separate blocks can be recognised in the circuit diagram.

The separate H and V sync and V shift are available from the frequency conversion box.

2.2 Circuit architecture

A key component in this set up is the deflection processor TDA8433. The horizontal and vertical picture geometry can be controlled by means of I^2C bus commands. Because this deflection processor has no vertical oscillator, there will be no vertical deflection when there are no vertical sync pulses applied to the set. For laboratory purpose a separate vertical oscillator is added to make the monitor part a self contained unit. When incorporated in a receiver this vertical oscillator can be omitted. When there are no vertical sync pulses, the guard circuit of the vertical output stage will blank the video information. This prevents spot burn-in of the tube.

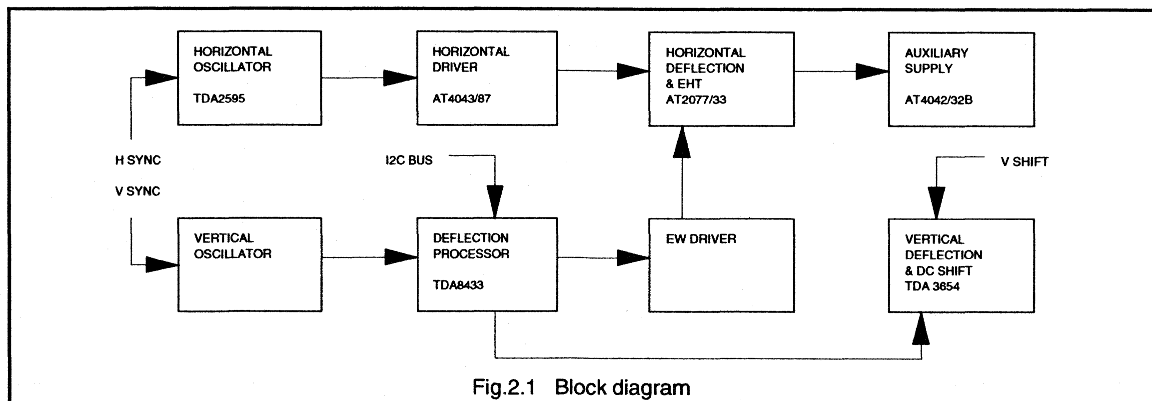


Fig.2.1 Block diagram

The vertical deflection stage consists of the well known TDA3654 vertical output IC. To make vertical shift insertion possible, the output stage is slightly redesigned. This AC coupled output stage now has a quasi DC coupled behaviour.

The EW driver is a voltage amplifier, acting as a buffer between the deflection processor and the diode modulator.

The block "horizontal oscillator" consists of the TDA2595 with its Φ1 and Φ2 loop, the horizontal oscillator itself and sandcastle generation. The other features of the IC are not used.

Coupling between the TDA 2595 and the deflection stage is made by horizontal driver stage. This stage is a transformer coupled inverting driver stage.

The horizontal deflection stage is a classic concept. It consists of a combined deflection and EHT generation. It also comprises linearity correction, S-correction, inner pin cushion correction and a DC shift circuit. The line output transformer (AT2077/33) belongs to the transformer family DSB (diode split box) and has four EHT layers. It delivers the following voltages:

* EHT = 27.5 kV @ 1.3mA
* Focus = 0.22 - 0.30 x EHT
* Vg_2 = 0.011 - 0.033 x EHT
* Heater ≈ $10.4V_{RMS}$
* Video supply = 192V
* Frame supply = 28V
* Φ2 ref. pulse = $+40V_{pp}$

Furthermore the line output transformer (LOT) has some taps which can be useful when the application is modified.

In parallel to the primary winding of the LOT the auxiliary supply transformer (AT4043/32B) is located. This auxiliary supply delivers the following voltages:

* +5V @ 5A
* +15V @ 1A
* -12V @ 1A

These supply voltages are intended for the digital and analog signal processing circuits.

The philosophy behind this circuit needs some further explanation.

It is very difficult to generate exactly 5V at the output of an SMPS or LOT. Due to an optimum winding design of this kind of transformer, the voltage ratio per turn is high (2 - 5V per turn). This implies that a stabilizer is required. A switching post regulator adds to the circuit complexity and cost. A dissipative series stabiliser needs at least 2V, so for a 5A supply the losses are already 10W.

The auxiliary transformer used in this concept is optimised for generating these low voltages at high currents. The winding design is such that no stabilizer is required after the rectifier. Due to the high primary inductance of this transformer the collector current increase of the deflection transistor is negligible.

If the auxiliary loads are low, this auxiliary supply transformer can be omitted and the unused taps of the LOT can be used to generate these voltages.

3. Circuit description

On the basis of sub circuit diagrams the functioning of this concept will be explained. This will be done with reference to the function blocks of Fig.1. The complete circuit diagram is given in Fig.7.1.

3.1 Vertical oscillator

As already stated in section 2.2 this vertical oscillator can be omitted in a final design.

This oscillator is the well known astable multivibrator built up around T8 and T9. This oscillator is free running at 45Hz and can be synchronised up to at least 120Hz. T7 is an additional sync transistor and is ac-coupled to the vertical sync signal (TTL level).

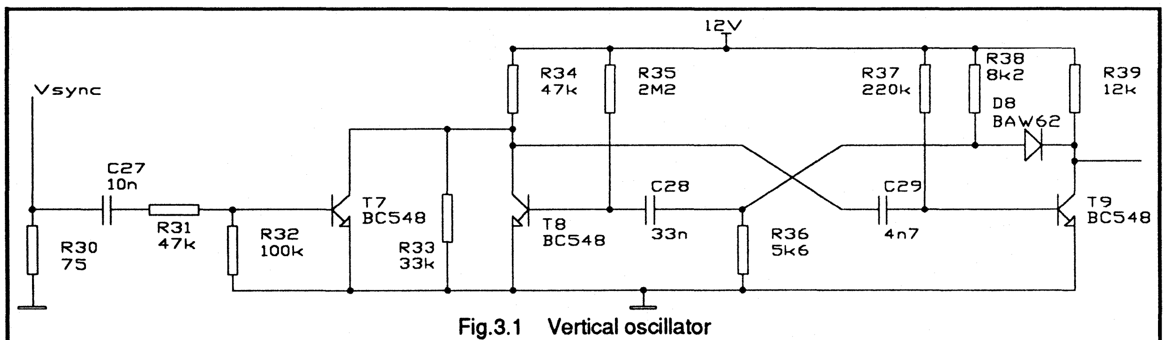


Fig.3.1 Vertical oscillator

3.2 Deflection processor TDA8433

The TDA8433 is an analog, I²C bus controlled, deflection processor. It generates the vertical deflection current waveform and the EW (East-West) waveform. The necessary corrections on these waveforms are I²C bus controlled. On board of this IC there are also some DACs and ADCs. They can be used for control functions of other circuitry [2].

The resistor at pin 4 determines the reference current for this IC. Pin 2 is the vertical sync input. At the capacitor at pin 5 (C-flyback) a triangle waveform is generated which is used for internal timing. This signal is used to generate the vertical sawtooth at pin 22 (C-saw). At pin 23 (C-amp1) a storage capacitor of the amplitude stablisation loop is found whose voltage determines the amplitude of the saw. The V-sync input can only handle unequal spacings of the pulses if there is a 2-sequence (e.g. Teletext 312-313 lines). A 4-sequence from the 100Hz box cannot be handled by the amplitude loop.

The vertical sawtooth is internally connected to the "geometry control" section. In this section S-correction, vertical shift and linearity correction are added to the sawtooth by I²C commands. The amplitude is controlled by pin 24 (EHT-comp) to compensate for EHT variations.

From here the signal goes to one input of the internal error amplifier. The other input is connected to pin 21 and the output to pin 20. By means of an I²C command the external input pin can be selected as an inverting or non-inverting input. This provision is made to handle both non-inverting and inverting vertical output stages.

The block "geometry control" also generates the EW parabola. The I²C bus controllable functions are: parabola, corner, trapezium and picture width. By means of the signal at pin 24 this signal is corrected for EHT variations. The EW drive output is available on pin 19.

On the digital side of this IC we find the following functions:

Pin 15 (SCL) is the Serial CLock and pin 14 (SDA) is the Serial DAta. Pin 1 is the address pin and can either be connected to ground or +12V. The three external DA converters can be controlled by the bus: DACA, DACB & DACC. With DACA the horizontal free funning frequency of the TDA2595 can be adjusted. The other two DACs (pin 7 & 6) are not used. They can be used for H-shift and H-phase control. See appendix A.
Pins 9 and 10 are output switch functions: not used in this application. When pin 10 is programmed high, it can be used as an input pin. Together with pin 17 it forms a comparator. Pin 10 is connected to the Φ1 voltage of the TDA2595 and pin 17 to the reference voltage. In this way an I²C bus signal is available whether the horizontal oscillator is in centre, locked and mute or coincidence so information can be sent to the IN-input. This also makes automatic f_0 adjustment possible.

The supply part of this IC contains 4 pins. Pin 18 is ground for the geometry and sawtooth part: pin 13 is ground for the output stages and I²C bus. Pin 12 is the +12V input and at pin 16 an external capacitor is required for filtering the +5V (internal generated).

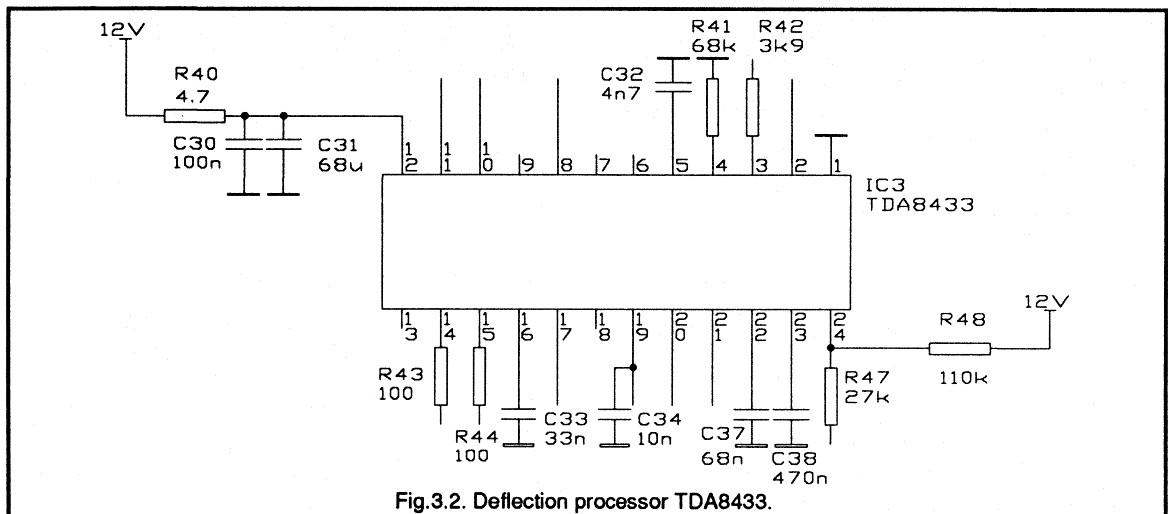


Fig.3.2. Deflection processor TDA8433.

3.3 Vertical output stage

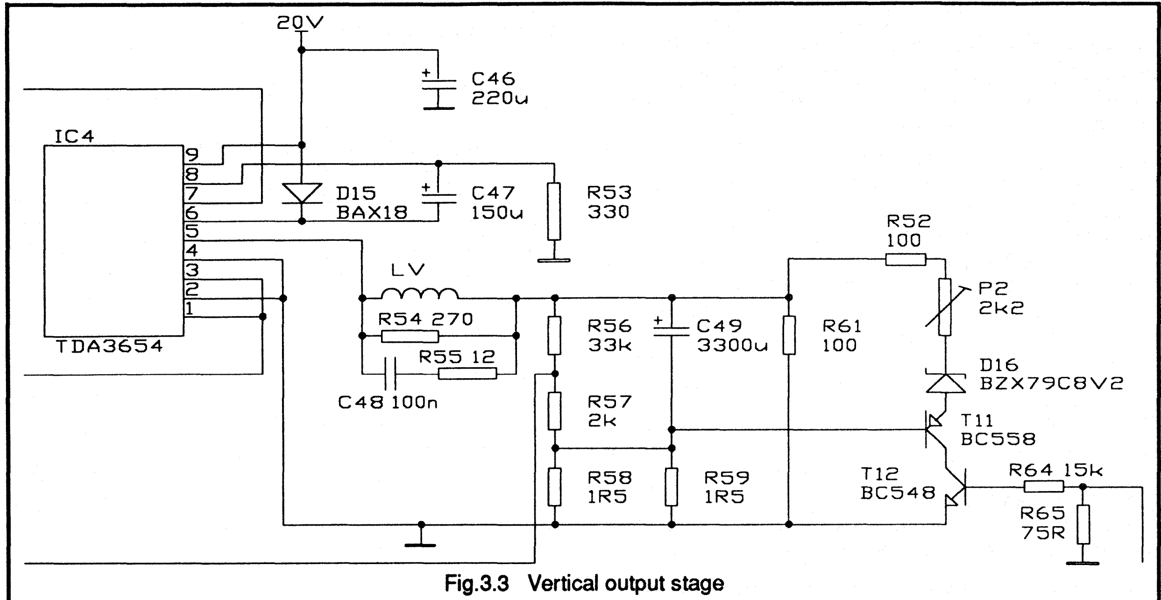


Fig.3.3 Vertical output stage

The vertical output stage is the well known TDA3654. To make this stage suited for 100Hz TV some modifications of the ordinary solution are required. See Fig.3.3.

A damper network is located in parallel to the vertical deflection coil. The values depend on the characteristics of the deflection unit. The line ripple that is injected from the horizontal deflection coil is damped by the series connection of R55 and C48. R55 reduces the line ripple to an acceptable value. C48 is added to block the relatively low vertical deflection voltage in order to limit the dissipation in R55. A resonant circuit is created by C48 and the inductance of the deflection coil. R54 is a critical damper for this circuit to minimise excessive oscillations after the vertical flyback.

The deflection current is measured by two 1.5 Ω resistors in parallel and fed back to the deflection processor. The network C36, R45 and C35 is added for a stable loop transfer because of the non resistive load at the output of the TDA3654.

The output stage is AC coupled. The DC bias point is fixed by the resistors R60 and R61. By the V-shift setting of the TDA8433 vertical shift of the picture is possible.

An additional shift circuit is connected in parallel to the DC shift circuit to make an alternating frame shift possible. It consists of T11 and its series elements. When T11 is conducting a small DC current will flow through the deflection coil. Due to the S-correction of the vertical deflection current a smaller current is required at the top and bottom than in the middle of the tube to guarantee proper interlacing across the whole screen. Therefore the waveform of the shift current is derived from the parabola voltage of C49. A potentiometer is provided because this interlace setting is critical.

The drive signal required for this alternating frame shift is generated by the 100Hz conversion box.

If two independent shift signals are needed, the whole circuit must be duplicated.

3.4 Horizontal oscillator

The horizontal oscillator used is the TDA2595. The horizontal sync signal (TTL level) is divided and ac-coupled to the input pin 11. At pin 14 the reference current is set by a 13 kΩ resistor. The sawtooth capacitor for the oscillator is connected to pin 16. The free running frequency is 31.25kHz and determined by the value of its capacitor and the reference current. By varying the reference current the free running frequency can be adjusted. This is done using the DAC-A output (pin 8) of the TDA8433 via resistor R25. See section 3.2.

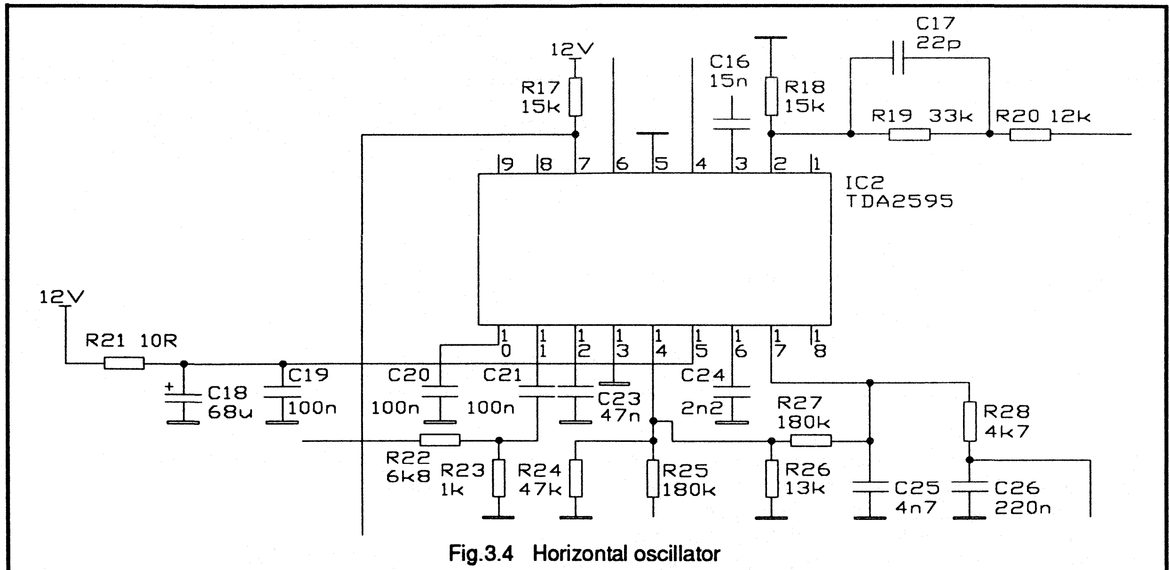


Fig.3.4 Horizontal oscillator

This oscillator is locked to the incoming sync signal by a PLL (Phase Locked Loop). The starting point of the horizontal sawtooth is compared with the horizontal sync. If this starting point is not in the middle of the horizontal sync pulse, an error signal will appear at pin 17. Via R27 the current of pin 14 is affected and thus the horizontal phase can be locked. The loop filter consists of C25, R28 and C26.

The output of the oscillator is internally connected to a second PLL Φ2 and to a phase shifter. The phase shifted signal is available via an output stage at pin 4 (horizontal output). This signal drives the deflection stage. A feedback signal of the deflection stage is applied to the other input of the Φ2 phase detector (pin 2). In this way the horizontal flyback of the deflection stage is locked to the oscillator and thus to the sync as well. The loop filter of Φ2 consists of one capacitor at pin 3.
This second PLL has a much larger bandwidth for compensating for the quick storage time variations in the deflection transistors.

At pin 6 a two level sandcastle pulse is available. It is mixed with the vertical blanking signal of the TDA8433 or the flyback of the TDA 3654 to generate a three level sandcastle. See also description of TDA8433 section 3.2 and TDA3654 section 3.3.

Pin 7 is the mute output. This signal is sent to the TDA8433 so that "oscillator locked" information is available at the I²C bus.

As these kinds of IC are sensitive to supply pollution provision is made for a local supply filter R21, C18 and C19.

For layout recommendations see section 4.

3.5 Horizontal drive circuit

The horizontal drive circuit is a classical transformer coupled inverting driver stage. When driver transistor T1 is conducting, energy is stored in the transformer. When T1 is turned off the magnetising current continues to flow in the secondary side of the transformer thus turning on the deflection transistor. At this time the voltage on the secondary side of the driver transformer is positive (V_{BE}+I_B*R6). When the driver transistor turns on again this secondary voltage reverses. At the same time energy is stored in the transformer again.

During this turn off action the forward base drive current decreases with a controlled dI/dt, thereby removing the stored charge from the deflection transistor. The dI/dt depends on the negative secondary voltage and the leakage inductance. When the drive circuit is designed properly, the deflection transistor stops conducting when its negative base current is about half the collector peak current.

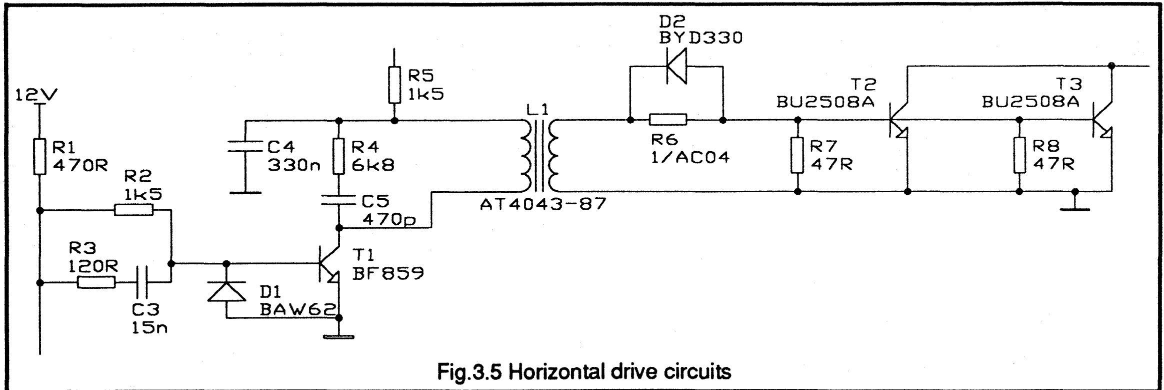


Fig.3.5 Horizontal drive circuits

To prevent the deflection transistor from turning on during flyback due to parasitic ringing on the secondary side of the driver transformer a damp resistor is connected in parallel with the base emitter junction of the deflection transistor. Also at the primary side of the driver transformer a damp network is added (R4 & C5) to limit the peak voltage on the driver transistor.

3.6 Horizontal deflection

Fig.3.6 Horizontal deflection

The horizontal deflection is the classical deflection stage with the diode modulator which not only provides the EW raster correction but also inner pincushion correction. Due to the high frequency in combination with large currents some problems do appear here. The horizontal deflection coil needs 10.4App. This results in a collector peak current of 6-7A, too much to handle with one BU2508A. So two transistors are used in parallel. If the print layout is made in a proper way no special precautions are required to use this type of transistor in a parallel configuration. (NB the circuit was constructed before the BU2525 became availabe.)

For the flyback capacitor the current is too high as well. So also here two devices are used in parallel. The S-correction capacitors do not have problems in handling the current.

The solution for the efficiency diodes is not common. At the moment there is no diode in power encapsulation available for this purpose. So a smaller type in glass passivation is used. To improve the thermal performance a heat sink is soldered onto the connecting leads. Another measure taken is a third efficiency diode that is connected directly across the collector emitter of the deflection transistor. This diode takes over a part of the current that normally would flow in D4.

For full performance of scan linearity a horizontal DC shift circuit is incorporated. In an ordinary TV set the horizontal off centre of the picture tube is compensated by the phase shift of the horizontal oscillator. This however introduces a linearity error in the deflection. In many cases this error is acceptable or one tries to compensate this by means of an adjustable linearity corrector.

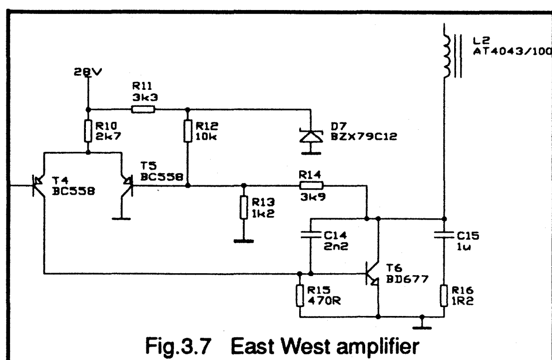


Fig.3.7 East West amplifier

The most proper way of picture alignment is the following: the linearity corrector is only used for compensating the linearity error caused by the resistive part of the impedance of the horizontal deflection yoke. The off centre of the tube is compensated by a shift circuit. Therefore a DC shift circuit is incorporated. This circuit has been built up around L5. With P1 the amount of shift current can be adjusted and with S1 the polarity can be selected.

The horizontal shift can be made bus controlled by using DAC-B or DAC-C of the TDA8433. A suggestion for a suitable interface is given in Appendix 2.

3.7 East west correction

The EW waveform is generated by the deflection processor TDA8433. An external amplifier feeds this correction to the horizontal deflection stage. It is injected in deflection via L2. The possible corrections are: picture width, EW parabola, corner correction, trapezium and EHT compensation.

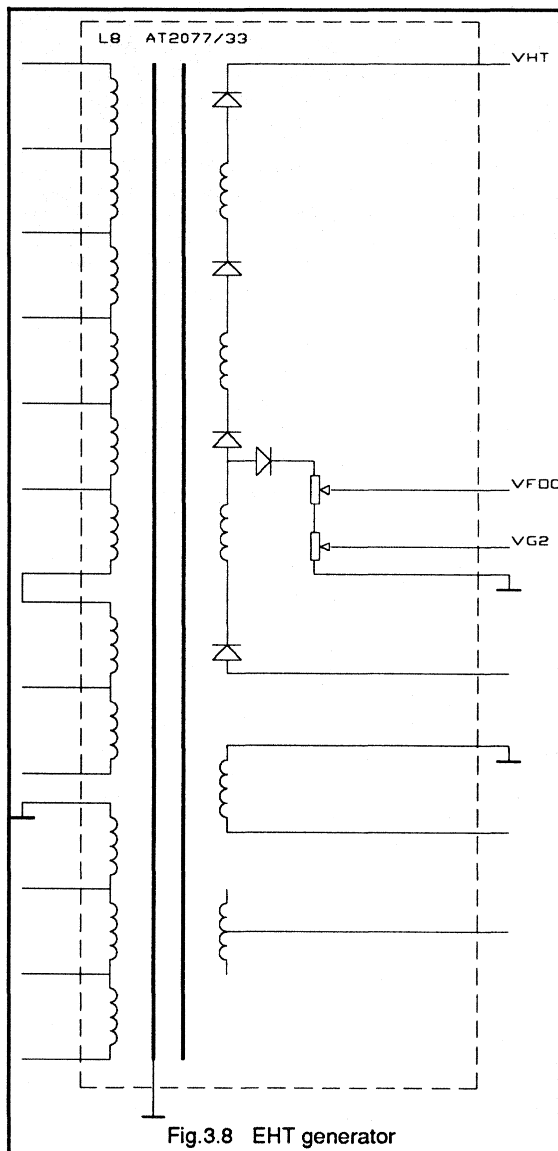


Fig.3.8 EHT generator

The EW amplifier is given in the Fig.above. It consists of a Darlington power transistor, the differential amplifier T4 T5 and a feedback network R13 R14. R12 is added for a proper DC-bias.
Because this amplifier has a non real load, special attention is paid to loop stability. Across T6 there is a miller capacitor. The line ripple current of L2 flows mainly through C15 and R16.

3.8 EHT generation

The darker glass requires a higher EHT power for an equal light output. An increase of only the beam current has two disadvantages: a larger spot size and a higher drive from the video amplifiers. An increase of only the high voltage would come in conflict with the legislation on X-ray radiation.

As a compromise an EHT=27.5kV @ 1.3mA is chosen. A new designed line output transformer is used. See Fig.3.8. To handle the increased high voltage a four layer diode split line output transformer is used. From an integrated potentiometer the adjustable focus and grid 2 voltage are taken.

3.9 Auxiliary supply

Some of the auxiliary supplies are taken from the LOT such as heater, video and frame supply. The other auxiliary supplies are taken from a separate transformer. The philosophy behind this concept is already explained in section 2.2.

The auxiliary transformer is connected in parallel to the line output transformer. On the secondary side of this transformer the auxiliary voltages are taken. They supply the signal processing circuitry (5V @ 5A, 12V @ 1A, -12V @ 1A).

The primary inductance of this transformer is relatively high, so the increase of collector current for the deflection transistor is low. To adjust the output voltage the primary winding has some taps. Due to the relative high ESR of the 5V smoothing capacitors a π-filter is required.

With moderate current levels all the auxiliary supplies can be taken from the line output transformer.

4. Printed circuit board design considerations

For general information see reference 3.

4.1 TDA2595

The following tracks and pins of the TDA2595 are critical and need special attention:

* The track length at pin 14 - reference pin - to its peripherals should be kept as short as possible.

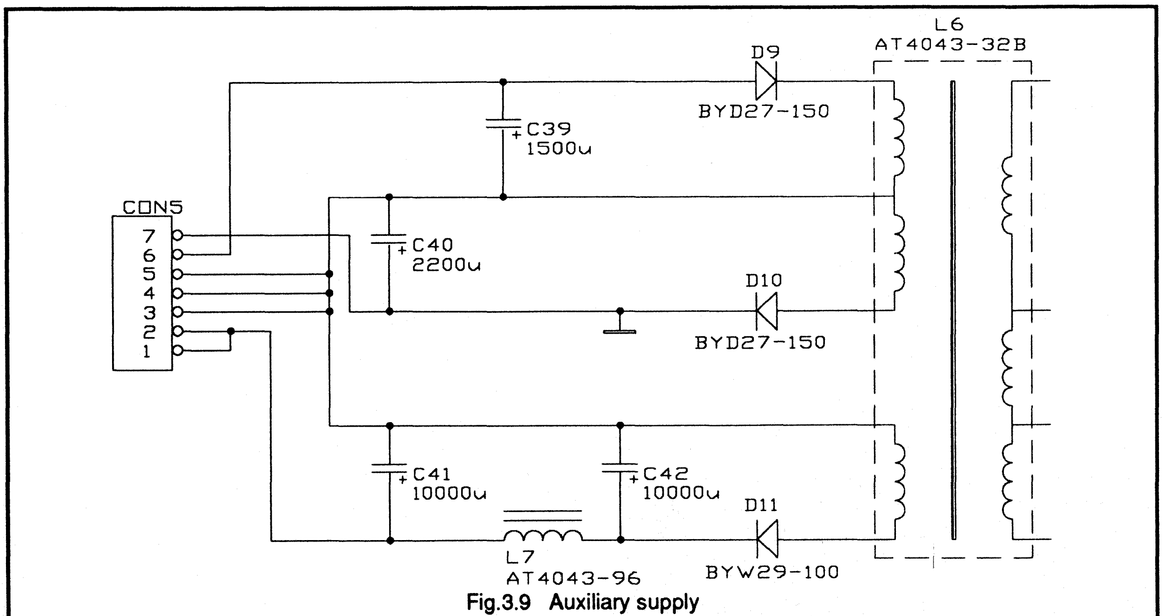


Fig.3.9 Auxiliary supply

* The peripheral components connected to pin numbers 14, 16, 3, 17 and 15 should be connected directly to the ground of this IC.
* The ground track of this IC may not carry current from other parts of the set.
* As this IC is sensitive for high frequency ripple on the supply rail a local decoupling is essential.

4.2 TDA8433

The following tracks and pins of the TDA8433 are critical and need special attention:

* The components connected to pin numbers 4, 5, 12, 16, 19, 22 and 23 should be connected to the analog ground (pin 18) as close as possible.
* The track length of the pin numbers 4, 5, 22 and 23 should be as short as possible.
* The ground track of this IC may not carry current from other parts of the set.
* Local decoupling is essential because this IC is sensitive for high frequency ripple on the supply rail.

4.3 Horizontal deflection and supply rectifiers

This kind of circuit carries currents with high dI/dt. The loops that contain these currents should have an area as small as possible to limit magnetic radiation.
Examples are the loop of deflection coil with the deflection transistors, diodes and flyback capacitors.
Also the loop formed by smoothing capacitor C43, primary of LOT and deflection transistor should be kept small.

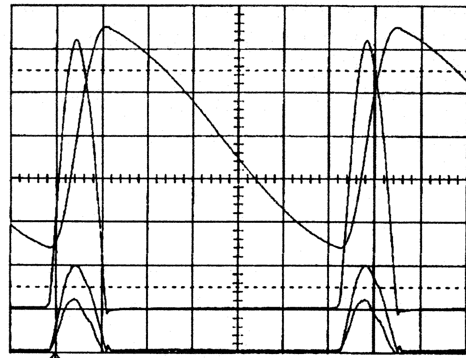
In case of rectifiers the ground track between transformer winding and smoothing capacitor may not be a part of any other ground track.

4.4 Drive circuit

To ensure current balance in the deflection transistors, the base and emitter tracks of the two transistors should be as similar as possible to create the same impedances for both transistors.

5. Oscillograms

All oscillograms were taken under nominal load conditions of the auxiliary supply and 1mA beam current.



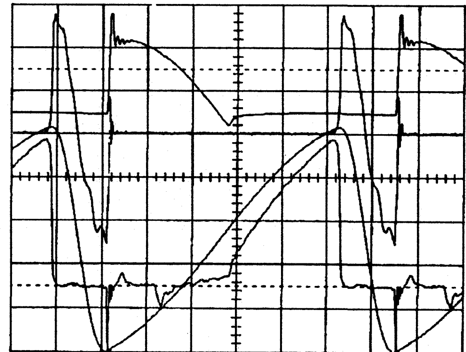
Oscillogram 1:

In this oscillogram the upper two traces show the average deflection current (2A/div) and the voltage across the deflection transistors (200V/div). The collector peak voltage is 1244V.

The lower two traces are the minimum and maximum values at the mid-point of the diode modulator (100V/div) due to EW modulation.

Remarks:

At the end of flyback there is a negative over shoot at the collector voltage. This is caused by the relative slow forward recovery of the efficiency diode.

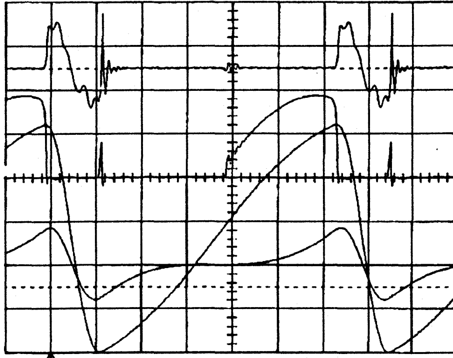


Oscillogram 2:

The lower trace is the current in the deflection transistors. The upper trace is the current in efficiency diode D4 and the middle trace is the current in the upper flyback capacitors (C7 + C8). All current settings 2A/div.

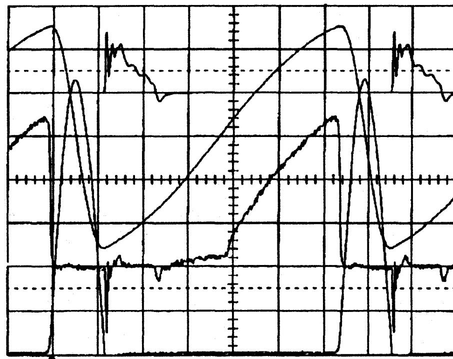
Remarks:

At the end of flyback the current in the flyback capacitor is taken over by the efficiency diodes. Due to parasitic capacitors and inductances ringing occurs. At 5 µs later there is a negative current in the deflection transistor. This is reverse conducting of the transistor caused by the fact that the base drive is already turned on.



Oscillogram 3:

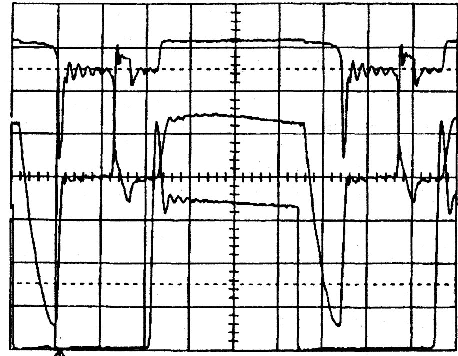
In this oscillogram the upper trace is the current in the lower flyback capacitors C9 + C10. The second trace is the current in the lower efficiency diode D5. In the bottom part the current in the bridge coil is given and the deflection current is shown once more as a reference.
All settings 2A/div.



Oscillogram 4:

In this oscillogram the deflection current and collector emitter voltages are given as a reference.

The upper trace is the current in the third efficiency diode D3. As soon as the deflection transistor is turned on the current of D3 is taken over by the transistors.
All current settings 2A/div.



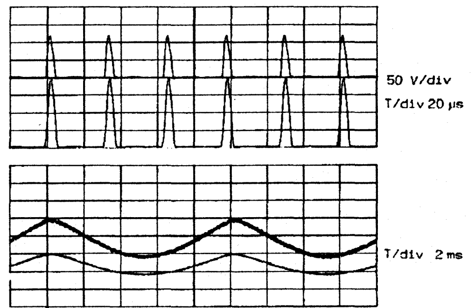
Oscillogram 5:

The upper trace is the base emitter voltage of the deflection transistors (5V/div). The middle trace is the base current of the deflection transistors (1A/div). The lower trace is the collector voltage of the drive transistor T1 (50V/div).

Remarks:

The over shoot at the rising edge of the driver transistor is caused by the leakage inductance of the driver transformer. By means of the damp network R4 C5 this over shoot is limited. This network is chosen in such a way that the ringing is critically damped.

The base drive circuit is designed in such a way that the peak of the negative base driver current is approximately half the collector current. During the turn off state of the deflection transistors the base voltage should remain negative. To achieve this the ringing is damped by R7 and R8.

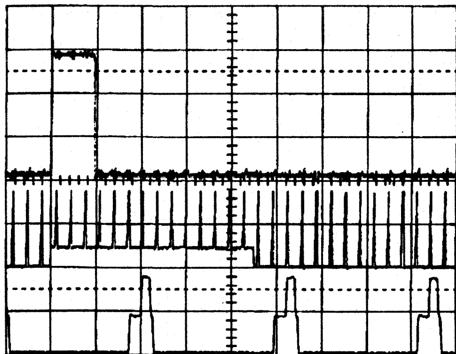


Oscillogram 6:

This split screen oscillogram was made with two different time base settings. In the upper grid the minimum and maximum values of the flyback pulses across C9 + C10 of the diode modulator are given under nominal conditions. The lower grid shows the amplified EW drive signal (collector T6 5V/div) and the output of the TDA8433 (pin 19 2V/div).

Remarks:

At the collector of T6 some line ripple is visible.

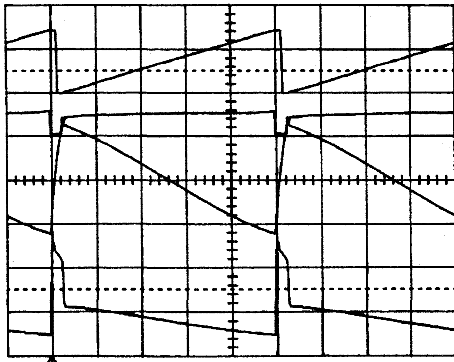


Oscillogram 7:

The upper trace gives the vertical sync signal (1V/div 100 us/div). The middle trace is the sandcastle (5V/div 100 us/div). The lower trace is the sandcastle during vertical scan (5V/div 10 us/div).

Remark:

This three level sandcastle pulse is the sum of the two level sandcastle of the TDA2595 and the vertical blanking of the TDA8433.

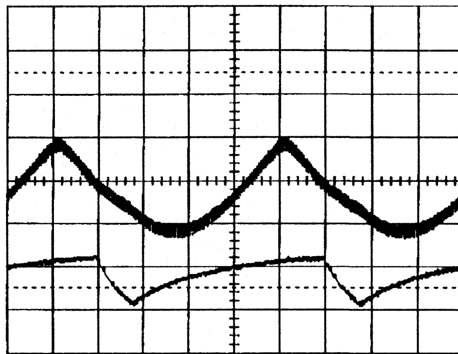


Oscillogram 8:

The upper trace is the generated sawtooth at pin 22 of the TDA8433 (5V/div). The second trace is the output signal of the error amplifier of the TDA8433 pin 20 (5V/div). The third trace is the sawtooth current in the vertical deflection coil (1A/div). The lower trace is the output signal of the vertical output amplifier TDA3654 pin 5 (20V/div).

Remark:

Due to the L/R of the vertical deflection coil the current in the coil can not follow the fast retrace time of the sawtooth generator. The output amplifier clamps after the flyback to 2xVb. When the control loop locks after the flyback, a slight voltage overshoot can be found at the output of the TDA3654. This is damped by C48, R55 and R54.



Oscillogram 9:

The lower trace is the voltage at the foot point of the line output transformer (10V/div). This signal is a representation of the EHT variations needed by the anti breathing.

The upper trace is the EW waveform at T6 (5V/div). On the EW waveform a correction signal is added to prevent the picture from breathing.

6. References

Information for this section was extracted from "32kHz/100Hz deflection circuits for the 66FS Black Line picture tube A66EAK22X42"; ETV89012 by J.v.d.Hooff.

1. P.C.A.L.E. report ETV/8906. "32kHz/100Hz deflection circuits for the 78FS picture tube" by Mr. J.A.C. Misdom.
2. C.A.B. report ETV8612. "Computer controlled TV; the deflection processor TDA8432" by Messrs. E.M. Ponte and S.J. van Raalte.
3. C.A.B. report ETV8702: "EMC in TV receivers and monitors" by Mr. D.J.A. Teuling.

7. Circuit diagram

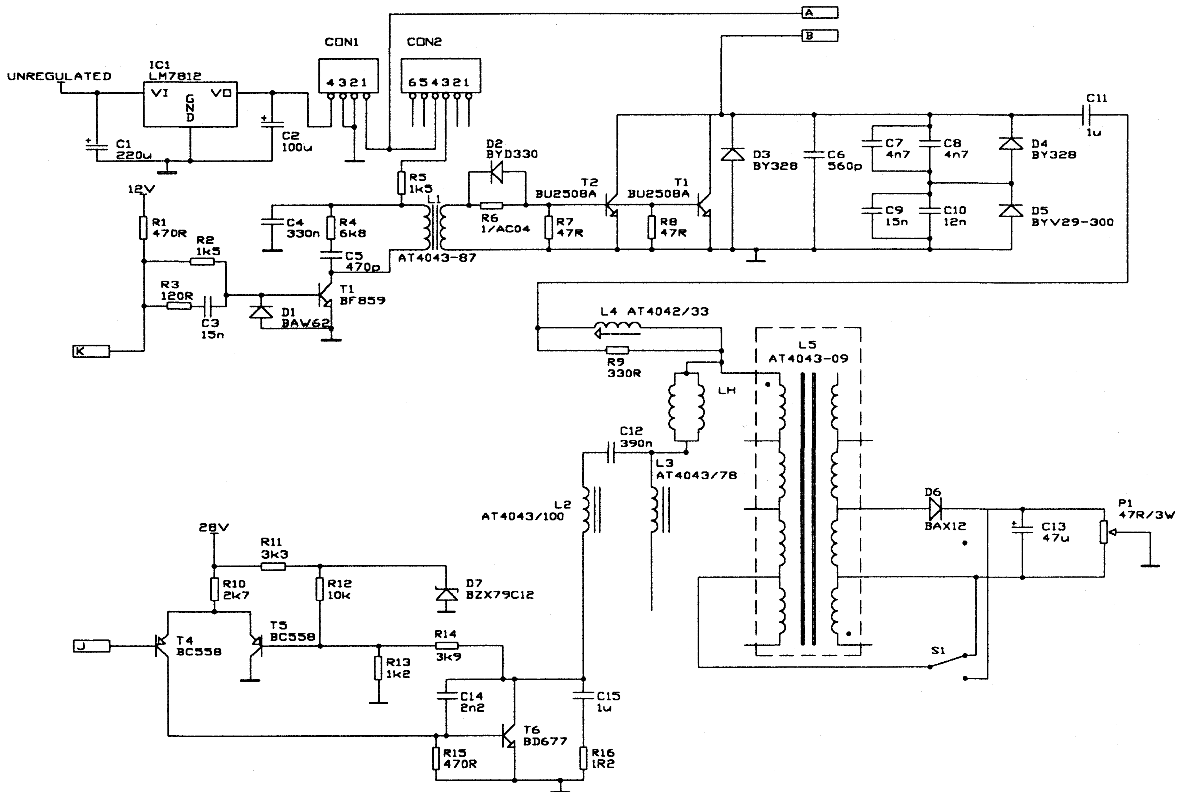


Fig.7.1 (continued on next 2 pages)

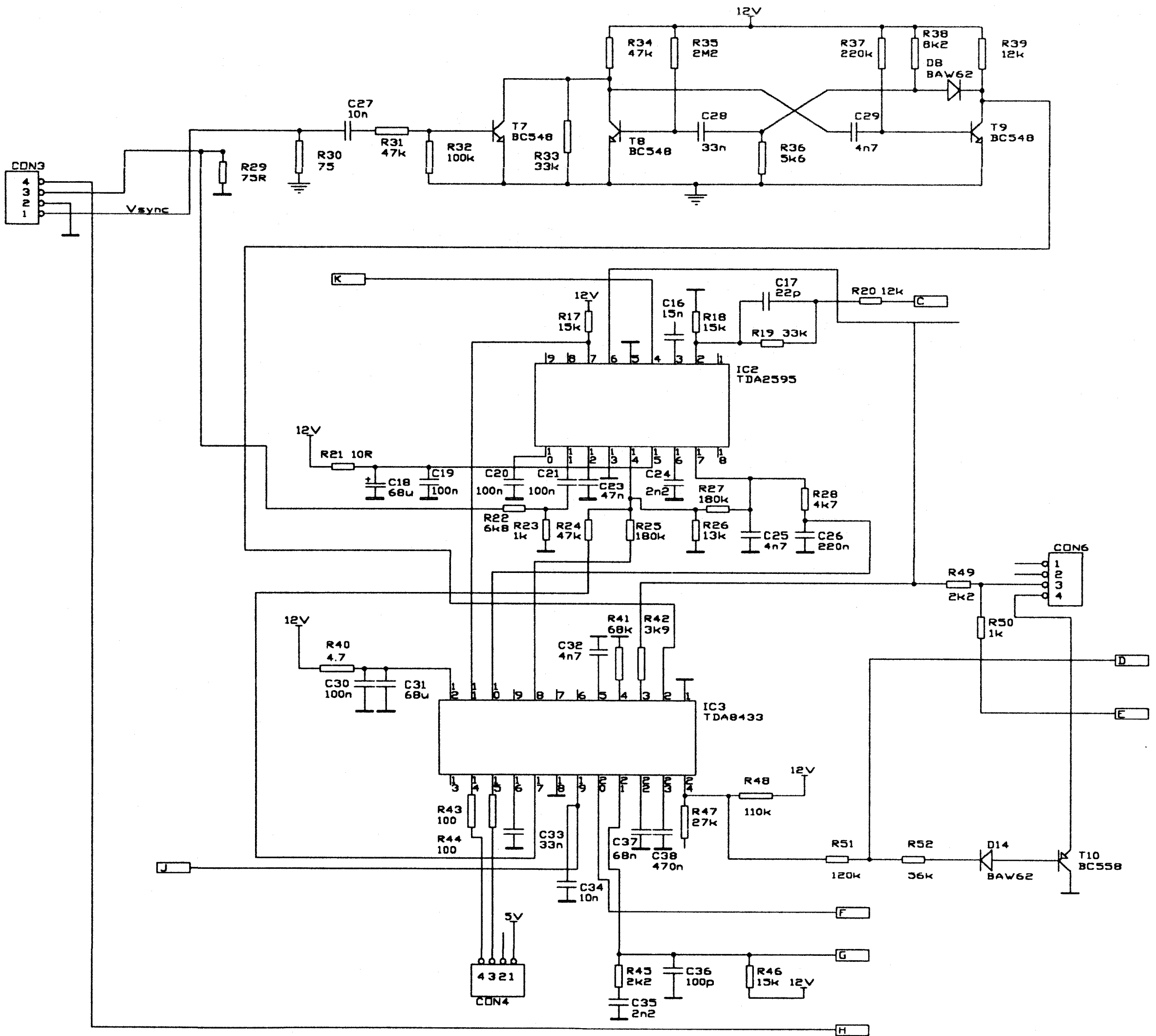


Fig.7.1 (continued from previous page, see also following page)

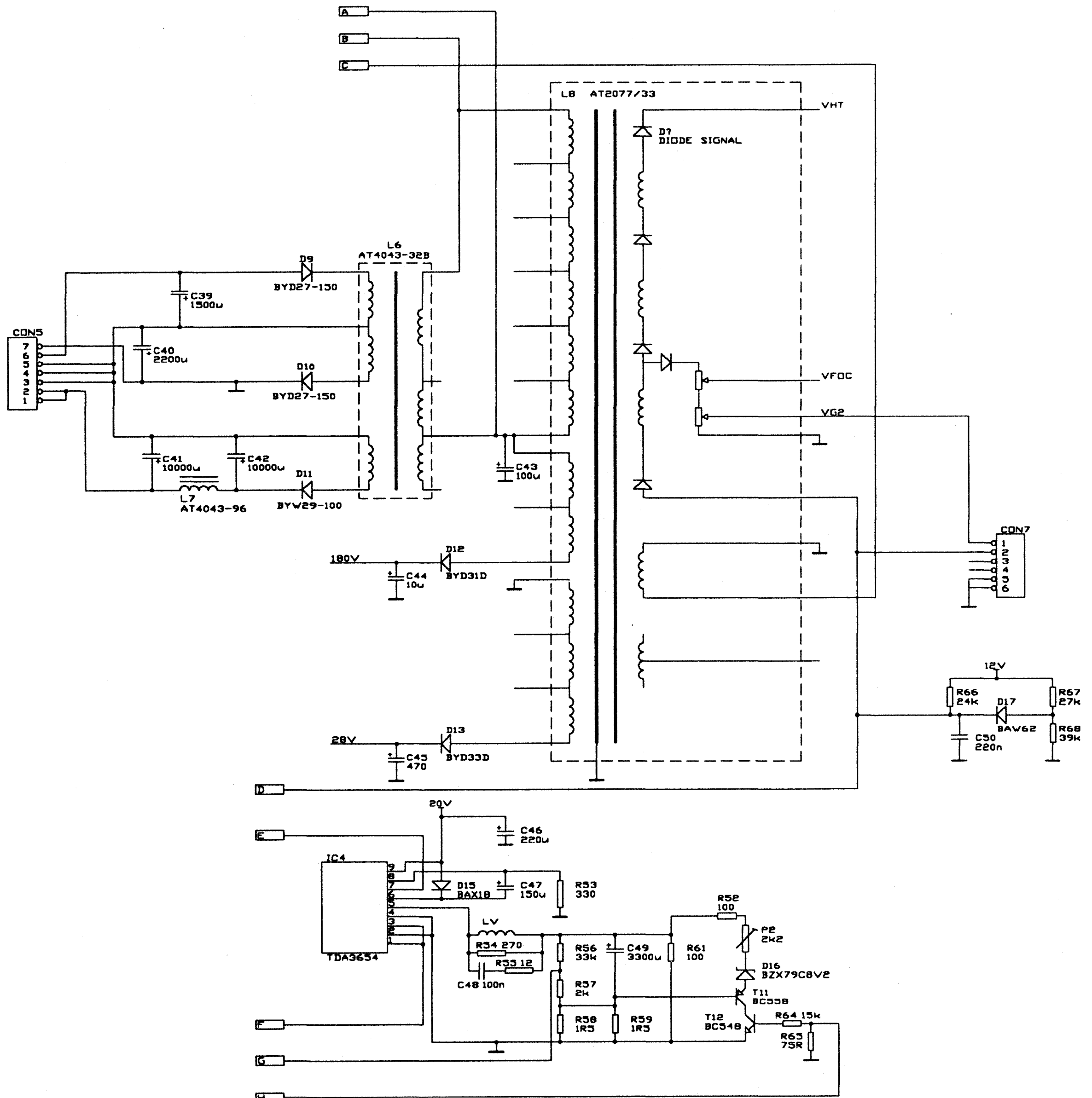


Fig.7.1 (continued from previous pages)

Appendix A

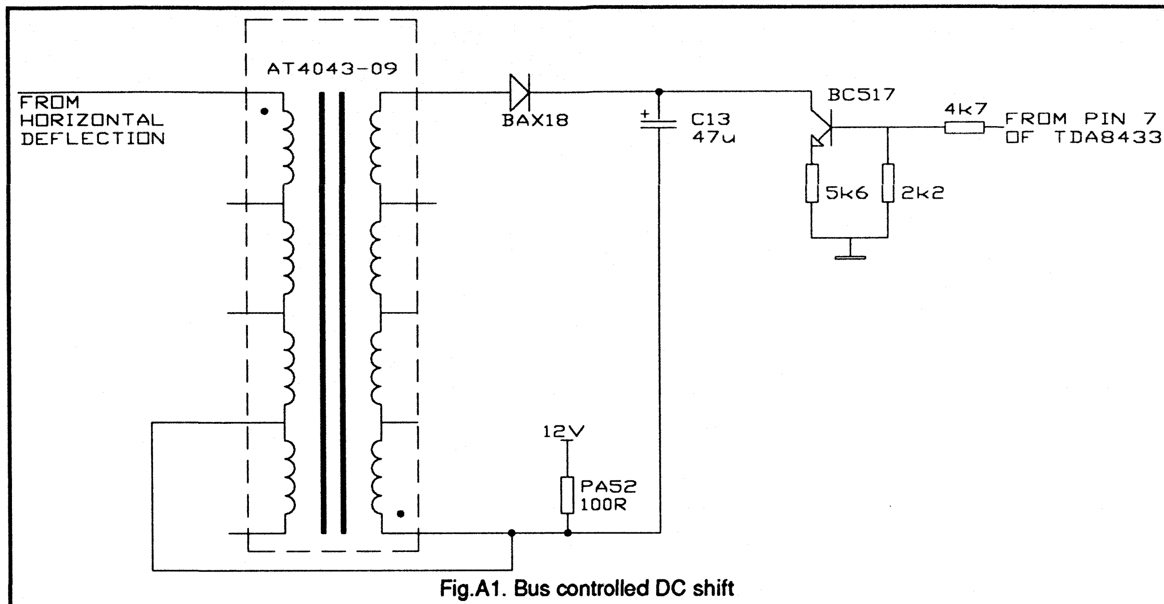


Fig.A1. Bus controlled DC shift

The deflection processor TDA8433 has three DACs. In this application only one DAC (DAC-A) is used. In this section some ideas are given to use the other two DACs.

DAC-B is a 6 bits DAC like DAC-A and is controlled by the H-PHASE register. Its output voltages can be controlled from 0.5V to 10.5V typically. Output resistance <1kΩ.

DAC-C is a two bit DAC and is controlled by the VTRA and VTRC bits. Its typical output characteristic is:

VTRA	VTRC	Output voltage	Output resistance
0	0	12V	7.5KΩ
0	1	5.3V	3.3Ω
1	0	1.7V	1.0KΩ
1	1	0.3V	<1KΩ

All settings in the set that are now manual controls can be made I²C bus controlled by using one of these DACs. The only restriction is that the alignment is controllable with a DC voltage. Otherwise an interface circuit is needed.

Appendix B

As a degaussing circuit the following suggestion is given.

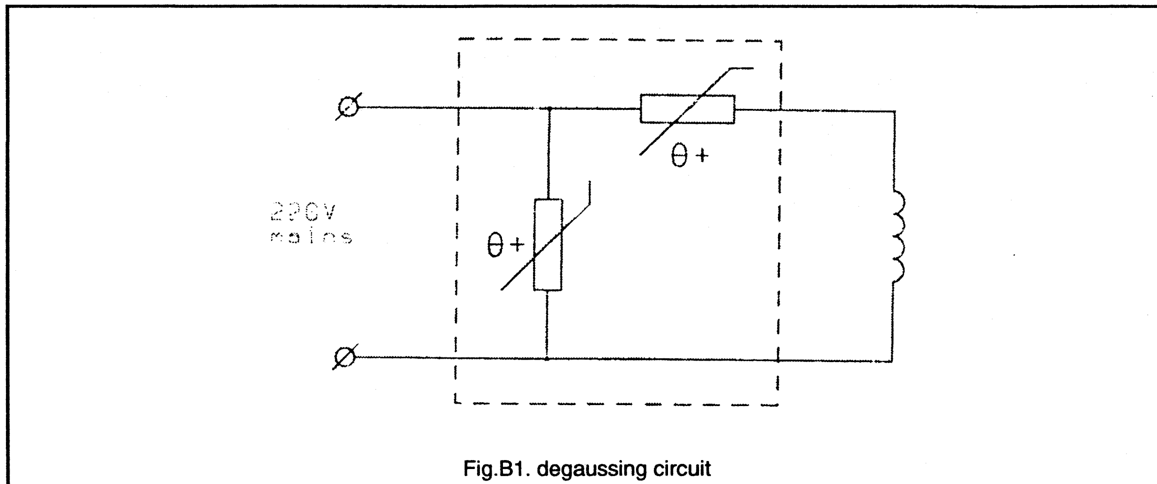
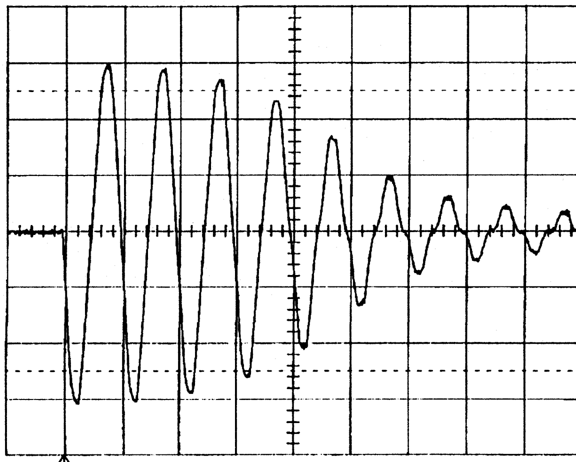


Fig.B1. degaussing circuit

Parts list:

Dual degaussing PTC	:	2322 662 96116
Degaussing coil	:	3111 268 20301 1x



Oscillogram 10:

Current is degaussing coil 2A/div.

SMPS Circuit Examples

4.3.1 70W Full Performance TV SMPS Using The TDA8380

The following report describes the operation of a 70W full performance switched mode power supply for use in television.

The TDA8380 SMPS control IC is used in a mains isolated, asynchronous flyback converter configuration.

The power supply incorporates the following features:

- Full mains range (110-265 Vrms)
- AT3010/110LL SMPS transformer
- BUT11A switching transistor
- Standby (suppression of output voltages by 50%)
- Standby supply (5V, 100 mA)
- Facility for synchronisation (using a pulse transformer)
- Short start-up time (less than 0.3 sec at 220 Vrms)
- Provision for anti-breathing circuit
- Output voltages 147V/57W, 25V/5W, 16V/7.5W

A full description of circuit operation, a circuit diagram and circuit performance figures are given.

A further additional circuit diagram is included in which the above power supply incorporates a Power MOS switching transistor for a mains range of 90-135 Vrms. Also details are given on an extension to the power capability of the supply, up to 120W output, for European mains using the bipolar switching transistor.

1. Introduction

The TDA8380 control IC has been designed to enable safe, reliable and efficient SMPS to be realised at minimum cost for TV and monitor applications. For further information on the IC reference should be made to 'Integrated SMPS control Circuit TDA8380' (ref. 1).

The 70W design employs a currently available AT3010/110LL foil wound transformer and the BUT11A bipolar switching transistor.

Feedback is taken from the secondary side to give less than 1% line and load regulation over the whole range. The output voltage is suitably divided down and compared in an error amplifier with a fixed reference voltage. The error amplifier then drives an optocoupler, which passes the error signal to the primary side directly into the TDA8380. A secondary side error amplifier is used to reduce the importance of the optocoupler characteristics.

Standby is achieved by injecting a signal into the feedback loop on the secondary side, suppressing all output voltages by 50%. A 5V standby supply is available relieving the need for a separate standby supply. During standby conditions the line output oscillator is halted to disconnect the main B+ load.

Synchronisation of the power supply to external control circuits is possible through a loosely coupled pulse transformer.

Appendix A gives a circuit diagram and a short description of the use of the Power MOS switching transistor in the 70W supply. The mains range is 90-135 Vrms.

Appendix B gives notes on how to extend the power capability of the 70W power supply to 105W, 32 kHz and 120W, 30 kHz. Both these power supplies have a mains range f 180-265 Vrms.

2. TV SMPS design

Flyback versus Forward Converter:

Whereas this IC can be applied in any type of SMPS, for example in FORWARD (or Buck) or FLYBACK (or Buck-boost) converters, the preferred SMPS type for TV applications is the Flyback converter. This is mainly because it allows for mains isolation of the TV chassis. Other advantages it affords in comparison with a forward converter are:

(a) It does not need 'crow-bar' protection against the input voltage appearing across the chassis in the event of short-circuit failure of the power switching transistor.

(b) The load permissible on auxiliary output supplies is not related (and therefore not limited) by the main line timebase supply (B+ voltage) load. Thus the auxiliary supply is available when there is no B+ voltage load, and this is important for servicing and fault finding on a TV chassis.

With the Flyback converter, however, mains pollution and visible interference require to be minimised by careful PCB layout and customarily a mains input filter is used.

Discontinuous versus Continuous Current Mode Operation:

Operation can be in the 'continuous' or in the 'discontinuous' current mode.

In the discontinuous mode the power switching transistor is not allowed to switch on until the SMPS transformer core is demagnetised. This has the advantages:

(a) It is inherently a safer mode of operation, since for all operating conditions, other than a dead-short of the output or a very severe overload transient occurring when the power transistor is conducting near peak current, it is not possible for the core to saturate. To protect for these two exceptions, the very fast (second level) current protection is included.

(b) Steep current pulse edges at switch-on are eliminated (important from point of view of Radio Frequency Interference problems).

Satisfactory performance, in terms of voltage regulation and input mains voltage range, can be obtained using the discontinuous mode which is therefore preferred for TV applications.

For this type of converter, the voltage transfer function can be deduced from the Volt-second equilibrium condition for a unity turns ratio transformer:

$$Vi \times d \times T = Vo \times \overline{d} \times T$$

$$\frac{Vo}{Vi} = \frac{d}{\overline{d}} \qquad (1)$$

where: $\overline{d} = (1 - d)$

Taking into consideration the transformer turns ration n = Np/Ns, then:

$$\frac{n \times Vo}{Vi} = \frac{d}{\overline{d}} \qquad (2)$$

where: T = oscillator period
Np = transformer primary turns
Ns = transformer secondary turns
d = on time of output transistor
$\overline{d}$ = conduction time of output rectifier
Vo = output B+ voltage
Vi = input DC voltage

The limit condition for 'discontinuous' current mode operation occurs at minimum input voltage and maximum load.

Thus, for this condition $\overline{d} = (1 - d)$
so that

$$\frac{n \times Vo}{Vimin} = \frac{dmax}{(1 - dmax)} \qquad (3)$$

The power output (including losses supplied via the transformer) is:

$$P = \frac{Vi^2 \times d^2}{2 \times Lp \times f} \qquad (4)$$

where: Lp = primary inductance of transformer
f = frequency of operation

from which general expressions for d, Lp and f can be obtained in terms of the power.

Thus, for a given transformer (n,Lp) the value of dmax can be calculated from (3) and the required frequency of operation from:

$$f = \frac{dmax^2 \times Vimin^2}{2 \times P \times Lp} \qquad (5)$$

The peak current in the power switching transistor is given by:

$$Ip = \frac{Vi \times d}{Lp \times f} \qquad (6)$$

The peak voltage across the power switching transistor (excluding ringing) is:

$$Vi + (n \times Vo)$$

Since most transformers produce ringing, a clamp circuit may be necessary and in order to slow the rising edge of the voltage a snubber circuit is usually required.

3. General circuit description

This section gives an overall general description of the power supply.

Figure 1 gives a block diagram of the circuit functions. Description of specific circuits will be carried out in the next section.

3.1 Mains filter

This is positioned at the AC mains input. Its function is to minimise mains pollution resulting from RFI generated within the SMPS due to fast transients of voltage and current. It is designed to meet the required mains pollution regulations (C.I.S.P.R. Special Committee on Radio Frequency Perturbation).

3.2 Rectification and Smoothing

The mains voltage is rectified and smoothed to provide a DC supply which is switched through the SMPS transformer.

3.3 SMPS Controller

This drives the power switching transistor regulating the frequency and the amount of current pulsed through the transformer primary. Thus, the controller regulates the energy transferred to the secondary windings. A voltage feedback signal which is representative of the output voltage is fed back to the controller in order to regulate the output voltage. At start up the supply voltage for the controller IC is derived from the rectified mains. A 'take-over' winding on the transformer supplies the IC once normal operation is established.

3.4 Transformer secondary circuits

The DC output voltage is obtained by simple rectification and smoothing of the transformer secondary voltage.

3.5 Feedback Attenuator

The output voltage to be regulated is fed back via an attenuator to the error amplifier.

3.6 Error Amplifier

The error amplifier compares the feedback signal with a fixed reference voltage to give an error signal which is passed to the primary side via an optocoupler.

Mains isolation is provided within the optocoupler and the power transformer, between the input primary and take-over, and the output secondary windings.

4. Detailed circuit description

This section gives a detailed description of each of the functions of the power supply circuit (Fig. 2).

4.1 Mains Input and Rectification

Diodes V1 to V4 rectify the AC mains voltage and, together with a smoothing capacitor C13, provides a DC input HT voltage for the SMPS. R1 is placed in series with the input to limit the initial peak inrush current whenever the power supply is switched on when C13 is fully discharged.

C1 and C3 together with L1 form a mains filter to minimise the feedback of RFI into the mains supply.

C6 to C9 suppress RFI signals generated by the rectifier diodes.

Asymmetrical mains pollution is reduced by the insertion of R26 and C18 between primary ground ('hot side') and secondary earth ('cold side') of the power supply. These components are required to satisfy the mains isolation requirements.

4.2 Control IC TDA8380

This section describes the function of each pin of the TDA8380 and its associated components.

Pin 1 - Emitter of Forward Drive Transistor:

The TDA8380 incorporates a direct drive output stage consisting of two NPN transistors. The collector and emitter of each are connected to separate pins of the IC (pins 1,2,15,16). The forward base drive current for the switching transistor is limited by R15. C16 acts as a voltage source equal to the zener voltage of V7 and is used for the negative base drive.

When the reverse drive transistor is turned on the zener voltage appears across L2, causing stored charge to be removed from the switching transistor, thereby ensuring correct storage time and minimum transistor dissipation during turn-off.

Pin 2 - Collector of the Forward Drive Transistor:

Connected through a resistor to the IC reservoir capacitor.

Pin 3 - Demagnetisation Sensing

Demagnetisation protects the core of the transformer against saturation by sensing the voltage across a transformer winding. In this application operation is in the discontinuous current mode. Sensing is achieved by resistor R10 from the take-over winding of the transformer to pin 3 of the IC. Figure 3 illustrates demagnetisation operation at low mains where the turn-on pulse is delayed until demagnetisation of the transformer is complete.

Pin 4 - Low Supply Trip:

Connected to the IC ground (pin 14), the low supply protection level is 8.4V.

Pin 5 - IC supply:

On power-up the IC supply is firstly drawn from C15. This capacitor is charged up directly from the rectified mains through bleed resistors R21 and R24.

Once the SMPS is running, the supply for the IC is taken over by the SMPS transformer. R12 prevents peak rectification of spikes. V8 rectifies the flyback signal which is smoothed by C15 to give a DC level. R16 limits the current drawn by the forward drive transistor. R9 and C5 provide a filtered DC supply to pin 5 of the IC.

Pin 6 - Reference Current:

This pin allows the external setting of the IC current source. This is set by R11.

Pin 7 - Voltage Feedback:

This is the input to the internal error amplifier for primary side feedback. Feedback in this case is taken from the secondary side and passed through a separate secondary side error amplifier where it is compared with a reference voltage. The error signal is then passed directly into the duty pin (pin 9) via an optocoupler.

To ensure that the Transfer Characteristic Generator (TCG) in the IC remains optional a 'pseudo' feedback voltage from the take-over winding of the SMPS transformer is applied to pin 7. R3 and R4 provide a nominal 2.5 V level at pin 7 during normal operation of the power supply.

Pin 8 - Stability:

This is the output of the error amplifier which is left open circuit.

Pin 9 - Duty:

This is the input to the pulse width modulator and is directly driven by the optocoupler transistor. R2, C2 and C27 form a frequency compensation network.

Pin 10 - Oscillator:

The frequency of the internal oscillator is set here by C4 and R11 on pin 6 (nominally 25 kHz).

Pin 11 - Synchronisation:

This is achieved by a loosely coupled pulse transformer passing sync pulses from the secondary to the primary side of the power supply (see later section).

Pin 12 - Slow Start:

The slow start option is selected here by the use of capacitor C11. Figure 4 shows a typical slow-start.

Pin 13 - Over-Current Protection:

To keep the collector current of V10 within safe operating limits over-current protection is incorporated into the power supply. R27 is the collector current monitoring resistor providing a negative going signal. This voltage is then shifted to a positive level with respect to ground potential by a reference current from the IC flowing through R14. An extra voltage shift is provided by R34 which varies with the IC supply voltage. This is particularly useful in output short circuit conditions. If the main regulated output is progressively short circuited, then all SMPS transformer flyback voltages will decrease respectively and hence the shift level of the current protection function leading to lower short circuit output currents (current foldback). The signal at pin 13 is then compared with two internal voltage levels to provide the two forms of current protection.

(The addition of R34 may not work in other power supplies using the TDA8380 because careful attention has to be given to the ratio of current through R34 to current output at pin 13 and to the start-up sequence of the power supply at different mains and loads. Conventional current protection can be achieved by omitting R34 and changing R14 to 13 kΩ and V13 to BYW95C).

Figure 5 illustrates the current protection waveform.

Pin 14 - Ground

Pin 15 - Emitter of Reverse Drive Transistor:

Grounded to the emitter of the switching transistor.

Pin 16 - Collector of reverse drive transistor.

4.3 Error Amplifier

The external error amplifier consists of two PNP transistors, V15 and V16, connected to form a high gain comparator. The stabilized reference voltage for the comparator is derived from a series-connected resistor R28 and zener diodes V5 and V6 at the SMPS output. The voltage to be compared with the reference voltage is a sample of the 147 V output derived from a potential divider (R29, R31 and R5). The optocoupler is directly driven with the error signal from the comparator. The level of the 147V output can be adjusted by R5.

4.4 Standby

In standby mode the power supply output voltages are suppressed to 50% of their normal level. Standby is achieved by reducing the reference voltage used in the comparator circuit and thus the power supply regulates at a lower output voltage level. A +5 V DC level is applied to the standby input, which turns transistor V14 on. The voltage reference level is halved from 12.4V to 6.2V and the main 147 V output is reduced to 75V. In this condition the power supply still maintains a 5V standby supply. In the television receiver during standby the line output oscillator should be halted to disconnect the main 147 V load.

To return the power supply to its normal operating levels, the standby input is removed.

The speed of transition to and from standby is controlled by the time constant of R13, R32 and C23.

4.5 Synchronisation

Synchronisation of the power supply is achieved by a loosely coupled mains isolated pulse transformer. +5V sync pulses are applied to the sync input at a frequency slightly lower than the free running frequency of the power supply. R6 limits the current in the primary winding of the pulse transformer and R8 loads the secondary winding. The pulse transformer differentiates the sync pulse input to create negative and positive going transitions of the sync input. The AC coupling (C14) shifts the entire signal positive and the internal circuitry of the IC clamps the negative going excursions to 0.85V. The positive going spikes are removed

by a transistor in the IC and the negative going spikes are used to synchronise the oscillator. Figure 6 shows plots of how the power supply is synchronised to a lower frequency.

A series RC network (C28, R35) is connected from pin 11 to ground to filter out high frequency noise which may interfere with synchronisation.

If the synchronisation option is not to be used, the sync input may be left open circuit. Another alternative is to short-circuit C14 and remove T2.

4.6 Beam Current Limiting (BCL)

Anti-breathing technique, whereby the 147V voltage is reduced for increasing beam current in such a manner as to compensate for the increase in picture size due to the fall in EHT. The components concerned are R30, C24, R7.

4.7 Power Switching Transistor

Pulsing of the transformer is carried out by the BUT11A bipolar power transistor under the control of the TDA8380 IC.

Figure 7 shows plots of the current through and voltage across the BUT11A. The base drive waveform is shown in Fig. 8 (a) and Fig. 8 (b) during standby conditions.

Figure 9 is a plot of the instantaneous power dissipated in the transistor during turn-off.

4.8 Damping Network

A damping network has been added across the switching transistor to protect the transistor from excessive switching dissipation and to suppress ringing on the SMPS transformer.

The dV/dt limiter consists of V9, C17, R22 and R23. When V10 is switched off, part of the energy stored in the leakage inductance of the SMPS transformer will charge C17. When V10 is switched on again this energy is dissipated in R22 and R23. When such a network is omitted, this energy must be dissipated in the switching transistor itself.

R22 and R23 are calculated in such a way that they also act as a network, damping the residual energy in the winding capacitance of the transformer when the secondary rectifiers have stopped conducting.

4.9 Outputs

There are three secondary rectifiers; the 147V (scan voltage for deflection stage), 25V (audio supply) and 16V (small signal supply). The 5 V standby supply is derived from a regulator connected to the 16V output.

R25 and C25 form a damping network to dissipate the energy in the high frequency ringing on the B+ secondary winding. Figure 10 shows the current through and voltage across the B+ winding.

Short circuit or overload of these outputs will cause the power supply to repeatedly go through the slow start procedure.

5. Performance specification

Mains input:		110-265 V AC	50 Hz-60 Hz
Outputs:	B+	147 V	57 W
	Audio	25 V	5 W
	L.T.	16 V	7.5 W
	Standby	5 V	0.5 W
Switching frequency:			25 kHz
Efficiency (normal operation):			72 %
Line and load regulation:			0.1 %
Start-up time (220 Vrms, full load):	300 msec (B+) 225 msec (+5 V standby)		
Max. collector current:	2.3 A		
Max collector voltage:	870 V		
Forward base current:	Normal operation		0.30 A min. 0.39 A max.
	Standby (*)		0.20 A min. 0.24 A max.
I.C. supply voltage:	Normal operation		18.5 V min. 21.0 V max.
	Standby (*)		8.8 V min. 9.7 V max.

Ripple output voltage (110 Vrms, 50 Hz, full load):

Frequency	B+ (mV)	L.T. (mV)	Audio (mV)	Standby (mV)
25 kHz	600	230	145	20
199 Hz	230	50	60	-

* The only load in this condition is the standby load.

6. Output short-circuit foldback

The SMPS incorporates duty factor foldback protection for short circuits on the 147 V (B+) output. Figure 11 shows the plot of the foldback characteristic for increasing load on the 147 V output using conventional protection and current foldback techniques.

8. References

Ref. 1. "Integrated SMPS Control Circuit TDA8380". Philips Components Publication Number 9398 358 40011
December 1988.

Appendix A

70W FULL PERFORMANCE USING POWER MOS (BUK456-800A)

A Power MOS switching transistor was incorporated into the 70W power supply design. This new power supply has a mains range of 90-135 Vrms. A circuit diagram is given in Fig. 12. Oscillograms of the Power MOS gate and drain switching waveforms are given in Figs. 13 and 14.

Alterations to Existing 70W Bipolar Transistor Design

(i) The value of C17 in the snubber is smaller, hence less dissipation in the snubber resistors. The dV/dt at the drain is now higher, but the Power MOS transistor has much lower switching losses than the Bipolar transistor.

The smaller value of C17 causes the 100 kHz ringing on the primary winding of the SMPS transformer after flyback to be more prevalent. This ringing has an effect on the demagnetisation function causing premature operation. To overcome this a resistive divider network has been used on pin 3 to minimise the effect of ringing.

(ii) The value of R14, the current protection shift register, is increased. This is to compensate for the fact that the Power MOS transistor does not suffer from storage effects at turn-off.

(iii) The filtering on the take-over winding for the IC supply is increased. This is because the average current demanded by the gate drive of the Power MOS is much less than in the case of the Bipolar transistor. Energy in switching spikes on the flyback voltage cannot be channelled into the gate of the Power MOS and so has to be dissipated in increased filtering.

A smaller value for the gate-source resistor is used to provide extra loading on the transformer winding.

(iv) C13 is increased to filter the higher current ripple at low mains voltages.

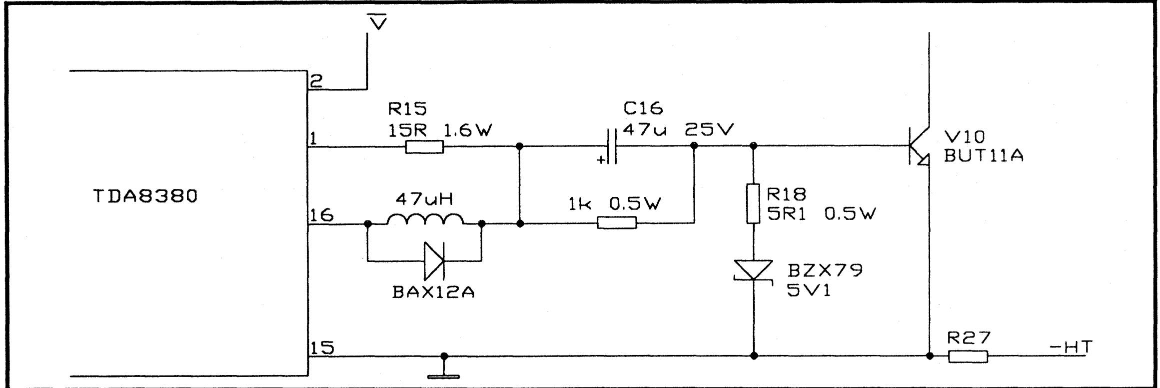
(v) A larger heatsink for the switching transistor is necessary due to the higher on-resistance of the Power MOS transistor facilitating the need for higher heat dissipation.

Performance Specification

Mains supply:	90-135 Vrms		
Switching frequency:	20.8 kHz		
Outputs:	B+	147 V	57 W
	Audio	25 V	5 W
	L.T.	16 V	7.5 W
	Standby	5 V	0.5 W
Regulation:	0.1 %		
Peak drain voltage:	650 V		
Peak drain current:	2.3 A		
Start-up time	300 msec		

Addendum

Alternative Cheap BUT11A Base Drive Design Eliminating 5 W Zener Diode



An alternative base drive for the power switching transistor (BUT11A) has been designed to eliminate the 5 W zener diode 1N5339B (V7) to reduce cost.

Alternative Low Cost Base Drive

This design has not been implemented into a PCB design yet, but the existing PCB design requires little alteration to accommodate the changes.

When the forward drive resistor is turned on at the start of the duty cycle, a current defined by R15 passes through C16 and into the base of the BUT11A. The 1 kΩ resistor in parallel with C16 discharges the capacitor when the SMPS is off to help starting at low mains. When the reverse drive transistor is turned on, the 5.1 V zener diode appears across C16 clamping the voltage across it, thus a reverse current flows from the base of the BUT11A through C16 and L2 turning off the power switching transistor. Some forward current does flow through the 5.1 V zener diode, but not enough to warrant a power zener. The BAX12A diode across the inductor is to prevent large negative going spikes from appearing at pin 1 of the i.c.; this can also be used in the previous base drive.

Base Measurements

Forward base current:	250mA min 400mA max
Standby mode (standby load only)	190mA min 250mA max
BUT11A storage time:	1.4µsec

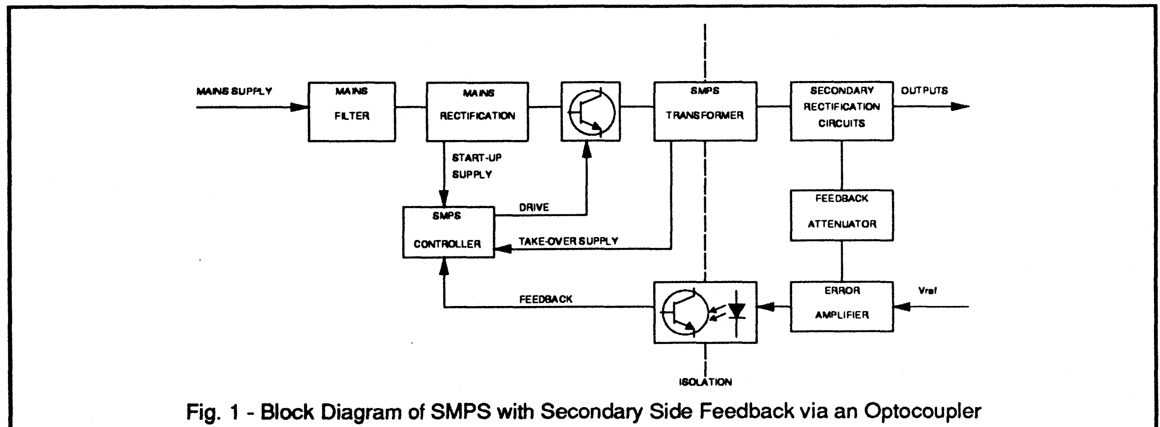


Fig. 1 - Block Diagram of SMPS with Secondary Side Feedback via an Optocoupler

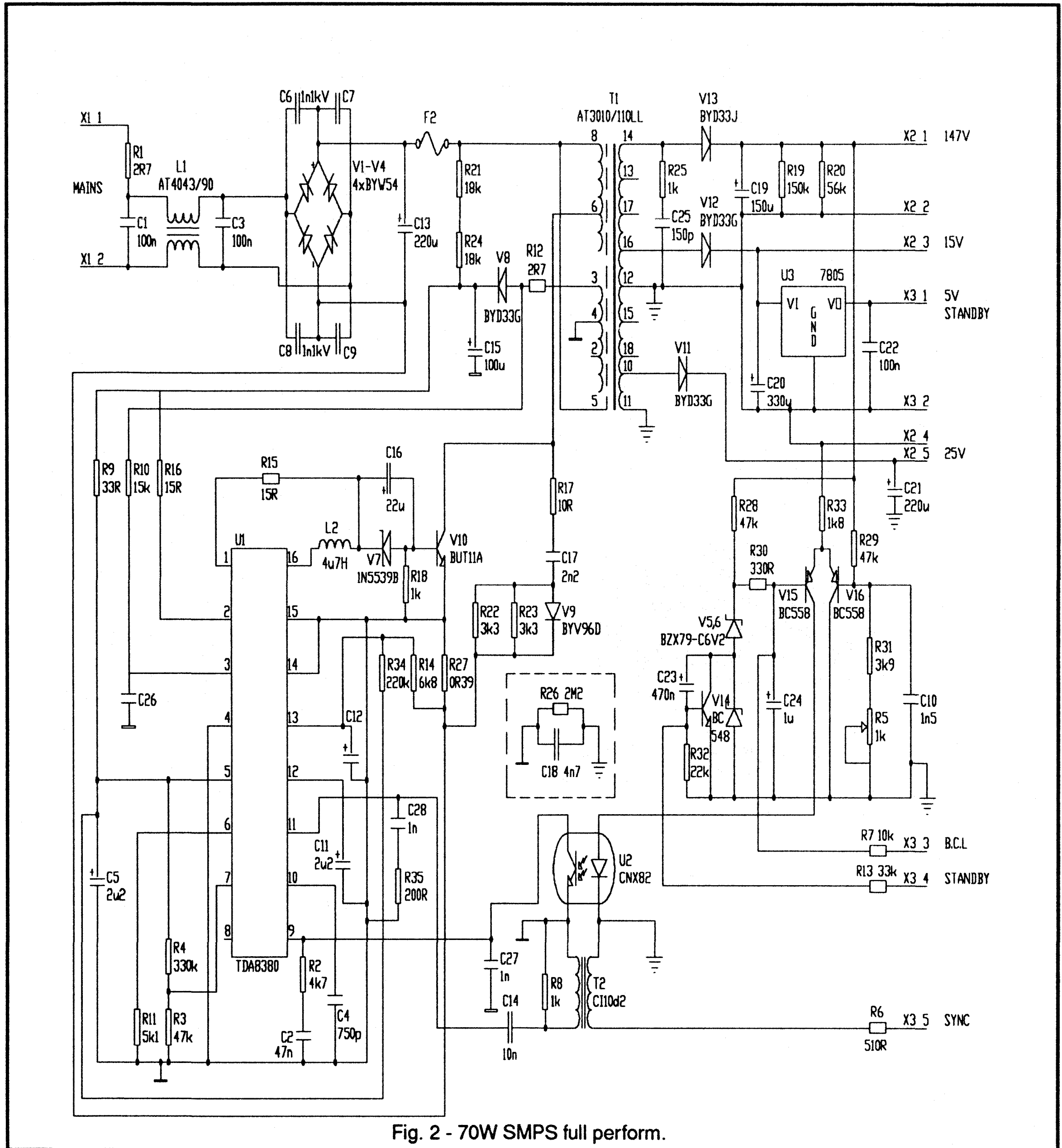


Fig. 2 - 70W SMPS full perform.

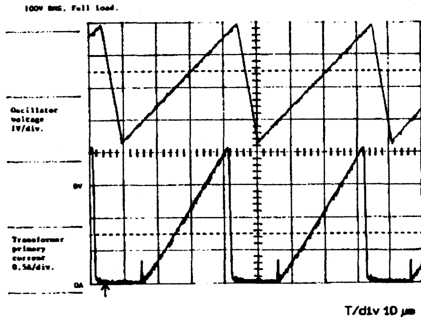


Fig. 3 - Demagnetisation operation. Oscillogram of the Oscillator Waveform and Transformer Primary Current

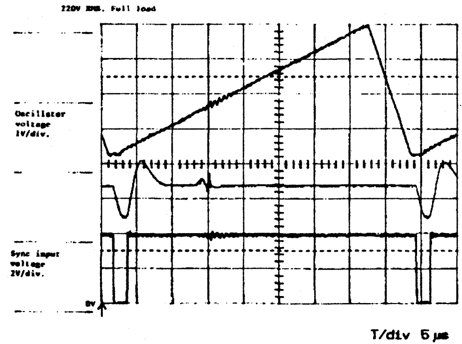


Fig. 6 - Synchronisation. Oscillogram of Oscillator Voltage, Voltage at Pin 11 (TDA8380) and Sync Input Voltage

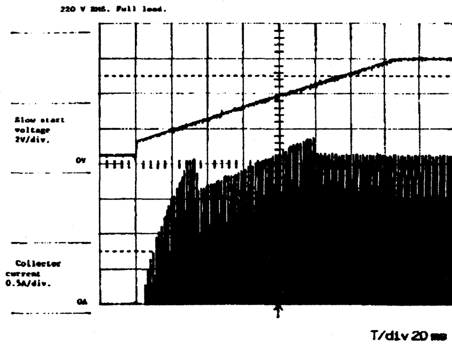


Fig. 4 - Slow Start. Oscillogram of the Voltage at the Slow Start Pin (TDA8380) and Current through the Switching Transistor.

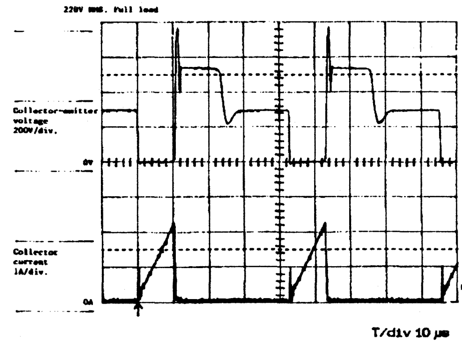


Fig. 7 - Switching waveforms. Oscillograms of the current through and voltage across BUT11A.

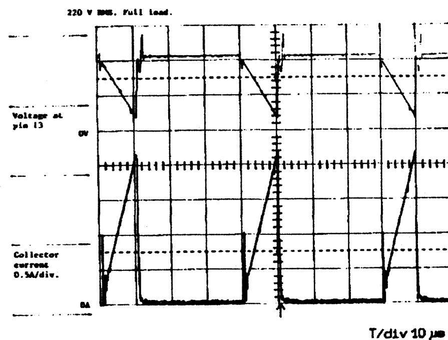


Fig. 5 - Current protection. Oscillogram of voltage at Pin 13 (TDA8380) and the Current through the Switching Transistor

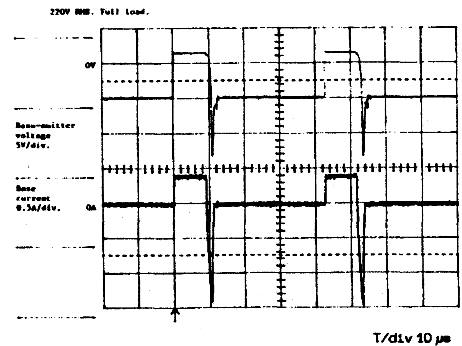


Fig. 8(a) - BUT11A Base Waveforms. Oscillograms of Base-Emitter Voltage and Base Current Waveforms for BUT11A

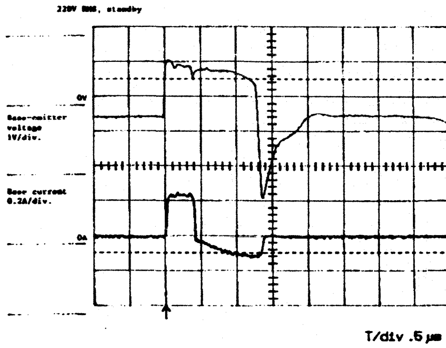


Fig. 8(b) - BUT11A Base Waveforms During Standby. Oscillograms of Base-Emitter and Base Current Waveforms for BUT11A in Standby Conditions

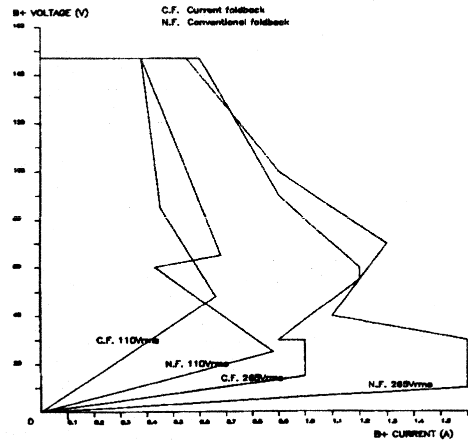


Fig. 11 - Plot of Duty Factor Foldback using Current Feedback and Conventional Foldback Techniques

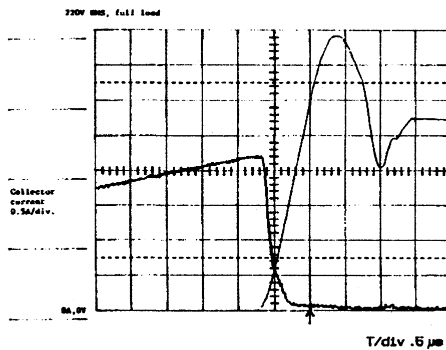


Fig. 9 - Turn off dissipation in BUT11A. Oscillogram of Collector-Emitter Voltage and Collector Current for BUT11A

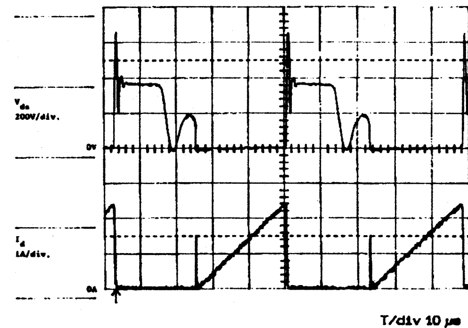


Fig. 13 - Oscillogram of Drain-Source Voltage and Drain Current for Power MOS Transistor (BUK456-800A) at Full Load 110 V RMS

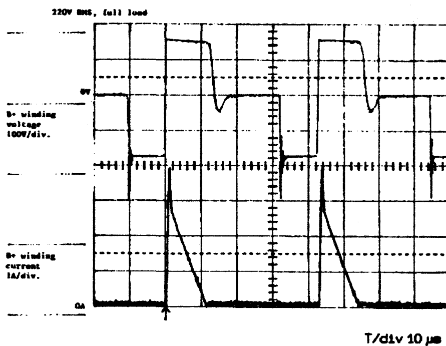


Fig. 10 - B+ Winding. Oscillogram of Voltage Across and Current Through the B+ Winding

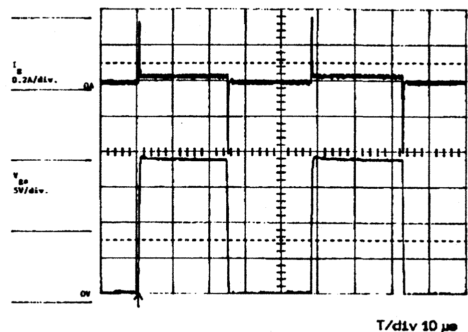


Fig. 14 - Oscillogram of Gate Current and Gate Source Voltage for Power MOS transistor (BU456-800A) at full load, 110 V RMS

Fig. 12 - 70W SMPS Full performance.

4.3.2 Synchronous 200W Switched Mode Power Supply For 16 and 32 kHz TV

Description of 200W Switched Mode Power supply incorporating the AT3020/01A transformer, the TDA8380 control IC, one opto-coupler for feedback, synchronisation and remote on/off. The SMPS is intended for TV and can be synchronised to 32kHz by flyback pulses of either 32 or 16 kHz. Standby supply is also provided.

1. Introduction

In this report a description is given of a 200W SMPS circuit and evaluation board, incorporating the TDA8380 control IC, the new SMPS transformer AT3020/01A and the BUW13 power switching transistor. The SMPS is a flyback converter has been designed to handle a maximum average output power of 200W and a peak power of 250W. The free running frequency of the SMPS is 34kHz, while it can also be synchronised down to 32kHz by either 16 or 32kHz line flyback pulses. For testing purposes no pre-loading is required. The circuit operates at a mains input voltage of 185-265VRMS, 50-60Hz. The output voltages are 150V, 32V and 16V. The 150V output is short circuit proof, while the 32V and 16V can be made short-circuit proof.

A new wire wound SMPS transformer has been designed. This transformer, the AT3020/01A with an EE46/46/30 core (grade 3C85), has a new winding technique which makes the RFI screens superfluous. Thanks to its low leakage inductance, the efficiency of the system is high (88%).

The control IC TDA8380 receives its start-up supply from the rectified mains voltage. The takeover supply is derived from a flyback and forward auxiliary winding on the transformer. This IC offers many attractive operating facilities. It directly drives the power switching transistor and incorporates several overload protections.

Due to its high current gain, the BUW13 was chosen as power switching transistor. For an output power of up to 150W, the BUT12 can be used. A CNG82 opto-coupler is used for feedback. If synchronisation is not required, the cheaper CNX82A can be used.

For the supply of some digital IC's in the standby mode, a small self-oscillating supply is used: the so called µSOPS (5V/300mA). In the standby mode the output voltages will be fully suppressed.

A printed circuit board (no 3634) is available incorporating the 200W SMPS and µSOPS but without mains filter.

2. Circuit description

2.1 Block Diagram

Figure 1 shows the block diagram of the 200W mains isolated flyback converter.

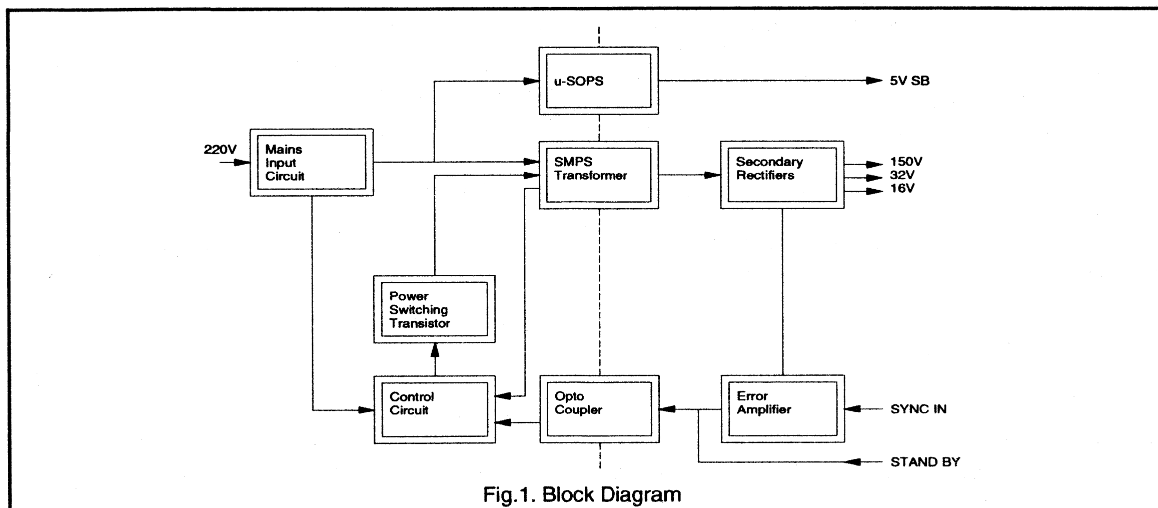


Fig.1. Block Diagram

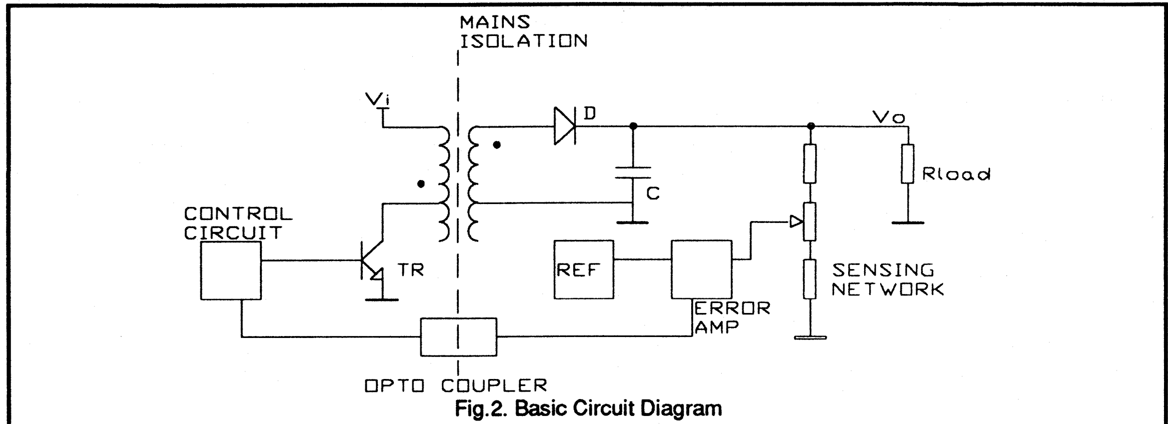


Fig.2. Basic Circuit Diagram

The 200W SMPS evaluation board does not contain an RFI filter, fuses or a degaussing circuit. These components should be located on the inlet of the mains cord into the TV set. The mains input voltage is rectified by bridge rectifying diodes and the DC supply to the SMPS transformer (AT3020/01A) is smoothed by a 220 µF buffer capacitor. The control IC TDA8380 derives its start-up supply from this DC voltage and as soon as the IC supply voltage exceeds a certain limit, the IC is initialised. Hereafter the duty factor of the SMPS power switching transistor (BUW13) increases slowly from zero onwards and its rate of increase is controlled until the SMPS output voltage reaches its nominal level. The take over supply is derived from a flyback and forward rectifier connected to an auxiliary winding of the SMPS transformer. The SMPS is a flyback convertor that operates in the interrupting current mode. At the secondary side the flyback voltage is rectified. One of the output voltages is fed back via an attenuator circuit to the error amplifier. The error signal is sent back via the opto-coupler circuit to the duty cycle control input of the IC TDA8380.

For standby purposes the µSOPS delivers a 5V supply. In the standby mode the output voltages will be fully suppressed. The SMPS is running at a fixed frequency of 34kHz. However it can also be synchronised down to 32kHz by either 16 or 32kHz line flyback pulses.

2.2 Basic Operation

Fig.2 shows the basic circuit of the mains isolated flyback converter.

The control IC TDA8380 directly drives the power output transistor. When the transistor conducts, a linear increasing current flows through the primary winding of the transformer. As a consequence energy is stored in the transformer. After switching off the transistor, the stored energy is transferred into the load via diode D. The attenuated output voltage Vo is compared with the reference voltage in the error amplifier. The error signal is fed back via the opto-coupler to the control IC. By controlling the duty cycle of the drive pulses the output voltage Vo is kept constant.

The flyback converter under discussion has been designed for the discontinuous current mode. The principle of this circuit has already been described in several reports [1]. For a nominal output voltage of 150V, $V_{mains\,min}$ = 185Vrms, a maximum load of 250W and a fixed free running frequency of 34kHz, the primary inductance of the transformer can be calculated. The required primary inductance is Lp = 420 µH ± 10%.

An attractive facility of this SMPS is that it can be synchronised down to 32 kHz by either 16 or 32 kHz line flyback pulses.

3. Circuit diagram

The circuit diagram is given in Fig.3. In this chapter detailed information is given of about several parts of the supply.

3.1 Mains input

Diodes D1 to D4 bridge rectify the mains input voltage and the DC supply to the SMPS is smoothed by C5. Capacitors C1 to C4 suppress the RFI generated by the diodes in the mains bridge rectifier. If C5 is fully discharged, the inrush current has to be limited by R1 to protect the bridge rectifier diodes. During continuous operation of the SMPS this resistor is for efficiency reasons short circuited by thyristor

THY1. After the soft start of the SMPS, thyristor THY1 is fired continuously by the peak voltage clamp of the SMPS via R3 and C6.

3.2 Start up supply

The control IC TDA8380 receives its start-up supply from the mains rectified voltage by the low wattage resistor R4. The IC is initialised as soon as the voltage on the supply pin 5 reaches 17V. This takes approximately 1.5s (Oscillogram 6). Shorter times are possible by lowering the value of R4. During the time leading up to the initialisation of the IC, the base coupling capacitor C10/C11 is pre-charged. So the power switching transistor T1 is switched off correctly during the start up period. With a duty cycle from zero onwards, the SMPS starts up. The take over supply is derived from a forward and flyback auxiliary winding on the transfomer (AT3020/01A). The forward rectifying diode D7 ensures that a temporary decrease of the supply voltage of the IC is restricted. After a while the flyback rectifying diode D6 directly provides all the current needed by the IC. During continuous operation of the SMPS the supply voltage for the IC is about 17V.

3.3 Control IC

The integrated SMPS control circuit TDA8380 offers many attractive operating facilities. Its controls the SMPS power throughput and regulation by pulse-width modulation. It can directly drive the power switching transistor and it can operate at a fixed frequency or a line locked frequency. A detailed description is given in Reference [2]. The function of each pin is described below.

Pin 1 Emitter of the forward drive transistor. It directly drives the power transistor with a source current of about 0.7A.

Pin 2 Collector of the forward transistor. This pin is connected via R14 to the supply. Resistor R14 and R15 mainly determine the source current of the power switching transistor.

Pin 3 Demagnetisation sensing. For this flyback converter, operating in the discontinuous current mode, the voltage across the SMPS transformer is sensed via R12 and R13.

Pin 4 Low supply-voltage protection level. This pin is connected to ground, so the V_{ccmin} of the IC is set at 8.4V.

Pin 5 IC supply. When the mains input is applied to the SMPS, the IC supply reservoir capacitor C9 is charged by a current determined by resistor R4. When the voltage at pin 5 reaches 17V, the IC initialises and diode D6 rectifies the flyback signal from winding 10/11 of the SMPS transformer to supply the IC with 17V.

Pin 6 Master reference current setting. Resistor R11 sets the master reference current for the TDA8380 to 600 μA.

Pin 7 Voltage feedback and overvoltage protection. The flyback signal from winding 10/11 of the SMPS transformer is smoothed by D6/R7/C9, to give a DC level that varies in proportion to variations of the 150V output from the SMPS. This level is reduced by the divider R9/R10 and fed to pin 7.

Note: In this application the feedback amplifier of the TDA8380 is not used. However an overvoltage on pin 7 will still activate a protection and slow start sequence.

Pin 8 Output of the error amplifier. Not used.

Pin 9 Duty. This is the input of the pulse-width modulator.

Pin 10 Oscillator. A 680 pF capacitor C15 is connected to this pin; together with resistor R11 (4k3) the oscillator frequency is set to 34kHz.

Pin 11 Synchronisation. The trailing edge of the positive sync-pulses, which are superimposed on the linear feedback signal, synchronise the oscillator.

Pin 12 Slow-start (capacitor C17) and maximum duty cycle (R20).

Pin 13 Over current protection. The over current protection safeguards the power switching transistor for being overloaded with a too high collector peak current. For that reason resistors R22 to R26 in the emitter circuit of the power switching transistor sense the collector current. This negative going signal is DC shifted into a positive signal with respect to ground by a DC current from pin 13 flowing through R21, while C18 removes the spikes.

Pin 14 Ground

Pin 15 Emitter of the reverse drive transistor, connected to ground.

Pin 16 Collector of the reverse drive transistor. See drive of the BUW13 SMPS power transistor.

3.4 SMPS Transformer

As already mentioned before the transformer (AT3020/01A) has been designed to handle a maximum output power of 200W and a peak power of 250W. The nominal primary inductance is 420 μH. To keep the leakage inductance (~2%) as small as possible, a turns ratio of 1:1 was chosen. The magnetic circuit of the trasformer comprises two Ferroxcube E46/23/30 cores, grade 3C85. The coil is built-up in layer of copper wire, separated from each other by insulation foil. Thanks to a clever winding

design no screens had to be applied. As a result the size of this transformer could be reduced significantly with respect to the transformer described in Reference [1].

The energy stored in the leakage inductance will be dissipated in the dV/dT limiter (D8/C13/R19) and peak voltage clamp (D5/C7/R5); the energy stored in the parasitic winding capacitance in the power switching transistor T1 and damping networks (R6/C8 and R37/C28).

3.5 Power switching transistor

By fixing the primary inductance of the transformer and its operating frequency, the collector peak current of the power switching transistor is fixed. At a peak output power of 250W the I_c peak is approximately 6.5A. On the other hand the maximum base drive is determined by the control IC TDA8380: $I_{source\ max}$ = 0.75A. The BUW13 has a sufficient high current gain and moreover the I_{boff} could be kept within the limit of the control IC: $I_{sink\ max}$ = 2.5A. For slightly lower maximum power (150W) the BUT12 can be used as the power switching transistor. Note that, in that case, current sensing resistor R21 has to be reduced.

The correct forward drive of the transistor is provided by the supply voltage of the IC and R14/R15, resulting in an I_{bon} of 0.7A. To obtain a correct negative base drive, the bias voltage across C10/C11 is kept constant by three BAW62 diodes (D9 to D11). During turn off, inductor L1 (1.7 μH) in combination with the bias voltage, determines the negative base current (-dI/dt) of the power switching transistor. R17 and C12 damp the ringing of the base-emitter and prevents parasitic switch on of T1 during the flyback.

3.6 Secondary rectifiers

The three secondary flyback rectifiers deliver the 150V (line deflection supply), 32V (audio supply) and 16V (small signal supply). A 12V stabiliser is not provided on the PC board. The load determines the dissipation in the rectifying diodes and hence the size of the heatsink (D15) and copper area. The number of electrolytic capacitors is determined by the load (ripple current) and the ESR of the capacitors.

To prevent interference between the SMPS switching frequency and the line frequency an L-C filter has been added. The inductor is L2 while the capacitor is located on the line deflection board. If the SMPS is running in the synchronous mode, the filter action is not required and L2 can be replaced by a 1 Ω resistor. The feedback voltage for the control circuit is taken in front of this L-C filter.

To prevent crosstalk, the audio supply is brought out floating. The minus of the 32V is connected to ground via R38 to prevent static charge of this transformer winding if kept unused. If there is an overload on the 32V or 16V supply, the currents in the secondary transformer windings can be excessive before the overcurrent protection of the IC is activated. The use of a fuse or fusible resistor (1Ω/4W) at position J3 and a fusible resistor (1Ω/1W) at J4 will make the SMPS short circuit proof also on these two outputs.

3.7 Error-amplifier

The error-amplifier consists of a single transistor T5. The base of this transistor receives the filtered and divided output signal while the emitter is connected to the reference voltage (ZD3). The output current of this error-amplifier is fed to the opto-coupler. As the current through T5 and hence its gain will settle at a value inversely proportional to the current gain of the opto-coupler, the SMPS loop gain will be independent of tolerance or ageing of the opto-coupler. The current through ZD3 is fixed by R42 at 2mA. By keeping it constant, the temperature dependance of the Vbe of T5 is compensated by that of ZD3 [3].

3.8 Opto-coupler

For feedback and mains isolation an opto-coupler (CNG82) is used. As already mentioned before, the opto-coupler is driven in such a way, that the large variation of IC/IF of the opto-coupler is filtered by means of R27 and C19. The emitter of the transistor drives the output-amplifer T2. This transistor is used for keeping the operating voltage of the phototransistor constant; this keeps the bandwidth high.

Except for feedback, the opto-coupler is also used for synchronisation. For this purpose, the sync pulses are superimposed on the linear feedback signal. The slower CNX82A can also be used at the expense of the wave-shape and delay of the sync pulse. Then at 16 kHz the maximum power will be restricted somewhat due to unequal duty factors of the odd and even SMPS pulses.

For standby operation, the opto-coupler diode is driven in forward (IF = 2mA) either by switchon-on transistor T6 or by externally driving resistor R43. In this mode the output voltages will be switched off.

3.9 Standby-supply

For the supply of some digital IC's in the standby mode, a small self-oscillating, current-mode controlled flyback converter delivers 5V/300mA. It uses the same mains input filter, bridge rectifier and RFI/safety capacitor C22 as the main SMPS. For mains isolation and power conversion a small transformer (AT3006/300) is used. The power switching transistor BUX87 requires a small heatsink. [4].

4. Synchronisation

The SMPS can be synchronised down to 32kHz by either 16 or 32 kHz (±4%) negative-going pulses on pin 5 of J17, with a pulse width of 18% of the line time (e.g. line flyback pulses). The amplitude of the sync-pulse measured at the sync-input, should lie between 2 and 6V. The sync-pulses are superimposed on the linear feed back signal. This can

only be done, if they do not affect the voltage stabilisation. To obtain short rise and fall times of the sync-pulse at the sync-input of the TDA8380, the CNG82(A) should be used. Capacitor C16 AC couples the sync-pulses to pin 11 of the TDA8380. The oscillator sawtooth is triggered by the trailing edge of the positive sync-pulse at pin 11 and all subsequent sync-pulses are ignored until the oscillator sawtooth is completed. The oscillator is then inhibited until the end of the next positive sync-pulse. The free-running oscillator frequency is determined by R11 (4k3) and C15 (680pF). Both components should be 1% tolerance types.

If synchronisation of the SMPS is not needed, the following components can be deleted: C19, C35; R29, R27, R49, R50, R51; D18, R19; T2. The opto-coupler CNG82 can be replaced by the CNX82A. Jumpers J1 and J2 should be placed.

5. Mains interference

RFI measurements are made of the SMPS (200W) together with the µSOPS and a mains input filter, consisting of the AT4043/93 and two X-capacitors (220nF). The results must stay below the limits of EN55013, which are drawn in the graph shown later. The measurements just meet the limits. If the SMPS is used with more than 165 watt input power, measures must be included to meet the IEC552-2 standard on mains pollution by higher harmonics.

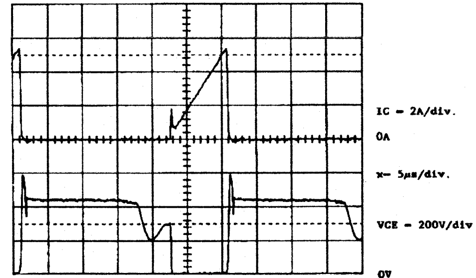
6. Performance

INPUT	185-265V RMS		50/60Hz
OUTPUTS	150V 1.0A STABILISED		LINE SCAN
	32V 1.5A UNSTABILISED		AUDIO
	16V 0.2A UNSTABILISED		SMALL SIGNAL
RIPPLE	150V	≤10mV	SWITCHING FREQUENCY
peak to peak		≤20mV	100Hz
	32V	≤150mV	SWITCHING FREQUENCY
		≤10mV	100Hz
	16V	≤50mV	SWITCHING FREQUENCY
		≤10mV	100Hz
EFFICIENCY	88%		200W LOAD
SWITCHING FREQ.	34kHz		

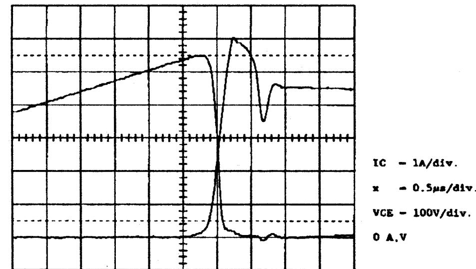
7. Oscillograms

The oscillograms have been made at the following conditions, unless otherwise indicated.

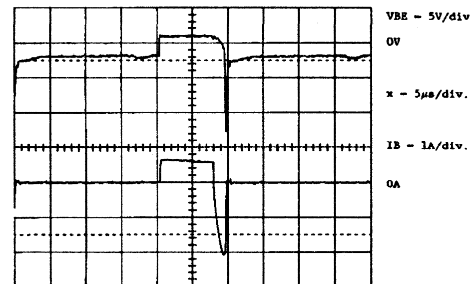
V_{input} = 220VRMS   Load = 200W   not synchronised.



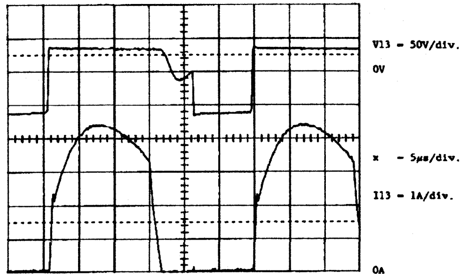
Oscillogram 1. Collector Current and Collector Voltage of the BUW13.



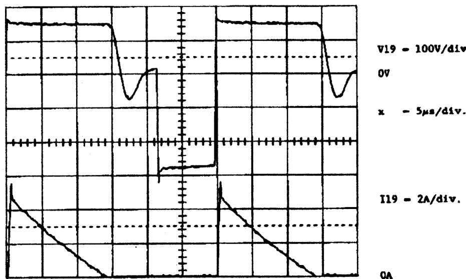
Oscillogram 2. Collector Current and Collector Voltage of the BUW13.



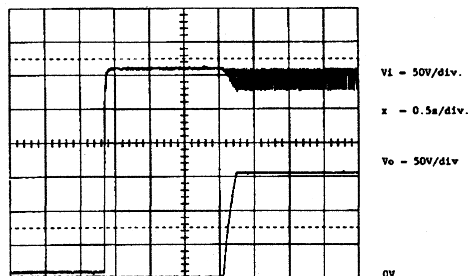
Oscillogram 3. Base Emitter Voltage and Base Current of the BUW13.



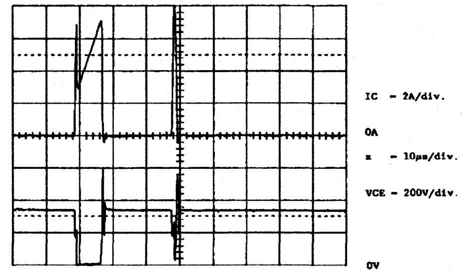
Oscillogram 4. Voltage and Current at pin 13 of the transformer.



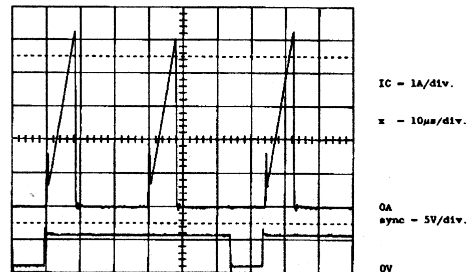
Oscillogram 5. Voltage and Current at pin 19 of the transformer.



Oscillogram 6. SMPS switch on behaviour.



Oscillogram 7. BUW13 Collector Current and Voltage at short circuit 150V output.



Oscillogram 8. BUW13 Collector Current and 15.625kHz sync pulses.

References

Information for this section was extracted from "Synchronous 200W Switched Mode Power Supply for 16 and 32kHz TV"; ETV89009 by H.Simons.

[1] ETV8711 A 200W switched mode power supply for 32kHz TV. Author: H.Misdom. Date: 01/09/87.

[2] Integrated SMPS control circuit TDA8380. Philips Components Publication Number 9398 358 40011 Date: 12/88.

[3] ETV89003 Novel optocoupler circuit for the TDA8380. Author: H.Verees. Date: 2/89.

[4] ETV8834 A dual output miniature stand by power supply. Author: H.Buthker.

8. Circuit diagram.

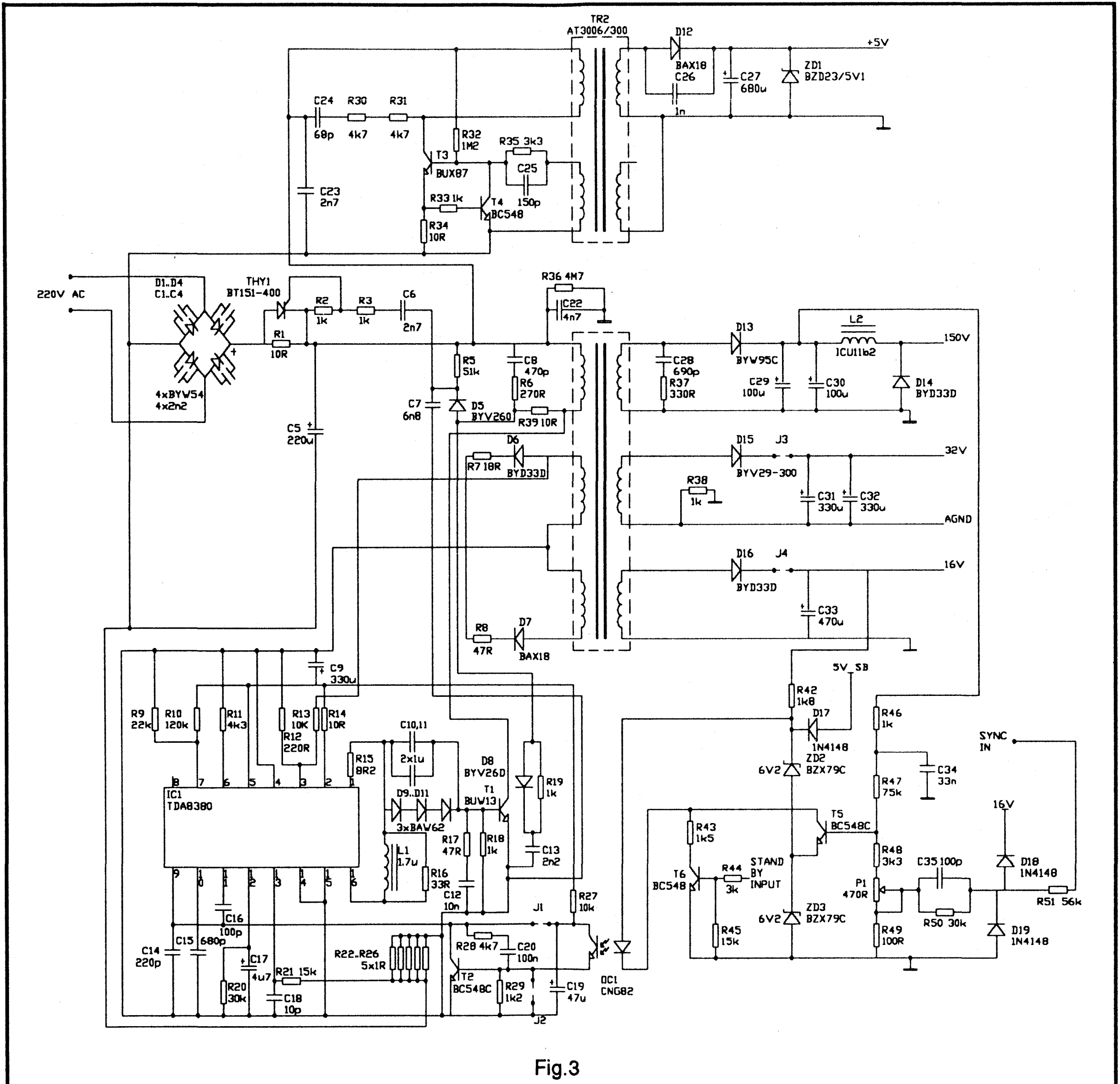
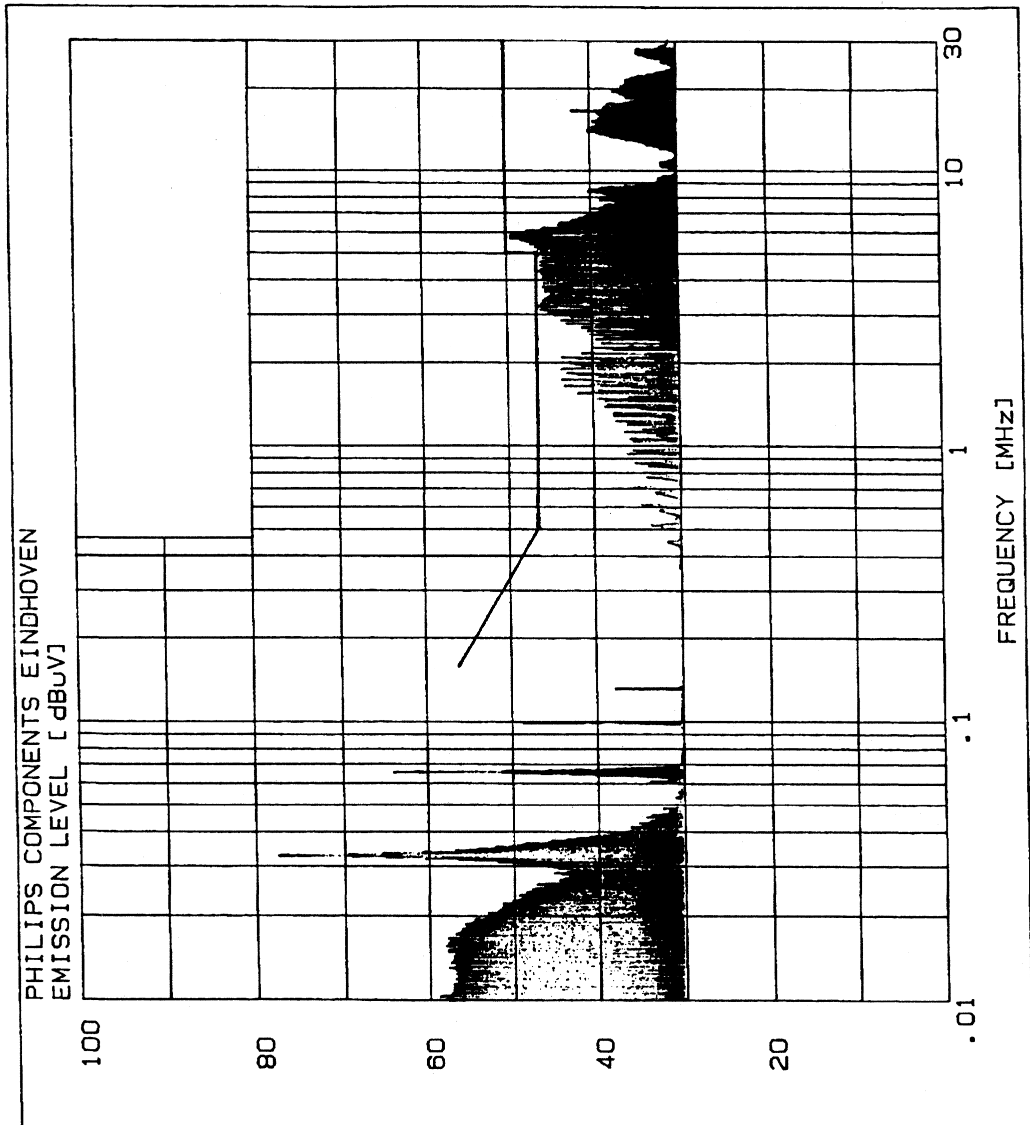


Fig.3

9. RFI measurement



Monitor Deflection and SMPS Example

4.4.1 VGA Monitor With The High Resolution Colour Tube 34ECL10X36

A high performance deflection circuit for use in a monitor, working with VGA standard signals, is presented. The circuit features DC control of most of the adjustments.

Summary

The report describes the deflection circuitry for a high performance monitor, working with VGA standard signals. The monitor features high linearity deflection circuits and good anti-breathing circuits. A special feature is the possibility to control most of the adjustments with a DC voltage, allowing the use of I²C bus controlled DAC's. A built-in circuit automatically detects the mode of the signal source and adjusts the circuit according to that mode.

1. Introduction

With more and more CAD software available for PCs, a high performance colour monitor is often needed. This report describes a monitor design intended for use in a system using VGA-standard signals. The design is based on the tube/coil combination M34ECL10X36. This is a high resolution colour display tube assembly, with black matrix screen, a 0.29 mm dot triplet pitch and advanced gun design for smaller spotsize. The tube can be chosen from a range of different versions of light transmission, different kinds of finishing faceplate and various types of phosphor combinations. The deflection coil is available in a range of impedances.

A special feature of the design is, that all the picture tube alignments (except the focus voltage and the horizontal linearity), and the horizontal and vertical free running frequency, are adjusted with a DC voltage between 0 and 12 volts. This opens the possibility, to use for instance, I²C bus controlled DAC's for all adjustments. In the production of such a monitor, this means that all these adjustments can be done electronically, without the need for expensive mechanical interfaces. An extra advantage is, that, if needed, the control potentiometers or DAC's can be located far away from the actual monitor circuit. On the deflection pc-board, presented in this report, both potentiometers as well as a connector for a control pc-board with I²C bus controlled DAC's can be used. The layout and component placement of an interface pc-board with TDA8444, can be found in section 6.

The design covers all three modes of the VGA standard: one line frequency of 31486 Hz and three field frequencies/number of displayed lines: 60 Hz/480 lines, 70 Hz/350 lines, 70 Hz/400 lines. In the design, a circuit is incorporated that automatically detects the mode of the signal source, by looking at the H and V sync polarity. The results in the displayed picture having the same dimensions in every mode.

Great care has also been taken to linearise the horizontal and vertical deflection and to minimise breathing of the picture. Furthermore, the design features a protection against spot burn-in, controlled switching off behaviour and beam current limiting.

Because of the 32 KHz line frequency, the 0.38 mH deflection coil is chosen for this design.

Only the horizontal and vertical deflection circuitry and the circuits for generating auxiliary supply voltages and tube voltages are described in this report. A complete set up, comprising a 100V/70W SMPS (see section 8) and wideband video pre- and output amplifiers (see section 7), was used to judge the performance of the deflection circuitry.

2. Circuit description

The circuit can be divided into seven sections:

1. Mode detector
2. Synchronisation circuit
3. Line deflection
4. Field deflection
5. E/W generator
6. Secondary and tube voltages
7. Miscellaneous

Each section will (if appropriate) be subdivided, following a short description.

2.1. Mode detector

There are four modes in VGA:

Mode	H/V	Display Mode	f-horiz	f-vert
1	+/-	720 x 350	31.5 kHz	70 Hz
2	-/+	720 x 400	31.5 kHz	70 Hz
3	-/-	640 x 480	31.5 kHz	60 Hz
4	+/+	1024 x 768	not implemented	
4A	+/+	800 x 600	not implemented	

The mode detector distinguishes the current mode from the polarity of the synchronisation pulses. The outputs of the mode detector are normalised horizontal (HS) and vertical (VS) synchronisation pulses, and three control outputs: 60 Hz/480L, 70Hz/350L, 70Hz/400L. The control outputs, indicating the current mode, are used to adapt the picture tube alignments for that mode.

The mode detector is built around IC107 and IC108.

2.2 Synchronisation circuit

2.2.1 Horizontal synchronisation

The TDA2595, IC101, is used here. From IC101, only the horizontal oscillator with synchronisation input, both phase control loops and the horizontal driver stage are used. The first loop compares the phase of the horizontal sync pulse HS and the oscillator. It protects the horizontal deflection stage against irregular erratic sync signals. The second loop compares the phase of the oscillator and the horizontal flyback pulse, connected via R111 to pin 2, thereby compensating for storage time variations of the horizontal deflection transistor (BU903).

The open collector output pin 4 of the TDA2595 provides the drive pulses for the line driver (see section 2.3.1.).

The adjustment of the free-running frequency of the oscillator, signal "HOR.FREQ.", and the horizontal shift, signal "HOR.SHIFT", are attained by a DC voltage between 0 and 12 Volts.

2.2.2 Vertical synchronisation

The vertical synchronisation pulses from IC107 are mixed via diode D106 with blanking pulses from IC102, a TDA2653A vertical deflection IC. Pin 2 of this IC is a combined synchronisation input/blanking output. The combined synchronisation/blanking pulses form the signal "VS", which is also used for picture blanking (see section 2.6.2.c.) and sample-and-hold control of the parabolic voltage generator (see section 2.5.1.).

2.3 Line deflection

2.3.1. Line driver

The line driver is built around transistor T101 and driver transformer TR102. Its a non-simultaneous drive circuit: when T101 conducts, the power transistor T102 is off. The high turns ratio of TR102 results in a low collector current of transistor T101. Therefore, a transistor in TO92 housing could be chosen.

A plot of the collector voltage and current of T101 are shown in section 4.

An extra feature of the drive circuit is that it is stacked with the +12 Volt supply. In this way, when +100 volts is applied, the horizontal deflection circuit automatically starts working, after which the other circuits start working too. Once the deflection operates, there is a takeover via D102 and R116.

2.3.2. Power output stage

The circuit is set up as the well known diode modulator (see ref. 4 and 5), built around power transistor T102. The line deflection coil is connected to "H-OUT/1" and "H-OUT/2". The S-correction capacitor is C120, the horizontal linearity-corrector is L101 (adjustable).

The supply is taken from the +100 Volt line. If a synchronised SMPS is used (synchronisation pulses are provided on pin 4 of the supply connector J103), coil L103 can be left out and replaced by resistor R228.

The filter R119/C121/L104 can be inserted to prevent ringing of the current through the primary winding of TR101. If used, one should be aware of the fact that this causes some ringing on the voltage on pin 10 or TR101. If the loop C122-primary winding TR101-C117-C118 is kept small on the pc-board, this filter can be deleted and replaced by a jumper.

Transistor T102 is driven by the line driver circuit. A plot of the voltages and currents of the collector and base of T102 can be found in section 4.

The signal "E/W-OUT" drives the modulator coil L2. It provides correction of the E/W distortion and also picture width control (see section 2.5.3.).

A peak rectifier (consisting of diode D103 and capacitor C116), connected to the collector of transistor T102, provides a high voltage of +900 Volts. This voltage is used as a supply voltage for the VG2 control circuit (see section 2.6.2.d.).

2.4. Field deflection

The heart of the circuit is IC102, the TDA2653A. Because of the requirement of DC control, the peripheral circuitry differs considerably from the typical application. Only the extra circuitry will be covered in this report. For a description of the TDA2653A, see the Philips Data Handbook IC02.

2.4.1. Oscillator

In its normal application, as presented in Philips Handbook IC02b, the long flyback time of the free-running oscillator of the TDA2653A would cause the blanking pulse to be too long. Therefore, the oscillator flyback time is shortened with the aid of transistor T109: on synchronisation, capacitor C151 is discharged very rapdily (to a certain level, set inside IC102) via resistor R145 and transistor T109.

Fig.2.3.1 Line deflection circuit

2.4.2. Sawtooth generator

The sawtooth generator (IC106-1/T105 to T108/C127) generates an extremely linear sawtooth voltage on capacitor C127, starting from zero volts. The capacitor C127 is rapidly discharged by a transistor in IC102 pin 11 on synchronisation. The charge current is set by resistors R137/142 and the control voltage on J200-4. For the 70 Hz modes, the charge current is changed by paralleling R133 or R135 to R137. Because the DC voltage of the sawtooth changes with its amplitude (the starting voltage is always zero volts), this would cause a vertical shift of the picture. This is compensated for by resistor R155 with the signal "VERT.AMP." and by R148/149 for the 70 Hz modes.
The control range of the picture height with "VERT.AMP." is approximately ±20 mm.

To compensate for EHT variations, resistor R139 is added. The signal "EHTINFO" (see section 2.6.2.b.), together with R139, provides a correction current for the sawtooth generator, to stabilise the vertical amplitude of the picture with EHT variations. The resulting vertical shift is compensated at the input pin 4 of the output amplifier of the TDA2653A.

This tube/coil combination also needs S-correction in vertical direction. This S-correction is provided by integrating a parabolic current in capacitor C127, in the following manner:

The signal "PARAB" (see section 2.5.1.) is shifted to the correct DC voltage with IC106-2, to prevent variation of the sawtooth amplitude with the amount of S-correction. By connecting a resistor R138 between the output of IC106-2 and the emitter of T107 a parabolic current is substracted from the constant current, charging capacitor C127. The amount of S-correction is set by resistor R138.

The result is a sawtooth with S-correction.

2.4.3. Vertical shift

To shift the picture in vertical direction, the DC working point of the output amplifier (reference voltage pin 10) is changed. With a control voltage of 6 ± 6 volts on J200-2, the picture can be shifted ±10 mm.

2.4.4. Buffer output

The sawtooth voltage on pin 11, generated by the sawtooth generator, starts at zero volts. Between pins 11 and 3 is an internal buffer, which shows a non-linearity at the start of scan if not properly preloaded. To prevent this, the output of the buffer is loaded with a resistor R153. The other side of resistor R153 is connected to a negative supply voltage, generated by the flyback generator. In this way the buffer output can also drive signals down to zero volts.

2.4.5. Preamplifier feedback

The vertical deflection current is sensed by resistor R160. The voltage gain of the amplifier is set by input resistor R152 and feedback resistor R156. So, the relationship between sawtooth input voltage V(sawt.) and deflection output current Io(pp) is given by the equation:

$$I_o(pp) = \frac{R156}{R152} \cdot \frac{V_{sawt}}{R160}$$

Resistor R154 is used to compensate for vertical shift with EHT variations.

2.4.6. Power output stage.

The vertical deflection coil is connected to "V-OUT/1" AND "V-OUT/2". The combination of capacitor C135 and transistor T110 provides a DC coupled output stage configuration, without the need for a split power supply. This configuration was chosen for reasons regarding safety and bouncing effects. To reduce the dissipation of transistor T110, resistor R162 is added. Resistors R161 and R162 limit the maximum obtainable -/+ shift.

2.5. E/W Generator

The E/W generator produces an output voltage to correct the line deflection current for the E/W distortion of the tube. Also, a control of the picture width is provided, with compensation for EHT variations.

2.5.1. Parabolic voltage generator.

By integrating the sawtooth voltage across resistor R160, a parabolic voltage "PARAB" is generated (IC103-1/R173/C139).

A "sample-and-hold" circuit (IC103-2/IC104-1/C137) senses the "PARAB" signal at vertical synchronisation. In this way, the peaks of the parabolic voltage are held at 3.6 volts (voltage at non-inverting input of IC103-2).

The signal "PARAB" is used to generate an E/W correction voltage for the line deflection (see section 2.5.2.), and also to generate S-correction on the sawtooth voltage for vertical deflection (see section 2.4.2.).

2.5.2 Electronic potentiometer

In order to facilitate adjustment of the E/W correction voltage with a control voltage between 0 and +12 volts, an electronic potentiometer is used. This potentiometer is built around IC105, a CA3046 transistor array, and transistors T112/113.

The signal "PARAB" is used as an input signal on pin 12 of IC105. The output of the electronic potentiometer is a current, flowing in pin 1 of IC105, that is modulated by the signal "PARAB" and controlled in amplitude by a DC voltage

of 0 to +12 volts on J200-5: "E/W-AMP.". With resistor R201, the DC value of the output current is made independent of variation of the control voltage.

The output current is used as an input current for the E/W power output stage.

2.5.3. E/W power output stage

A current-to-voltage converter (IC109-1/T111) uses the parabolic shaped current, generated in the electronic potentiometer, and a DC current, set by resistors R184/202 and the control voltage on J200-6: "HOR. AMP." to generate the desired output voltage. This output voltage is corrected for variations of the EHT by the signal "EHTINFO" and resistors R182/R183. The output of this converter: "E/W-OUT", is connected to the appropriate point of the diode modulator (see section 2.3.2.) via resistor R167. On this point, a negative going parabolic voltage, superimposed on a DC voltage is needed.

For the different modes, different corrections are needed. This is facilitated by electronic switches IC104-2/3. The switches are controlled by the mode indicating signals.

2.6 Secondary and tube voltages

2.6.1. Secondary voltages

Besides the EHT of 25 kV, five extra voltages/signals are derived from secondary windings of the Diode Split Box line output transformer TR101:

a. "+24V": +24 volts for supply of the vertical deflection stage.

b. "-70V": -70 volts for supply of the grid 1 driver stage.

c. "HOR.FLYB.": a positive going horizontal flyback signal for the phase comparator of the TDA2595.

d. "VF1/2": heater current for the tube.

e. "HCL/"SYNPS": a positive going horizontal flyback signal, used as horizontal clamp for black current stabilisation in the video output amplifiers ("HCL"), and synchronisation of the SMPS ("SYNPS").

2.6.2. Tube voltages

2.6.2.a. EHT and focus

The EHT is taken directly from the EHT output of the DSB TR101, and via a series resistor in the EHT cap and bleeder unit, connected to the anode of the picture tube. The use of a bleeder circuit on the EHT has several advantages:

- it provides a minimum load on the EHT, reducing and linearising the internal impedance of the EHT significantly;
- by incorporating the focus potentiometer in the bleeder circuit, the tracking of the focus voltage with the EHT is greatly improved:
- variations in EHT can be derived from the bleeder current on a low voltage, which gives good possibilities for stabilising the picture with EHT variations.

2.6.2.b. EHT compensation

IC109-1 derives a signal "EHTINFO" from the bleeder current. For a correct working of this circuit, P109 should be adjusted so that the signal "EHTINFO" is +12 volts with minimum EHT load (dark screen). Another way of adjusting is as described in section 3.

Potentiometer P109 is necessary because of the large tolerance of the bleeder circuit components. With a fixed resistor the working voltage of the E/W power output stage would vary very much, making a very large control range of the horizontal amplitude necessary.

2.6.2.c. Grid 1 voltage

The highest output voltage of the video output amplifiers is approximately +92 volts (supply voltage of the video output stages is +100 volts). With a highest cut off voltage of the picture tube of 125 volts, the voltage on grid 1, VG1, has to be -33 volts. Since VG1 is also used for user black level adjustment ("brightness control"), VG1 is made adjustable between -22 and -42 volts by means of the inverting amplifier around transistor T117.

Brightness control can be implemented in two ways:

- by means of a potentiometer of 22 kohm, connected between +12 volts (J105/5) and ground (J105/1), the wiper connected to "DCBRIGHT" (J105/3).
- by means of I2 bus control: connect the signal brightness on the I^2C bus interface print with "DCBRIGHT" (J105/3).

Field blanking is achieved by adding blanking pulses to the grid 1 voltage via resistor R220. The signal "VS" causes a -20 volts blanking pulse on the collector of transistor T117. Capacitor C146 provides a low ohmic path for this pulse to the actual tube-pin.

Beam current limiting is acheived through diode D116. During normal operation, maximum beam current is supplied via resistor R219 (the excess current flows through diode D115 to ground). Further increasing the beam current, will cause a negative voltage on the anode of diode D115. If this voltage drops below the voltage on VG1, diode D116 becomes conductive. Now a further increase of beam current is not possible, because that would further increase the voltage drop across R219, so decrease the voltage on VG1, causing a decrease of the beam current.

The horizontal flyback pulses, rectified via D119, charge C147 to a negative voltage of approximately -8 volts during scan. During flyback, C147 is charged positive through resistor R221. During normal operation however, D120 is always blocked. In case the horizontal output stage stops operating or in case of a short circuit of the +12 volts, the +24 volts on resistor R221 will cause diode D120 to become conductive. The large current through resistor R221 will cause the output voltage on the collector of T117 to become approximately -60 volts. The possibly excessive beam current is effectively suppressed in this way.

At power switch off, the +100 volts supply voltage will decrease very rapidly. The cathode of capacitor c145 goes to a large negative voltage. Now, capacitor C145 is discharged via diode D117 and resistor R225, causing a large negative voltage on VG1. In this way, the screen is blanked at power switch off.

2.6.2.d. Grid 2 voltage

The grid 2 voltage has to be adjustable betwen +340 and +750 volts. To allow an input voltage control range of 0 to +12 volts, a differential inverting amplifier with high output voltage capability has been developed. Transistors T115 and T116 are used as a differential pair to reduce temperature dependance of the output voltage. Transistor T114 with resistor R207 form the high voltage output stage.

If no I^2C bus control of the grid 2 voltage is needed, the circuit around T115/115/116 can be deleted, and the grid 2 voltage can be taken from the DSB TR101. A wire can be soldered in a spare hole in the pc-board near the DSB, and contacted to the VG2 output of the DSB.

Item	Pot.	DAC o/p	Note
Focus	P110		Adjust for maximum sharpness.
Horizontal Frequency	P102	2/00	Short circuit pin 12 of the TDA2595 to ground. Adjust until horizontal rolling stops. Remove short on pin 12.
Vertical Frequency	P105	2/07	Connect a frequency counter to pin 6 of TDA2653A. Remove VGA signal. Adjust to 55Hz. Reconnect the VGA signal.
EHTINFO	P109		Adjust the brightness and contrast control for a just visible picture. Adust P109 until the horizontal amplitude of the picture just starts increasing.
Horizontal Amplifier	P107	2/02	Adjust to 248mm between outer lines.
Vertical Amplifier	P103	2/04	Adjust to 186mm.
Horizontal Shift Vertical Shift	P101 P104	2/01 2/06	Adjust for centre of screen.
E/W Amp	P106	2/03	Adjust for perfect rectangular picture.
Black Level	P1201 P1301 P1401	1/05 1/06 1/07	Adjust the voltage on the cathode of the picture tube to 92 volts. Set VG1 to -33 V and VG2 to 360 V. Disconnect the VGA signal.
VG2	P108	2/05	Measure the luminance of the picture tude with a colour analyser. Increase VG2 until the brightest gun displays 0.5 nit. Adjust the black level of the other two guns until all three guns display 0.5 nit.
White Balance	P1010 P1030 P1050	1/02 1/03 1/04	Set contrast to maximum. Apply a white signal to the monitor. Decrease the two brightest guns, to equal all three outputs.

Table 3.1

2.7 Miscellaneous

The value of resistor R217, in the heater supply of the picture tube, depends on the circuit on the picture tube panel. With the two coils of 12 µH in series in the heater supply on the picture tube pane, resistor R217 should be replaced by a jumper.

The value of resistors R230, R231 and R232 depends on the input impedance of the following circuit. With the video preamplifier, presented in section 7.1., these resistors should be left out. The input impedance of the preamplifiers is 75 ohms.

During testing of the deflection circuit with the presented pc-board, it was necessary to change the location of resistor R203, potentiometer P109 and capacitor C142. On the presented board, these components are located near the focus potentiometer. However, because of the differential voltage between ground connections of P109 and IC109, the signal "EHTINFO" was overloaded with line pulses. Therefore, these three components should be located near IC109. P109 and c142 should then be grounded at the same ground as IC109. Furthermore, the following components had to be added:

- resistor R234 in the supply of Ic109, to prevent induction of line pulses through this long lead.
- capacitor c152, for decoupling of the supply of IC109. Ground connection should be chosen near to pin 4 of IC109.
- capacitor C153, to reduce the gain of this stage for higher frequencies.

Also, it was found that the wipers of potentiometers P101 to P108 can be short circuited to each other, because the potentiometers are located very close to each other. Care should be taken to avoid this during mounting of the components.

3. Alignment procedure

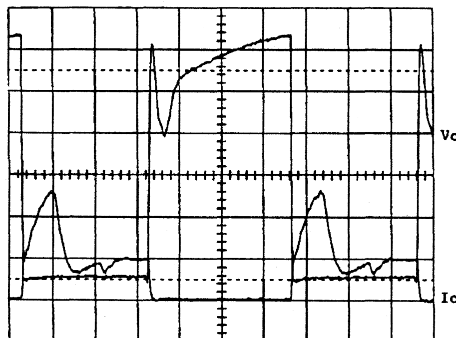
Turn all potentiometers, except P109 and P1010/1030/1050 on the video pre amp board, to their middle position or make all the outputs of the I²C bus controlled DAC's +6 volts. P109 should be turned fully clockwise, i.e. maximum resistance. P1010/1030/1050 should be set for maximum output.

Apply a standard 60 Hz VGA signal (preferably a cross hatch) to the monitor.

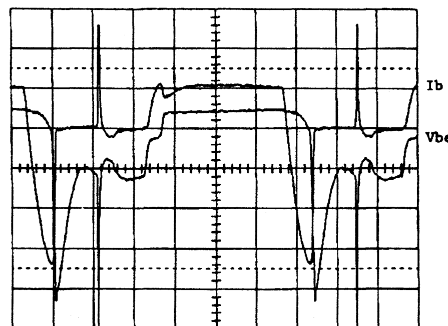
The alignment should be done in the sequence as stated in table 3.1.

Turn on the power. Turn the brightness control up for a normal picture.

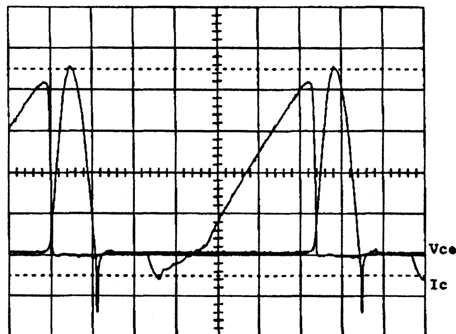
4. Measuring results



Driver transistor T101: collector current IC (50 mA/div.) and collector voltage Vc (20V/div). Note: If T101 is conducting, although the collector voltage is +12V, the collector-emitter voltage is < 0.2V.
Horizontal scale 5µs/div



Line output transistor T102 : base current Ib (0.5A/div) and base-emitter voltage Vbe (2V/div).
Horizontal scale 5µs/div



Line output transistor T102 : collector current Ic (1.0A/div) and collector-emitter voltage Vce (200V/div).
Horizontal scale 5µs/div

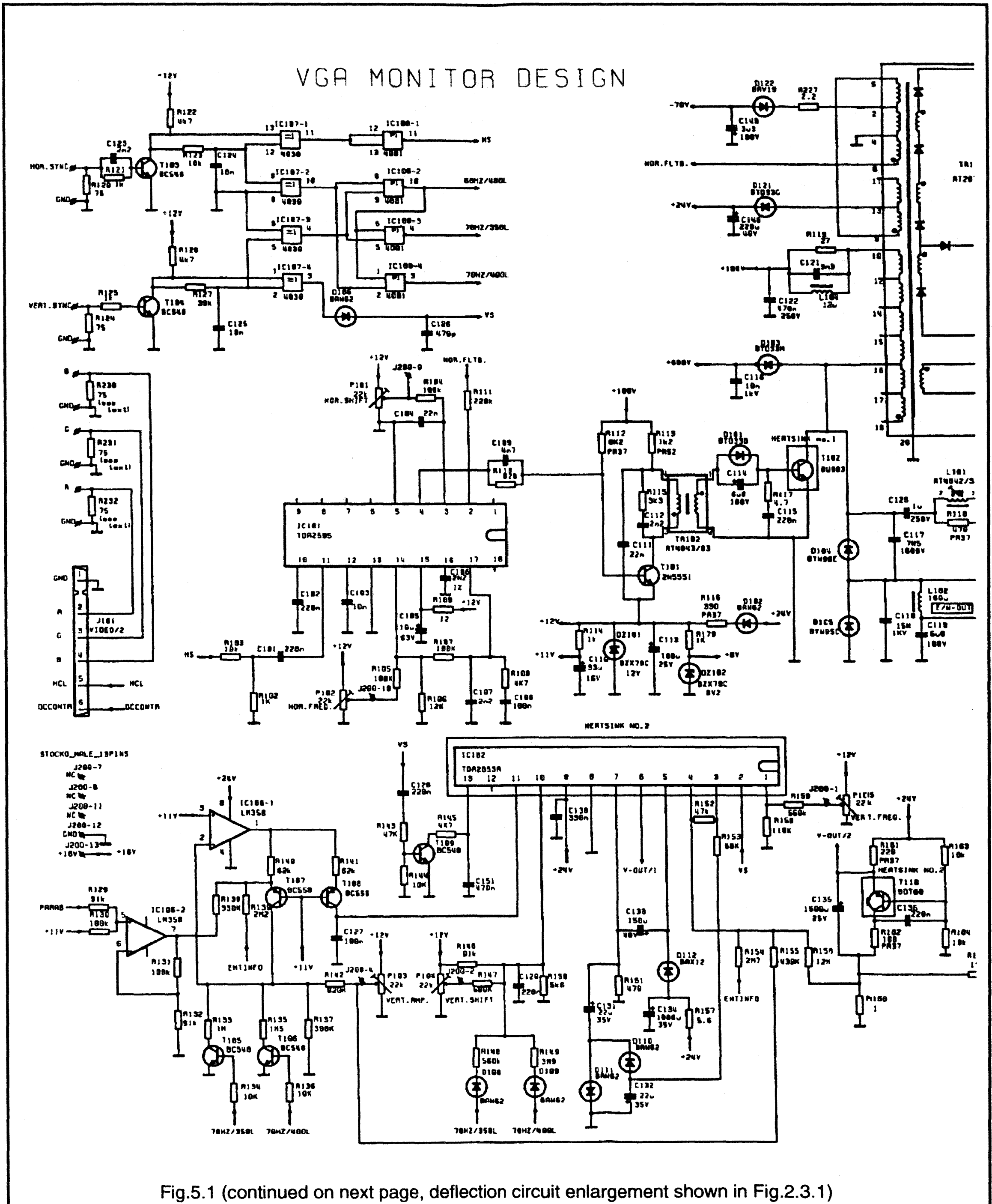


Fig.5.1 (continued on next page, deflection circuit enlargement shown in Fig.2.3.1)

Fig.5.1 (continued from previous page)

6. I²C bus interface

6.1. Introduction

The deflection pc board provides the user with three options for alignment of picture geometry.

1. With potentiometers on the deflection pc board, located all together at an easy accessible side on the pc board.

2. with potentiometers on a sub pc board, connected via a flat cable to the deflection pc board.

3. by means of an I²C bus controlled interface board, as presented in this section.

6.2. Circuit Diagram

The circuit uses two octuple DAC's TDA8444. They feature I²C bus control of eight individual analog outputs. IC1 can be used to control brightness (output 1/00, not implemented), contrast (output 1/01), gain (outputs 1/02 to 1/04 for resp. Red, Green and Blue) and black level adjustments (outputs 1/05 to 1/07) of the video amplifiers. DC-control of the black level of the video output amplifiers is implemented in the design presented in section 7.1, is used for contrast control, while the potentiometers at the inputs are used for white balance. This second TDA8444 has series resistors in the outputs, to protect it against possible high voltages, coming from the picture tube panel (in case of a flashover).

IC2 is used to control the adjustments of the deflection circuitry on the main pc-board.

A complete overview of the DAC related functions is given in the table below.

DAC	IC1 Function	IC2 Function
00	(brightness)	Hor. Oscillator
01	contrast	Hor. Shift
02	gain red	Width
03	gain green	E/W Amp
04	gain blue	Height
05	Bl. lev. red	VG2
06	Bl. lev. green	Vert. Shift
07	Bl. lev. blue	Vert. Oscillator

The address of the IC's can be set with jumpers.

A +12 volt stabiliser is fitted on the pc-board to supply the two IC's. Optional, an extra +5 volt stabiliser can be inserted, to supply power to external IC's. The power dissipation of this stabiliser can be reduced by a series resistor in the input.

Connection of the interface board to the main board, is made by con.3. This connector actually consists of two connectors; con. 3a (seven fold) and con 3b (six fold). This 13 fold female connector fits directly on the corresponding pins on the main board. The I²C bus and outputs for control of the vide amplifiers are connected via a four resp. seven fold stock connector.

7. Video amplifiers

7.1. Optional Video Preamplifier

The preamplifier consists of three identical stages for red, green and blue. A potentiometer is placed in each input, to allow for an adjustment of the white balance, but also the input voltage can be limited here. The nominal input voltage is .7 Vpp Video, which gives an output voltage of 3 Vpp. the disadvantage of this preamplifier is that by turning the contrast potentiometer P1001, not only the amplitude of the output signal changes, but also the DC level. This implies that a black level clamp in the video output amplifiers is required. The advantage of this solution is its simplicity and price.

The preamplifier can only be used in conjunction with an AC coupled video output stage.

The user contrast control input "Contr." (J1002 pin 1) is also a DC control. This input is adapted for 0 - 12 volts by means of the resistors R1002 and R1003. Without these resistors the control voltage of the contrast control input must be between 0 to +5.1 volts.

The supply voltage of +16 volts is taken from the SMPS.

7.2 Video output amplifiers

The video signals are amplified from TTL level (3 Vpp) to 45V output swing by three identical amplifiers. The amplifiers are commonly known as buffered cascode amplifiers. The gain is determined by the collector impedance (for low frequencies: R1202 in parallel to R1203) divided by the emitter impedance (for low frequencies: R1211). In this application the gain is 15 times. The maximum output fall time is 11 nanoseconds. The maximum pixel rate is 0.4/Tfall, which corresponds to approximately 35 MHz. The maximum rise time is 15 nanoseconds, but has much less influence on the perceived contrast of small details because of the gamma factor of the tube.

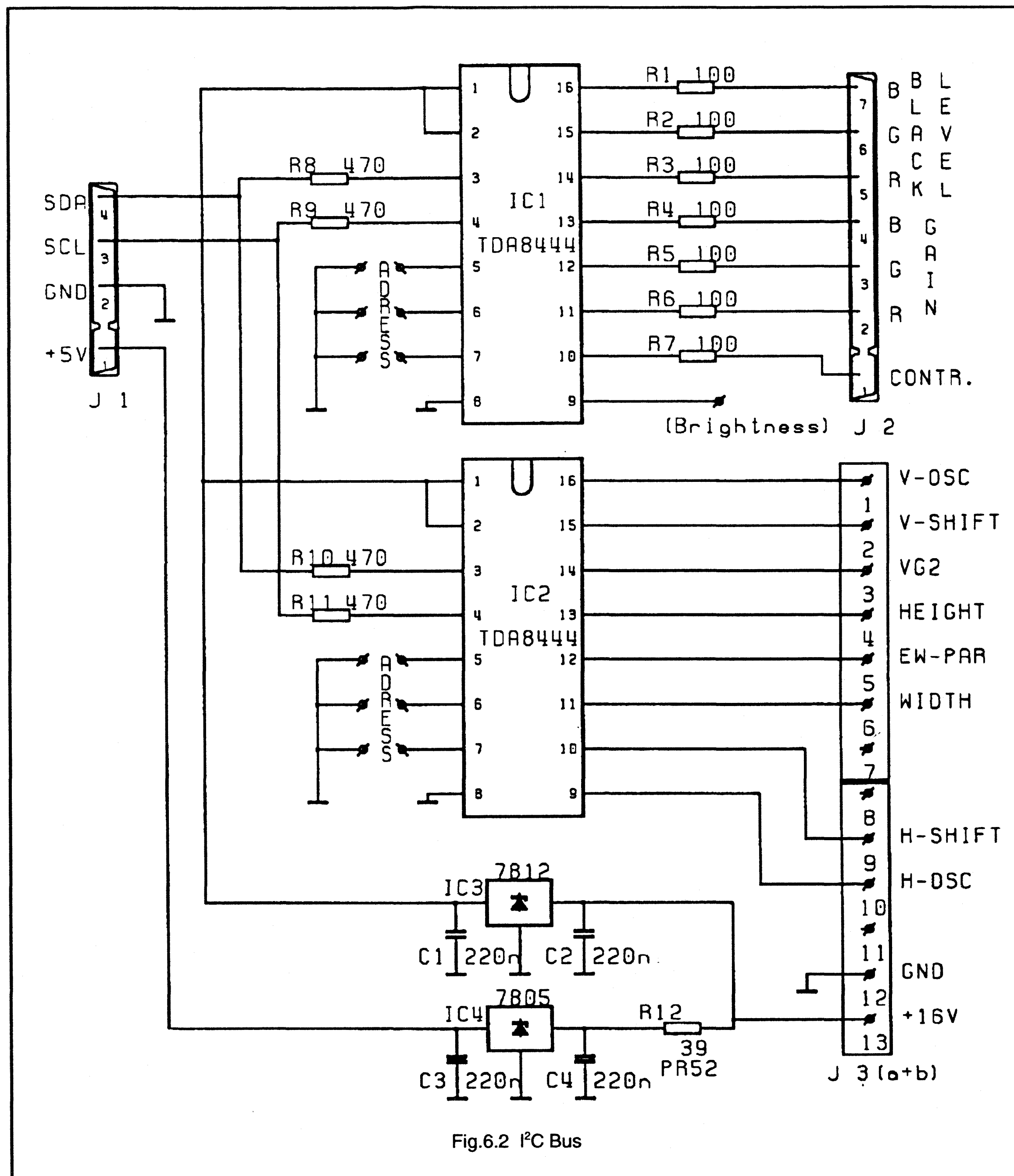


Fig.6.2 I²C Bus

Fig.7.1 Video preamplifier

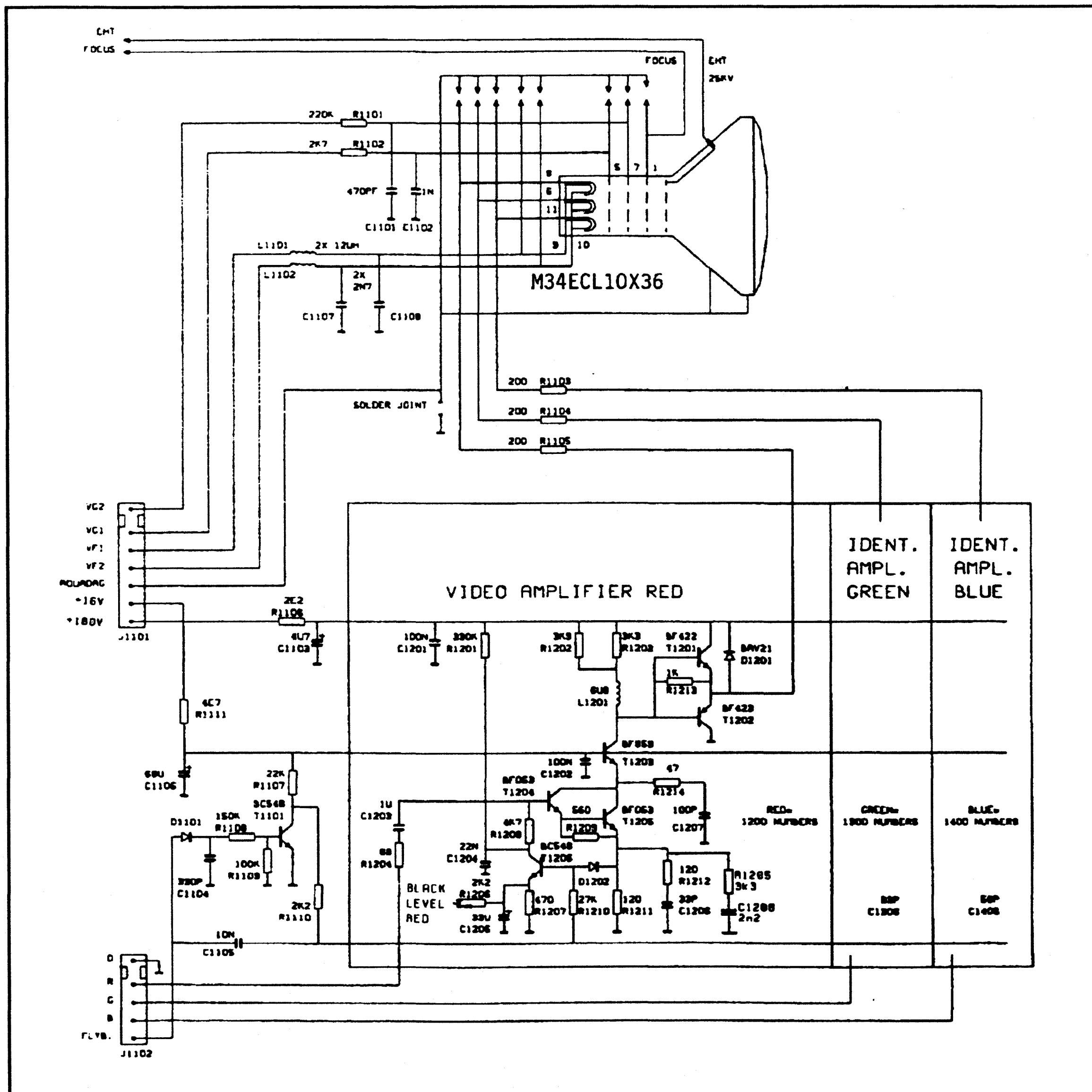
If the input signals of the amplifiers are connected via the main pc-board, or via an unbuffered preamplifier (like described in chapter 7.1.), the video amplifiers may not be terminated by a resistor of 75 ohm. If the video cables are connected directly to the amplifier, the reserved space on the video pc-board should be used to terminate the coax cables with 75 ohm.

The video amplifier is AC coupled and therefore the black level needs to be restored. For this purpose a small control loop (around transistor T1206 and diode D1202) will stabilise the DC voltage on the emitter of T1205 during blanking. This voltage determines the black level at the output.

If flyback pulses do not appear for whatever reason, the amplifiers would go into bottoming, causing a very bright pricture and excessive dissipation in the collector resistors R1202 and R1203. If flyback pulses are missing, transistor T1101 will provide a continuous blanking voltage for the

black level control loop. As a result, the screen will blank.

The black level adjustment is DC controlled with a voltage between 0 and +12 Volts. Although the pc-board is not supplied with a connector for external adjustment of the black level, in a redesign an extra connector can easily be implemented on the pc-board. The three signals "BLACK LEVEL R/G/B", from the I²C interface board, should be connected to resistors R1206, R1306 and R1406. Potentiometers P1201, P1301 and P1401 should be left out.



8. Power supply

8.1. SMPS

A circuit diagram of a suitable SMPS is given on the next page. The design uses the TDA8380 (ref. 1) for control of the SMPS and an opto-coupler for feedback and synchronisation (ref. 2). It delivers +100 volts for the deflection circuitry and the video output amplifiers. A +16 volts output is provided for the video preamplifiers and the I²C bus interface. The sync output on pin 4 of connector J103 of the deflection pc-board can be coupled directly to the sync input of this SMPS.

Care should be taken, concerning the position of the input filter of the SMPS. It should be kept away from the picture tube as far as possible, to prevent interference from the input filter to the deflection. This is especially visible when the difference, between line and vertical deflection frequency, is 10 Hz.

If the SMPS design of ref. 1 is used, then (see drawing PCAL 2115 in ref. 1):

- the connection point of the anode of V13 and R25 should be connected to pin 13 of T1 (instead of to pin 14).
- replace R28 and R29 with 33k resistors (both were 47k)
- replace C4 with 560 p/1% (was 750 p)
- the following components can be deleted:

  transistor V14

  i.c. U3

  capacitors C22 and C23

  resistors R7, R13 and R32

Adjust the output voltage to +100 volts under normal load conditions.

8.2. Degaussing

The degaussing circuit, as shown below, is designed to operate over the entire input voltage range of 100 VAC to 264 VAC. Within this range, the current is > 4.5 App at switching on. The current after 30 sec. is < 2 mApp.

9. References

Information for this section was extracted from "VGA monitor with the high resolution colour tube M34ECL10X36"; ETV89008 by H.Verhees.

1 Title : Integrated SMPS Control Circuit TDA8380, Philips Components Publication Number 9398 358 40011, December 1988.

2 Appl. Note : Novel optocoupler circuit for the TDA8380
Author : H.Verees
Report No. : ETV/AN89003

3 Philips Data Handbooks

4 Title : A new design of a diode modulator for E/W raster correction in CTV receivers.
Author : A.H.Nillsen.
Report No. : EDS7312

5 Title : Some aspects of a diode modulator.
Author : C.H.J.Bergmans.
Report No. : EDS 7805

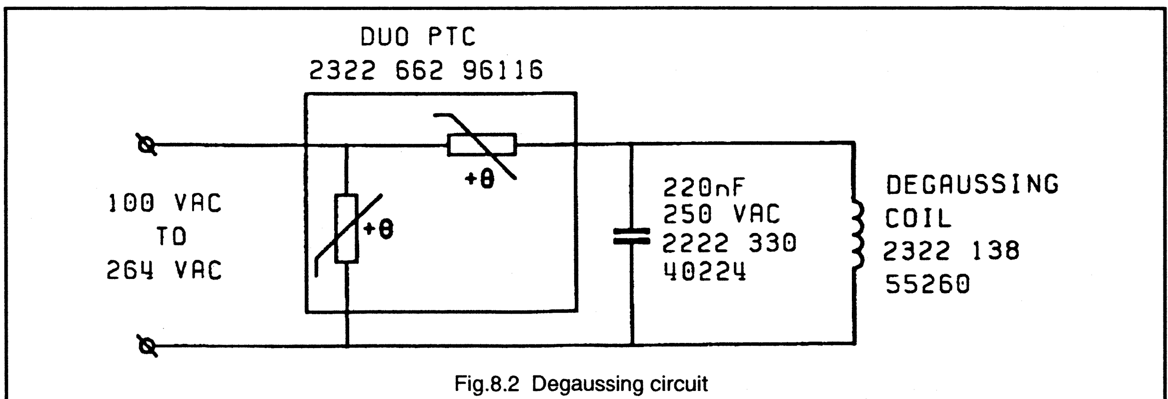
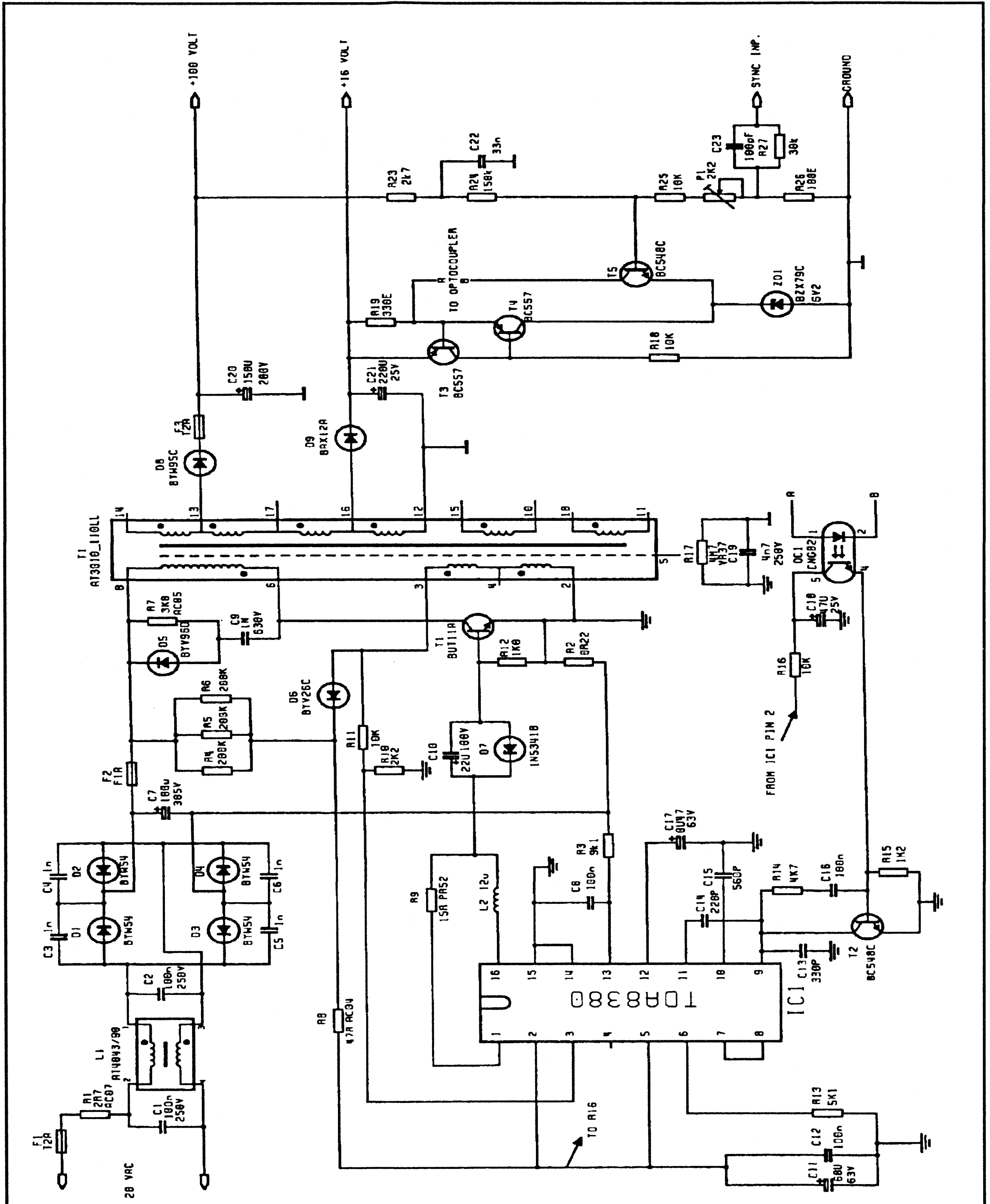


Fig.8.2 Degaussing circuit


+100 VOLT
+16 VOLT
SYNC INP.
GROUND
TO OPTOCOUPLER
FROM IC1 PIN 2
TO R16
28 VAC
TDA8380
IC1
BU11A
BYW95C
BAX12A
BYV26C
BYV96D
BTW54
BC548C
BC557
BZX79C
1N5341B
CNG82
AT3010_110LL
AT4043/90

CHAPTER 5

Automotive Power Electronics

5.1 Automotive Motor Control
(Including selection guides)

5.2 Automotive Lamp Control
(Including selection guides)

Automotive Motor Control (Including selection guides)

5.1.1 Automotive Motor Control With Philips MOSFETS

The trend for comfort and convenience features in today's cars means that more electric motors are required than ever - a glance at Table 1 will show that up to 30 motors may be used in top of the range models, and the next generation of cars will require most of these features as standard in middle of the range models.

All these motors need to be activated and deactivated, usually from the dashboard; that requires a lot of copper cable in the wiring harnesses - up to 4km in overall length, weighing about 20 kg. Such a harness might contain over 1000 wires, each requiring connectors at either end and taking up to six hours to build. Not only does this represent a cost and weight penalty, it can also create major 'bottlenecks' at locations such as door hinges, where it becomes almost impossible to physically accommodate the 70-80 wires required. Now, if the motor switching, reversing or speed control were to be done at the load by semiconductor switches, these in turn can be driven via much thinner, lighter wiring thus alleviating the bottlenecks. Even greater savings - approaching the weight of a passenger - can be achieved by incorporating multiplex wiring controlled by a serial bus.

Types of motors used in automobiles

Motor design for automotive applications represents an attempt at achieving the optimum compromise between conflicting requirements. The torque/speed characteristic demanded by the application must be satisfied while taking account of the constraints of the materials, of space and of cost.

There are four main families of DC motors which are, or which have the potential to be used in automobiles.

Wound field DC Commutator Motors

Traditionally motors with wound stator fields, a rotor supply fed via brushes and a multi-segment commutator - see Fig.1 - have been widely used. Recently, however, they have been largely replaced by permanent magnet motors. Characteristically they are found with square frames. They may be Series wound (with high torque at start up but tends to 'run away' on no-load), Shunt wound (with relatively flat speed/torque characteristics) or (rarely) Compound wound.

Permanent Magnet (PM) DC Commutator Motors

These are now the most commonly used motors in modern cars. The permanent magnet forms the stator, the rotor consists of slotted iron containing the copper windings - see Fig.2. They have a lighter rotor and a smaller frame size than wound field machines. Typical weight ratios between a PM and a wound field motor are:

Copper	1:10
Magnets	1:7
Rotor	1:2.5
Case	1:1

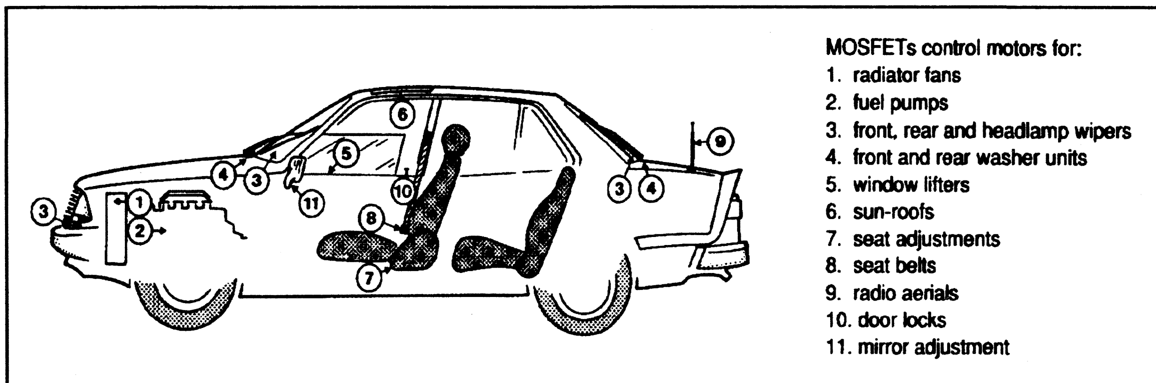


Table 1 Typical motor and switch requirements in top of range car.

motor application	typical power (W)	nominal current (A)	typical number of such motors	type of drive	typical number of switches per motor	proposed standard BUK-	MOSFET* L²FET BUK-	comments
air-conditioning	300	25	1	unidirectional, variable speed	1	456	556	Active suspension may also require such high power motors
radiator fan	120-240	10-20	1	unidirectional, variable speed	1	455	555	These motors may go brushless, requiring 3 to 6 lower rated switches
fuel pump	100	8	1	unidirectional	1	453	553	
wipers: front			1-2	unidirectional, variable speed				Reversing action is at present mechanical. This could be done electronically using 2 or 4 switches
rear	60-100	5-8	1		1	452/453	552/553	
headlamp			2					
washers: front			1-2					
	30-60	2.5-5		undirectional	1	452	552	
rear			1-2					
window lifter	25-120	2-10	2-4	reversible	4	452/455	552/555	
sun-roof	40-100	3.5-8	1	reversible	4	452/453	552/553	
seat adjustment (slide, recline, lift, lumbar)	50	4	4-16	reversible	4	453	553	
seat belt	50	4	2-4	reversible	4	453	553	
pop-up headlamp	50	4	2	reversible	4	453	553	
radio aerial	25	2	1	reversible	4	452	552	
door lock	12-36	1-3	6-9	reversible	4	451/452	551/552	
mirror adjustment	12	1	2	reversible	4	451	551	

* These are meant for guidance only. Specific applications should be checked against individual users requirements. In addition to standard and L²FETs, FredFETs, SensorFETs and IPS might be considered. Also a variety of isolated and non-isolated package options are available

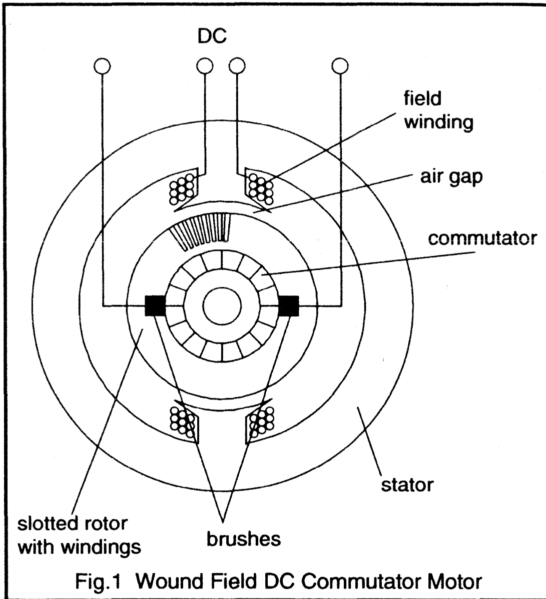


Fig.1 Wound Field DC Commutator Motor

PM motors have a linear torque/speed characteristic - see Fig.3 for typical curves relating torque, speed, current and efficiency. (Philips 4322 010 76130). They are generally used below 5000 rpm. Their inductance (typically 100 - 500 µH) is much lower than wound field machines. New materials (e.g. neodymium iron boron compounds) offer even more powerful fields in smaller volumes.

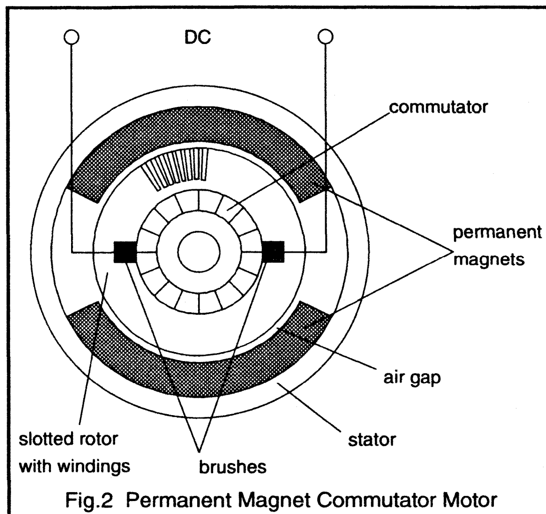


Fig.2 Permanent Magnet Commutator Motor

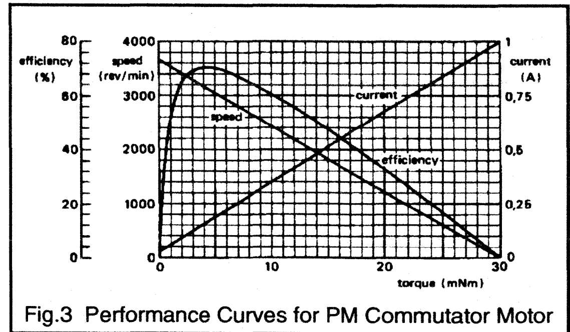


Fig.3 Performance Curves for PM Commutator Motor

PM Brushless DC Motors

Although common in EDP systems, brushless DC motors are not yet extensively used in cars. They are under consideration for certain specialised functions, e.g. fuel pump where their 'arc free' operation makes them attractive. They have a wound stator field and a permanent magnet rotor - Fig.4. As their name suggests they have neither mechanical commutator nor brushes, thus eliminating brush noise/wear and associated maintenance. Instead they depend on electronic commutation and they require a rotor position monitor, which may incorporate Hall effect sensors, magneto resistors or induced signals in the non energised winding. Thanks to their lightweight, low inertia rotor they offer high efficiency, high power density, high speed operation and high acceleration. They can be used as servos.

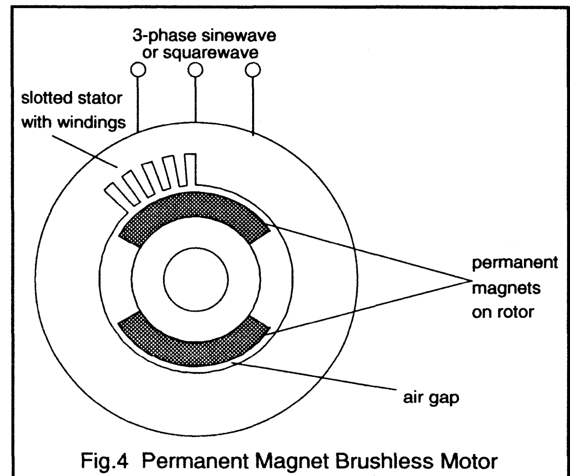


Fig.4 Permanent Magnet Brushless Motor

Switched Reluctance Motors

These motors - see Fig.5 - are the wound field equivalent to the PM brushless DC machine, with similar advantages and limitations. Again, not yet widely used, they have been

proposed for some of the larger motor applications such as radiator and air conditioning fans, where their high power/weight ratio makes them attractive. They can also be used as stepper motors in such applications as ABS and throttle control.

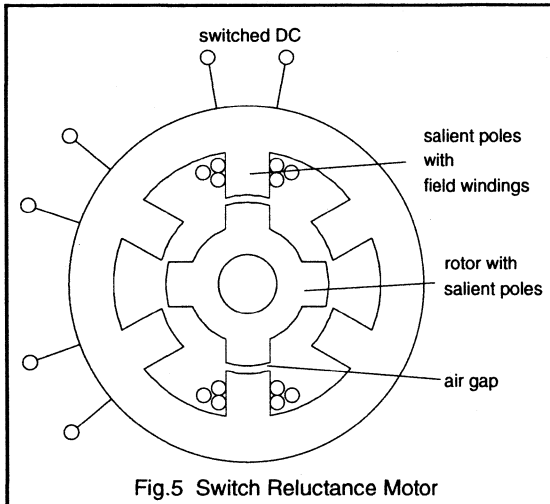


Fig.5 Switch Reluctance Motor

Motor drive configurations

The type of motor has a considerable influence on the configuration of the drive circuit. The two families of DC motors, commutator and brushless need different drive circuits. However suitably chosen MOSFETs can be used to advantage with both.

Commutator Motors

Both permanent magnet and wound field commutator motors can be controlled by a switch in series with the DC supply - Fig.6. Traditionally relays have been used, but they are not considered to be very reliable, particularly in high vibration environments. Semiconductors offer an attractive alternative, providing that :

- low on-state voltage drop. Some authorities require that it should be <10% of the supply voltage at maximum current, others say <1V.
- low drive power requirements.
- immunity from vibration.

The Power MOSFET scores on all counts, offering ON resistances measured in mΩ and requiring only a few volts (at almost zero current) at the gate, to achieve this.

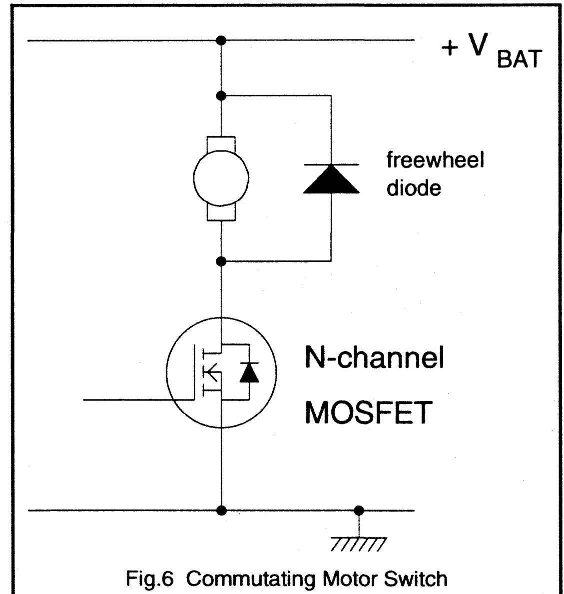


Fig.6 Commutating Motor Switch

When a motor is switched off, it may or may not be running. If it is, then the motor acts as a voltage source and the rotating mechanical energy must be dissipated either by friction or by being transformed into electrical energy and returned to the supply via the inherent anti-parallel diode of the MOSFET. If it is not turning, then the motor appears as purely an inductance and for a low side switch the voltage transient developed will take the MOSFET into avalanche. Now, depending on the magnitude of the energy stored in the field and the avalanche capability of the MOSFETs, a diode in parallel with the motor may or may not be required. That is, if

$$\frac{1}{2}.L_m I_m^2 < W_{DSS}$$

then no diode needed.

Reversing the polarity of the supply, to a commutator motor, reverses the direction of rotation. This usually requires an H bridge of semiconductors, see Fig.7. In this case the built in diodes, inherent in MOSFETs, mean that no extra diodes are necessary. It should be noted that there are now two devices in series with the motor. So, to maintain the same low level of on-state voltage drop, each MOSFET must be doubled in area. With four devices in all, this means a reversing H bridge requires 8 x the crystal area needed by a unidirectional drive.

Chopping the supply controls the mean voltage applied to the motor, and hence its speed. In the case of the H bridge TR1 and TR4 might be used to control direction, while a chopping signal (typically 20kHz) is applied to TR3 or TR2.

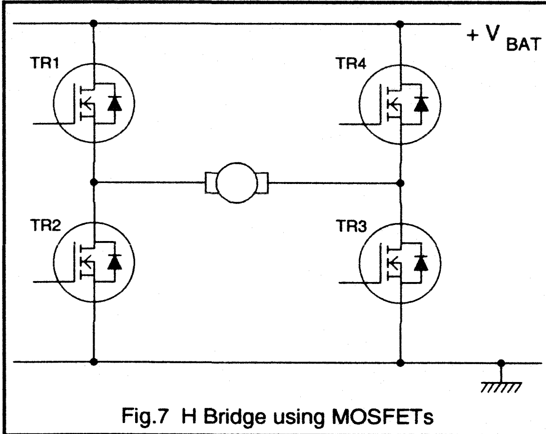


Fig.7 H Bridge using MOSFETs

When reversing the direction of rotation, it is preferable to arrange the gating logic so that the system goes through a condition where TR1, TR2, TR3 and TR4 are all off.

Adding current sensing to the circuit would allow the motor torque to be monitored, controlled or limited. Unfortunately, standard current monitoring methods increase the on-state voltage drop and reduce efficiency. However lossless sensing can be achieved by using SensorFETs for TR2 and TR3.

Switched Field Motors

PM brushless motors typically require 6 switches to generate the rotating field, see Fig.8. Although there are motors, which operate at lower power density, which can be driven from 3 switches. The circuit in Fig.9 shows a low side switch version of such a drive. A similar arrangement with high side switches would be possible.

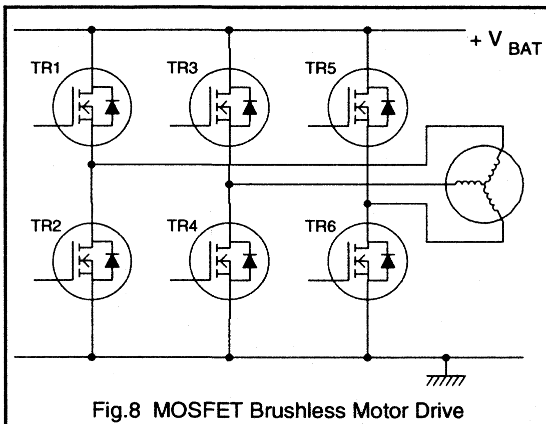


Fig.8 MOSFET Brushless Motor Drive

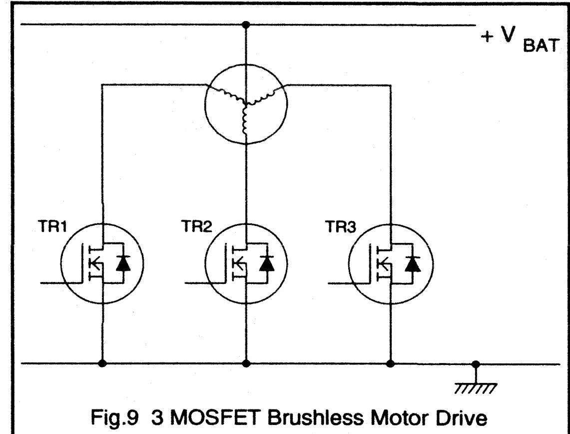


Fig.9 3 MOSFET Brushless Motor Drive

Switched reluctance motors may use as few as 4 or as many as 12 switches to generate the rotating field, a 4 switch version is shown in Fig.10.

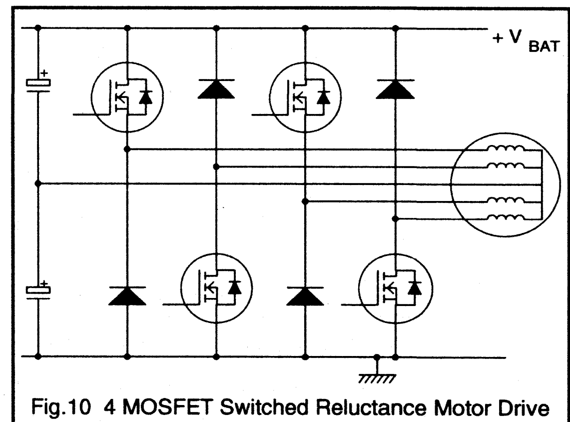


Fig.10 4 MOSFET Switched Reluctance Motor Drive

The speed and direction of all switched field motors is controlled by the timing of the field pulses. In the case of brushless DC machines these timing pulses can be derived from a dedicated IC such as the Philips NE5570. Rotor position sensing is required - using, for example, magnetoresistive sensors - to determine which windings should be energised. Compared with a DC commutator motor, the power switches for a brushless motor have to be fast, because they must switch at every commutation. PWM speed control pushes up the required switching speed even further. Philips MOSFETs are designed so that both switch and inbuilt diode are capable of efficient switching at the highest frequencies and voltages encountered in automotive applications.

High side drivers

Often, in automobiles, there is a requirement for the switch to be connected to the positive battery terminal with the load connected via the common chassis to negative. Negative earth reduces corrosion and low side load is safer when loads are being worked on or replaced. Also, when H bridges are considered the upper arms are of course high side switches.

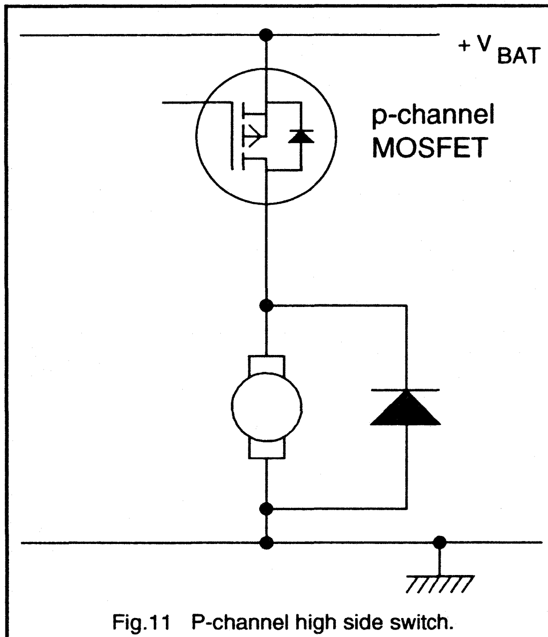


Fig.11 P-channel high side switch.

There are two MOSFET possibilities for high side switches:

- **P-channel switches**. These simplify the drive circuit which only needs referencing to the positive supply, see Fig.11. Unfortunately p-channel devices require almost three times the silicon area to achieve the same on resistance as n-channel MOSFETs, which increases cost. Also P-channel devices that can be operated from logic level signals are not readily available.
- **N-channel switches.** To ensure that these are fully turned on, the gate must be driven 10 V higher than the positive supply for conventional MOSFETs or 5 V higher for Logic Level types. This higher voltage might be derived from an auxiliary supply, but the cost of 'bussing' this around the vehicle is considerable.

The additional drive can be obtained locally from a charge pump, an example in shown in Fig.12. An oscillator (e.g Philips AU7555D) free runs to generate a rectangular 12 V waveform, typically at around 100kHz. A voltage doubler then raises this to around twice the battery voltage. This arrangement is equally suitable for 'DC' or chopper drives.

An alternative approach for H bridge choppers is to use the MOSFETs themselves to generate the drive voltage with a bootstrap circuit as shown in Fig.12. This circuit works well over a range of mark-space ratios from 5% to 95%. Zener diodes should be used in this circuit to limit the transients that may be introduced onto the auxiliary line.

Currents in motor circuits

There are 5 classes of current that can flow in a motor circuit:-

- **nominal** - this is the maximum steady state current that will flow when the motor is performing its function under normal conditions. It is characterised by its relatively low level and its long duration.
- **overload** - this is the current which flows when the motor is driving a load greater than it is capable of driving continuously, but is still performing its function i.e not stalled. This is not necessarily a fault condition - some applications where the motor is used infrequently and for only a short time, use a smaller motor, than would be needed for continuous operation, and over-run it. In these cases the nominal current is often the overload current. Overload currents tend to be about twice the nominal current and have a duration between 5 and 60 seconds.

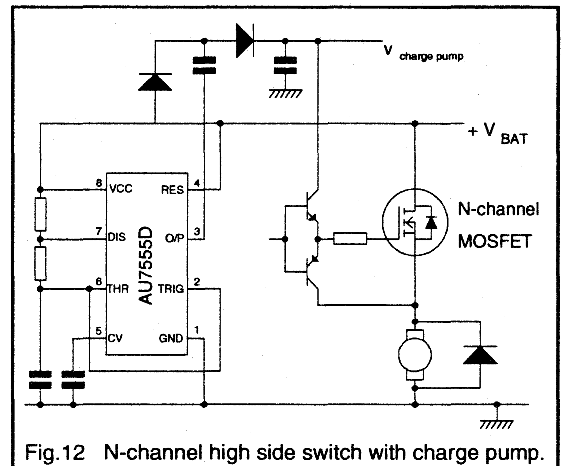


Fig.12 N-channel high side switch with charge pump.

- **inrush** - or starting currents are typical 5 to 8 times the nominal current and have a duration of around 100 ms, see Fig.14. The starting torque of a motor is governed by this current so if high torque is required then the control circuit must not restrict the current. Conversely if starting torque is not critical, then current limiting techniques can be employed which will allow smaller devices to be used and permit sensitive fault thresholds to be used.

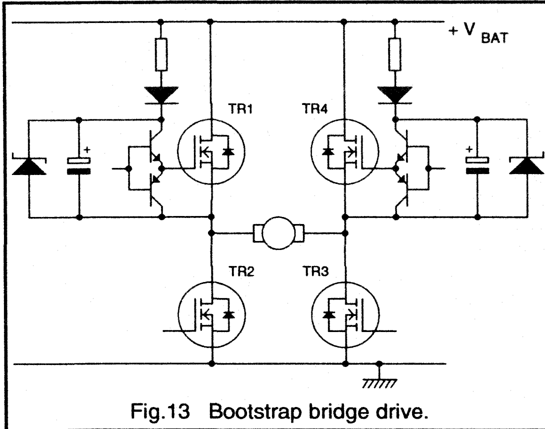


Fig.13 Bootstrap bridge drive.

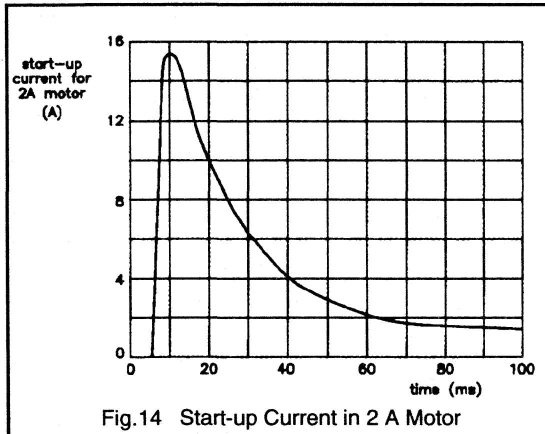


Fig.14 Start-up Current in 2 A Motor

- **stall** - if the motor cannot turn then the current is limited only by the series resistance of the motor windings and the switch. In this case, a current of 5-8 times the running current can flow through the combination. Fig.15 shows the current that flows through a stalled 2 A motor - the current gradually falls as the temperature, and consequently the resistance, of the motor and the MOSFET rises.

- **short circuit** - if the motor is shorted out then the current is limited only by the resistance of the switch and the wiring. The normal protection method, in this case, is a fuse. Unless other current control methods are used then it is the I^2t rating of the fuse which determines how long the current will flow.

It is important that the devices, selected for the control circuit, can operate reliably with all of these currents. With some types of switching device, it is necessary to select on the basis of the absolute maximum current alone. Often this results in a large and expensive device being used. The

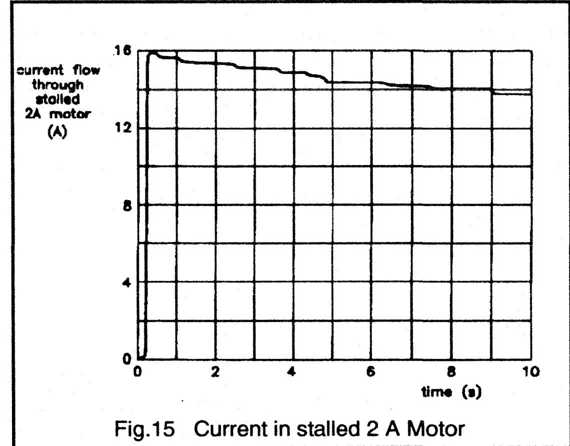


Fig.15 Current in stalled 2 A Motor

characteristics of MOSFETs, in particular their thermally limited SOAR (no second breakdown), allows the designer to specify a much smaller device whose performance more closely matches the needs of the circuit.

Current control with SensorFETs

The introduction of semiconductor switches allows the designer to add current limiting features to the control circuit. Some means of monitoring the current now becomes essential. Whilst it would be possible to use series sensing resistors to detect overload current these tend to be expensive. They also dissipate power and result in an unwelcome voltage drop during normal running. Additionally. if conventional resistors are used their inductance results in the generation of voltage spikes. Fig.16 shows the voltage drop across a 0.03 Ω conventional resistor, in series with the source of a MOSFET, monitoring the start-up of a motor. The inductive overshoot and ringing can be seen.

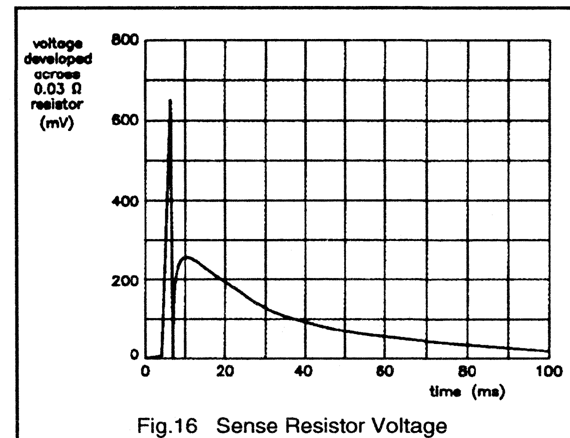


Fig.16 Sense Resistor Voltage

SensorFETs, on the other hand, such as the BUK793-50 or BUK795-50, can provide 'loss-less' current sensing. With these devices a separate connection to a few of the source cells is brought out. Thanks to the inherently good cell matching the sense current is a known proportion of the total. Feeding this sense current through a low power resistor results in a voltage which, with suitable circuitry, can be used to limit or shut down the SensorFET gate drive in the event of an overcurrent. This subject is discussed in greater depth in reference 1

L²FETs

The supply voltage in an automobile derived from the battery is only 12 V (nominal). This can vary from 10.5 V to 16 V under normal operation. It is important that the MOSFET switches be fully turned on under these conditions, not forgetting that for high side switches it may be necessary to derive the gate drive from a charge pump or bootstrap.

Whilst a gate source voltage of 6 V is usually sufficient to turn a conventional MOSFET on, to achieve the lowest on resistance 10 V is required. Thus the margin between available and required gate drive voltage may be quite tight in automotive drive applications.

One way to ease the problem is to use Logic Level MOSFETs (L²FET), such as the BUK553-60A or BUK555-60A, which achieve a very low on resistance state with only 5 V gate-source.

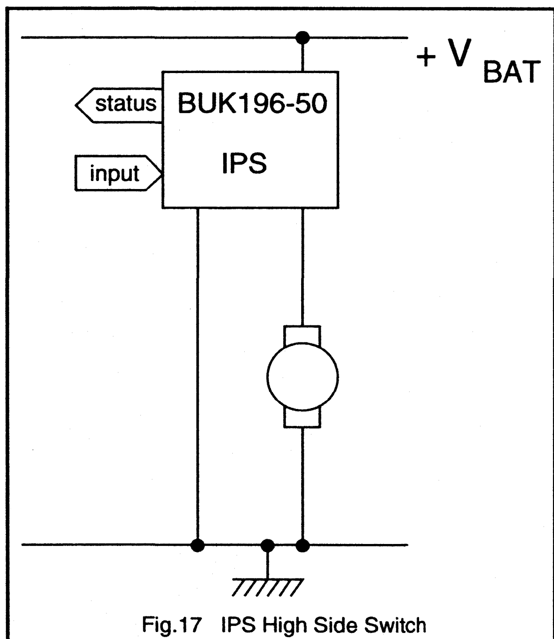


Fig.17 IPS High Side Switch

Intelligent Power Switch

The ideal high side switch to drive motor loads would be one which could be switched on and off by a ground referenced logic signal, is fully self-protected against short circuit motors and over temperatures and is capable of reporting on the load status to a central controller.

The Philips response to these requirements is the BUK196-50 Intelligent Power Switch; which features on board charge pump and level shifting, short circuit and thermal protection and status reporting of such conditions as open or short circuit load. With an on resistance of 33mΩ the BUK196-50 is capable of driving motors of up to 11A. (fig 17)

Table 2 Conditions Affecting Abnormal Supply Voltages

Voltage Range	Cause
>50 (60)*	coupling of spurious spikes
30 to 50	clamped load dump
22 to 30	voltage surge on cut-off of inductive loads
16 to 22 (32 to 40)*	jump start or regulator degraded
10.5 to 16 (20 to 32)*	normal operating condition
8 to 10.5	alternator degraded
6 to 8 (9 to 12)*	starting a petrol engine
0 to 6 (0 to 6)*	starting a diesel engine
negative	negative peaks or reverse connected battery

* 24 V supply

Device requirements

Voltage

The highest voltage encountered under normal operation is 16 V, under jump start this can rise to 22 V. In the case where the battery becomes disconnected with the alternator running the voltage can rise to 50 V (assuming external protection is present) or 60 V in the case of 24 V vehicles see table 2. Thus the normal voltage requirement is 50/60v, however the power supply rail in a vehicle is particularly noisy. The switching of the numerous inductive loads generates local voltage spikes and surges of both polarities. These can occur singly or in bursts, have magnitudes of 100 V or more and durations of the order of 1ms - see reference 2

It is important to chose MOSFETs capable of withstanding these stresses, either by ensuring V_{DS} exceeds the value of the transients or by selecting 50/60 V devices with sufficient avalanche energy capability to absorb the pulse. For transients in excess of these values it is necessary to provide external protection.

Temperature

The ambient temperature requirement in the passenger compartment is -40 to +85˚C , and -40 to +125˚C under the bonnet. All Philips MOSFETs shown in Table 1 have T_{jmax} = 175˚C.

Conclusions

There is an increasing demand for low cost, reliable electronic switching of motors in automobiles. Despite the wide variety of motor types and drive configurations there is a Philips Power MOSFET solution to all of these demands. The broad range of types includes L^2FETs, SensorFETs, FredFETs and devices with on-chip Intelligence. The combination of low on-state resistance, ease of drive and ruggedness makes them an attractive choice in the arduous automotive environment.

References

1) SensorFETs For Motor Control Applications, chapter 5.1.2.

2) ISO Technical Report 7637

5.1.2 SensorFETs For Motor Control Applications

The integration of current limiting circuitry into modern motor control systems is a key factor in providing the reliability demanded by todays applications. In the absence of any form of restriction, a stall condition will cause an electric motor to pull a current between five and eight times that which flows under normal operating conditions. Excessively high current levels in the drive circuitry can also result from accidental short circuit of the motor terminals. If overcurrent stress of this kind is permitted to occur in motor control systems, the likelihood of damage to both the drive and the motor is high.

Current limiting techniques have traditionally involved the use of either a series resistor or current transformer to monitor the instantaneous current in the switching device. Both techniques present serious disadvantages to the designer. Insertion of a series resistor results in power loss to the circuit which must be dissipated by the resistor. A high power, low resistance, non-inductive component is thus generally required which can add appreciable cost to the system. The alternative method of using a current transformer can also be costly and is usually inconvenient.

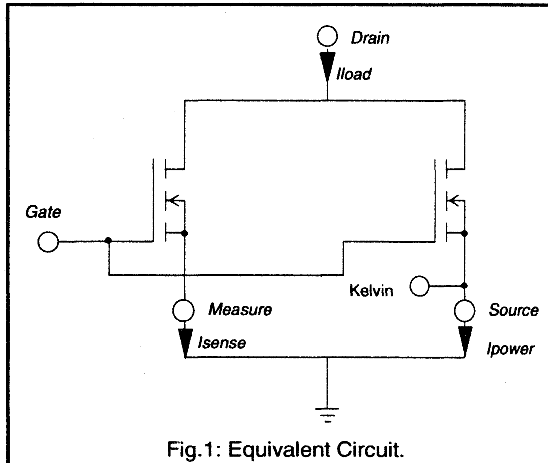


Fig.1: Equivalent Circuit.

The Philips SensorFET offers a new and easy to use approach to the problem of current sensing. The SensorFET is a Power MOSFET which divides the load current into power and sense components. The sense current can be monitored with a cheap, signal level resistor, thus avoiding power loss and presenting circuit designers with a simple and efficient means of current sampling.

Basic Concept

SensorFET design is based upon a separate source connection to a few cells out of the many thousand which go to make up a Power MOSFET. Since each of the individual cells is identical, current is distributed equally between them and with the source potential of both the sense and power parts the same, current will share between the two parts according to the ratio of the on-resistance of each. This ratio is in-turn determined by the ratio of the number of sense cells to the number of power cells and is typically of the order 1:1500 .Fig.1 illustrates how the SensorFET may be represented as two parallel FETs; a low $R_{DS(ON)}$ Power transistor and a high $R_{DS(ON)}$ sense transistor.

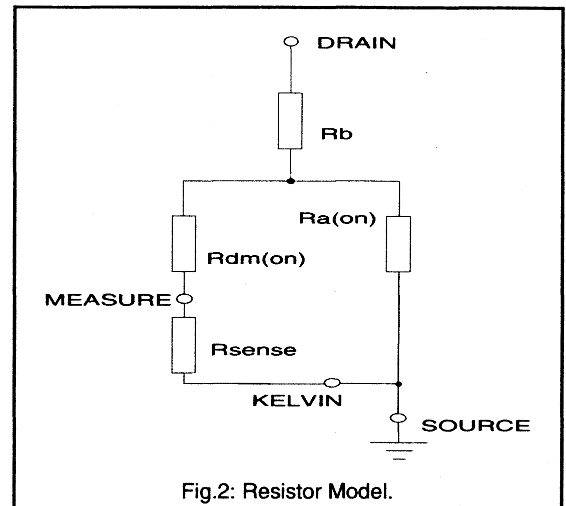


Fig.2: Resistor Model.

Current sensing is achieved by the insertion of a signal level resistor between the measure and kelvin terminals. However should direct amplification of the sense signal be required, the resistor can be replaced by a virtual earth op-amp circuit (this is discussed more fully in reference [1]). The examples given in this article will consider only the method of resistive sensing.

A SensorFET in its on-state may be represented by the model shown in Fig.2. The device is separated into its resistive components distinguishing between the bulk drain resistance, R_B, common to both devices and the active components $R_{DM(ON)}$ and $R_{A(ON)}$. $R_{DM(ON)}$ is the drain to measure on-state resistance with $R_{A(ON)}$ being the active component for the power part. R_{sense} represents the external sense resistor. Using this model the equation which describes the sense voltage is simply:

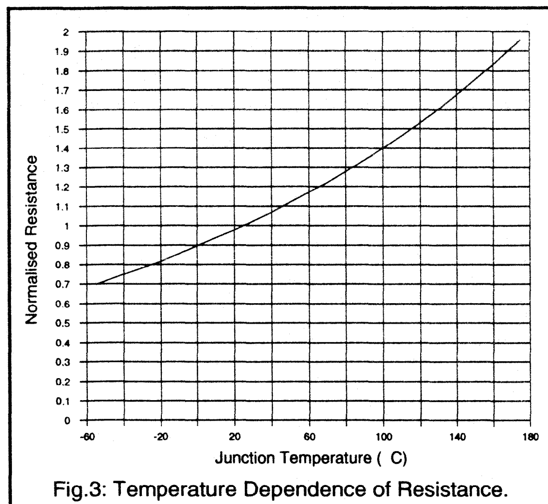


Fig.3: Temperature Dependence of Resistance.

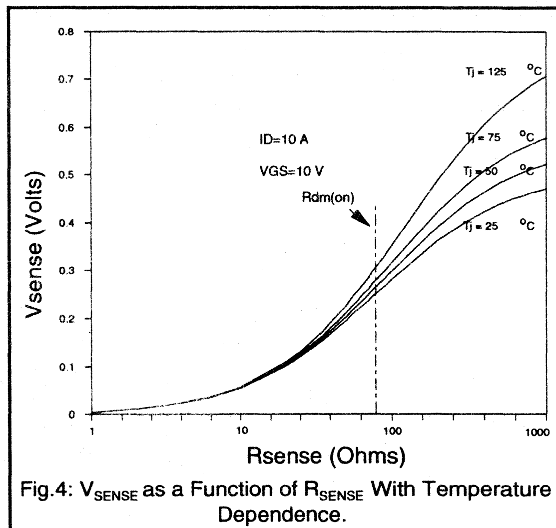


Fig.4: V_{SENSE} as a Function of R_{SENSE} With Temperature Dependence.

$$V_{SENSE} = R_{SENSE} \cdot \frac{I_D \cdot R_{A(ON)}}{(R_{DM(ON)} + R_{SENSE})} \quad .....1$$

Equation (1) may be re-arranged to give expressions for R_{sense} and I_D, equations 2 and 3.

$$R_{SENSE} = \frac{V_{SENSE} \cdot R_{DM(ON)}}{\{(I_D \cdot R_{A(ON)}) - V_{SENSE}\}} \quad ......2$$

$$I_D = V_{SENSE} \cdot \frac{(R_{SENSE} + R_{DM(ON)})}{(R_{A(ON)} \cdot R_{SENSE})} \quad ......3$$

From equation 1, if R_{SENSE} is made very large compared to $R_{DM(ON)}$, V_{SENSE} becomes equal to I_D $R_{A(ON)}$. This value is clearly the maximum sense voltage that can be obtained and as such represents the compliance of the measure terminal. A value for $R_{A(ON)}$ may be determined from the potential between the measure and Kelvin terminals with the measure terminal open circuit, $R_{A(ON)} = V_{SENSE} / I_D$. A value for $R_{DM(ON)}$ can be gained from $R_{DM(ON)} = R_{A(ON)} \cdot n$ where n is the drain to measure current ratio. Since R_B will be very small compared to $R_{DM(ON)}$, the latter may also be measured directly as the drain to measure on-state resistance.

Reference was made above to the connection of the sensing resistor between the measure and kelvin terminals. The kelvin terminal is an additional connection to the power source which must be used if accuracy is to be maintained. The current sensing technique involves sense voltages typically less than 300 mV. If sensing voltages of this magnitude were measured with respect to natural ground, the effect of current flowing from the power source into a ground impedance could easily introduce noticeable sensing errors [1]. Sense voltages must therefore always be measured with respect to the kelvin terminal.

Choosing R_{SENSE}

Consider first the case where R_{SENSE} is set to zero. This implies that V_{SENSE} is also zero and that the sense current is exactly predicted by the drain to measure current ratio, n. The latter is relatively insensitive to operating temperature and is specified in data to have a tolerance of ± 5 %. Consider now the other extreme with R_{SENSE} set to infinity. The sense current is obviously zero while the sense voltage is determined simply by the product of $I_D R_{A(ON)}$. Being a majority carrier device, power MOSFET resistances have a positive temperature dependence. This is illustrated for the $R_{DM(ON)}$ and $R_{A(ON)}$ of a BUK793-60A in Fig.3. The implication here is for a sense voltage variation of nearly 100 % between 25 °C and 150 °C in the case where R_{SENSE} is set to infinity. In addition data tolerances on the resistance allow a difference of up to 50 % between typical and maximum values. The accuracy with which V_{SENSE} may be used to reflect the drain current with large values of R_{SENSE} is therefore relatively low. Accuracy improves as R_{SENSE} is reduced and approaches a maximum as R_{SENSE} tends to zero.

As a general rule R_{SENSE} should be chosen to be less than the drain to measure on-resistance $R_{DM(ON)}$ (Fig.4). This is necessary for the preservation of accuracy and to ensure current sensing is made relatively independent of device tolerances and junction temperature. (A full treatment of the effect of sense resistance on current sensing accuracy is presented in reference [1].)

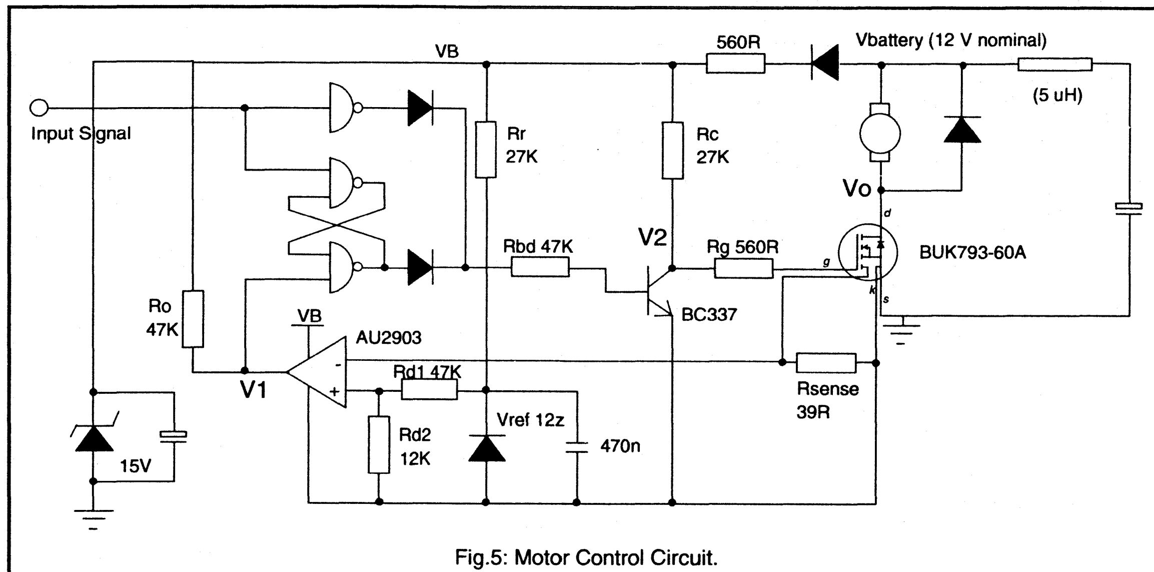


Fig.5: Motor Control Circuit.

Designing For Overcurrent Protection

An example of how the SensorFET can be used in the control of a fractional horsepower d.c. motor is illustrated in Fig.5. The circuit is configured to operate off a 12 V (nominal) battery supply and provide overcurrent protection in the event of a short circuit. Should the drain current exceed a value of 15 A the SensorFET will switch off and may only be switched back on by resetting and then reapplying the input signal.

CIRCUIT DESCRIPTION. The input signal is inverted and diode OR'd with the output of an overcurrent drive suppression flip-flop. The resultant signal operates an npn bipolar transistor which provides the voltage drive for the BUK793-60A SensorFET. The latter is a 60 V, 20 A device with an $R_{DS(ON)}$ rating of 0.1 Ω @ 25 ˚C. The voltage developed across R_{SENSE} is fed to the inverting input of the current limit comparator where it is compared with a stabilised voltage reference, derived from a bandgap device and a voltage divider network. A High to Low transition at the comparator output triggers the Set input of the overcurrent flip-flop which suppresses drive to the SensorFET. Reset only occurs on removal of the input signal. NB. In the design of this circuit the values of R_C, R_{BD}, R_R, R_{D1} and R_{D2} have been chosen to minimise the standby current.

DESIGNING THE CURRENT SENSING CIRCUIT. An idea on a suitable value for the sense voltage may be gained from the data curve example shown in Fig.4. If only R_{SENSE} values lower than $R_{DM(ON)}$ are considered, for a drain current of 10 A, V_{SENSE} must be less than 300 mV. Applying this same upper limit at 15 A, a value of 250 mV was chosen as the reference level for triggering the gating circuitry.

Providing a 250 mV reference for the comparator is accomplished with the ref 12z 1.26 V bandgap device and a voltage divider network. To provide a stable reference the ref 12z requires a minimum quiescent current of 90 μA. This current must be supplied from the minimum battery voltage at which the system is required to function, (chosen to be 6.5 V for this example). Using preferred resistor values for the divider network an actual reference voltage of 256 mV was achieved.

The sense resistor value may be calculated from equation 2. Sensing parameters for the BUK793-60A are specified in the data sheet as follows:

	min	typ	max
$R_{DM(ON)}$ @ 25 ˚C Drain-Measure On-State Resistance		80 Ω	120 Ω
I_D/I_M (=n) Drain-Measure Current Ratio	1490	1570	1650

Using the typical values a figure for R_{SENSE} of 41.5 Ω is obtained. Taking the nearest preferred value of 39 Ω, the actual trip current calculated from equation 3 is 15.6 A.

ACCURACY. Substituting the maximum values of $R_{DM(ON)}$, and $R_{A(ON)}$ (derived from the maximum value of n) into equation 3 yields the minimum trip current that could result due to parameter tolerances. This value at a junction

temperature of 25 ˚C is 14.5 A. The nature of the SensorFET process ensures that $R_{DM(ON)}$ will not fall significantly below the typical value. The maximum possible trip current will not therefore deviate significantly from the 15.6 A typical value.

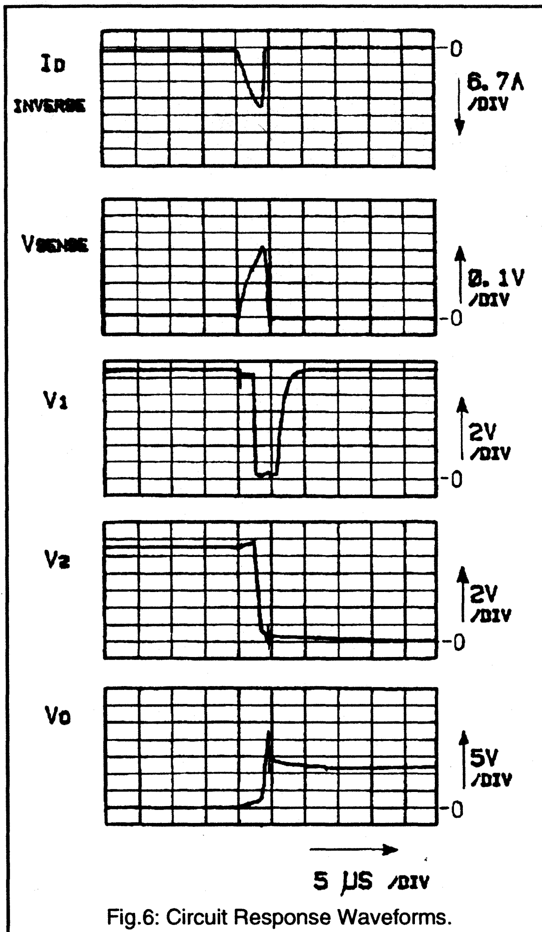


Fig.6: Circuit Response Waveforms.

For most applications the junction temperature of the SensorFET will be raised above 25 ˚C. The effect of temperature on the absolute drain to measure current ratio is minimal since the temperature coefficient of resistance is the same for both the sense part and the power part. However the presence of the external sense resistor in series with $R_{DM(ON)}$ will cause the current sharing to change slightly with temperature. Using the above components the trip current that will result if the junction temperature of the SensorFET were 125 ˚C instead of 25 ˚C may be calculated by substituting the 125 ˚C values of $R_{DM(ON)}$ and $R_{A(ON)}$ (Fig.3) into equation 3. The trip current typical for these conditions is now 13.5 A with a minimum of 13.1 A. (Alternatively R_{SENSE} may be recalculated using the revised 125 ˚C sensing parameters. A value of 34 Ω would ensure a trip current of 15 A at the elevated junction temperature.)

CIRCUIT FEATURES. To avoid sensing errors through ground loops and loop impedances it is necessary to reference the sensing circuitry to the kelvin terminal ground and not the power source ground. The kelvin terminal thus forms a signal ground for the sense resistor and comparator circuitry. (NB It is important that the comparator supply and the voltage reference be referred to the signal ground.)

The power supply for the drive and sensing components is taken directly from the battery supply and decoupled using diode D1 and a 100 µF capacitor referenced to power ground. The 500 Ω resistor and 15 V zener ensure a maximum supply voltage of 15 V. (It is recommended that decoupling capacitors on the signal side are referenced to the power ground to avoid the possibility of large current transients in the kelvin connection.)

CIRCUIT PERFORMANCE. The response of the overcurrent detection circuitry to a short circuit applied across the motor is shown in Fig.6. The current trip is designed to respond when the source current reaches 15.6 A. However the large signal response time of the AU2903 is typically 300 ns such that the source current has risen to 17.8 A prior to a change in the output of the comparator. An additional delay of 1.4 µs is incurred due to the slow turn-on speed of the bipolar drive transistor. The latter is limited by the high value of R_{BD}. The total response time between the moment the current exceeds 15.6 A and the turn-off of the SensorFET is thus 1.7 µs and results in the source current rising to 23.5 A prior to switch-off. (NB The dI/dt is limited by the 5 µH taken to be representative of the supply lead inductance.) The standby current of this circuit with a battery voltage of 14 V was 1.5 mA.

PWM Motor Control

The design requirements of the previous example were limited only to providing the power device with protection in the event of a short circuit condition. Protecting both motor and drive against the motor stall condition was not considered. This second example illustrates how the same circuitry may be used in PWM motor control and demonstrates protection in the event of a motor stall condition. The motor stall characteristic is shown in Fig.8 for a 2 A dc motor. To fully protect the power device without having to resort to excessive heatsinking, the overcurrent protection circuitry is now designed to operate when the drain current exceeds a value of 9 A. This is achieved in the circuit by reducing the reference voltage from 0.256 V to 0.143 V by a simple change to resistor R_{D2} from 12 kΩ to 6 kΩ. (From equation 3 the exact trip current is 8.7 A.)

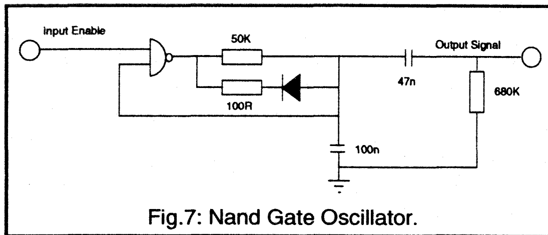


Fig.7: Nand Gate Oscillator.

For this example a 1 kHz, 99 % duty cycle signal was generated using a Nand gate oscillator as shown in Fig.7, (NB this signal is gated according to the status of the input enable). At this frequency the gate drive impedance used for straight dc switch operation is too high and must be reduced. To this end R_C was reduced from 27 kΩ to 3.9 kΩ however the consequence of this was to increase the standby current to 4.5 mA. (As an alternative the bipolar drive stage may be replaced by a HEF4049 Inverter Buffer IC.)

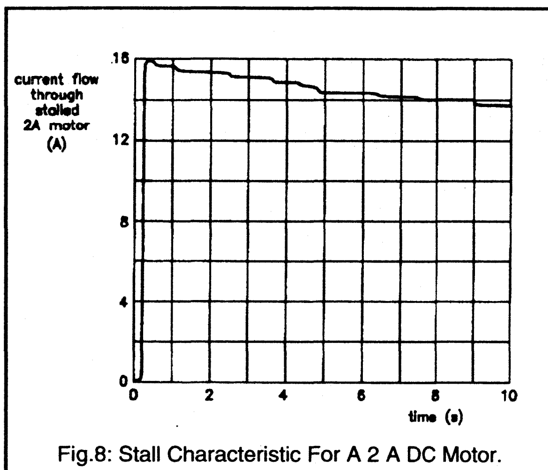


Fig.8: Stall Characteristic For A 2 A DC Motor.

CIRCUIT PERFORMANCE. In PWM drives it is important that the current limit loop should not be allowed to oscillate at its natural frequency. Such oscillation would likely be of very high frequency and be in itself destructive due to incorrect switching of the power device. The circuitry illustrated in Fig.5 ensures that this cannot happen by synchronising the current protection circuitry to the input signal. The current suppression flip-flop is reset only when the oscillator signal goes low. This performance is demonstrated in Fig.9 which shows the response of the circuit in the event of a stall condition. Fig.9a shows the sense voltage envelope with the stall beginning at the second horizontal division. Expanded traces of the sense voltage and oscillator signal in Figures 9b and 9c show the peak current being limited below 8.8 A and the duty cycle reduced below 30 %. (Sense voltage is used here to represent drain current, 0.144 V is equivalent to 8.8 A.)

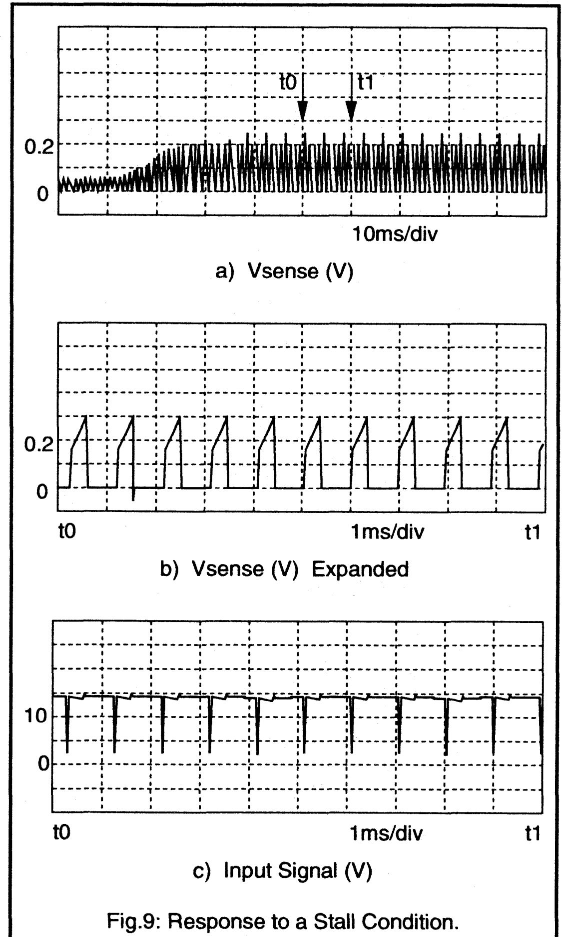


Fig.9: Response to a Stall Condition.

The current limiting circuitry thus maintains the power dissipation in the SensorFET at a low level even during the stall condition. In this case the power dissipated by the BUK793-60A is less than 1 W and the stall condition could therefore be tolerated indefinitely. Without current limiting, the stall current for this particular motor would be in the region of 16 A. Excessive heatsinking would then be required to avoid failure of the power device.

NB. When a dc motor is turned on an initial surge current is drawn which is also 5-8 times the running current. In order that the starting torque is not unduly compromised, it is usually necessary to allow a higher than normal current to flow during the start up period. In the above example the

drive suppression flip-flop would need to be gated out for the first 20 ms of operation if the full turn-on surge current was required.

Conclusions

The Philips SensorFET represents a new level of efficiency in the use of current sensing for the enhancement of motor drive reliability. SensorFET current sensing is achieved without the need for the insertion of costly components into the power circuit and thus avoids the extra losses which those components would normally incur. Correct choice of sense resistor is made from a simple expression which relates power circuit current to sense voltage and makes designing with the SensorFET both straightforward and accurate.

The two design examples presented in this article demonstrate how the SensorFET may be used for effective overcurrent protection in low voltage motor drive applications. Both examples are based around the BUK793-60A, a device which has a standard gate technology and hence a nominal gate drive requirement of 10 V. It is however recognised that certain applications demand the switching device to operate with a gate drive of only 5 V. For this purpose the Philips range of SensorFETs also includes Logic Level versions (BUK993-60A/100A and BUK995-60A/100A) which are fully enhanced with a gate source voltage of 5 V.

References

1) An Introduction To The Philips SensorFET, see chapter 1.

Automotive Lamp Control (Including selection guides)

5.2.1 Automotive Lamp Control With Philips MOSFETS

The modern motor vehicle, with its many features, is a complex electrical system. The safe and efficient operation of this system calls for sophisticated electronic control. A significant part of any control system is the device which switches the power to the load. It is important that the right type of device is chosen for this job because it can have a major influence on the overall system cost and effectiveness. This choice should be influenced the nature of the load. This article will discuss the features of the various types of switching device - both mechanical and solid state. These factors will be put into the context of the needs of a device for the control of resistive loads like lamps and heaters. It will be shown that solid state devices allow the designer a greater degree of control than mechanical switches and that the features of Power MOSFETs make them well suited to use in automotive applications.

Choice of switch type

Mechanical or solid-state

Designers of automotive systems now have the choice of either mechanical or solid-state switches. Although mechanical switches can prove be a cheap solution they do have their limitations. Solid-state switches overcome these limitations and provide the designer with several useful additional features.

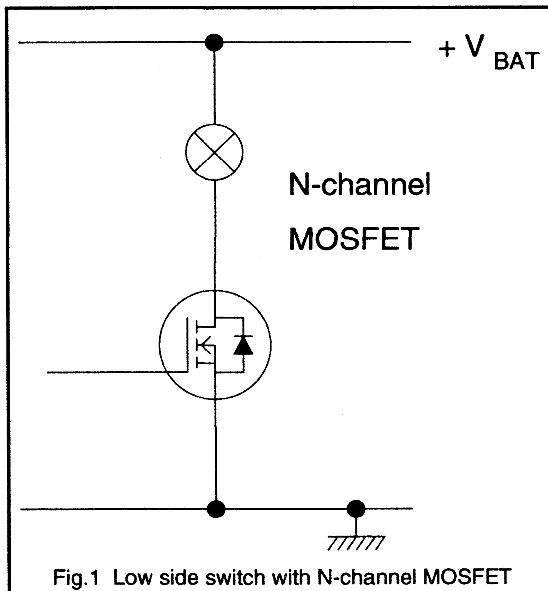


Fig.1 Low side switch with N-channel MOSFET

Areas where the limitations of relays become apparent include:-

- **Reliability** - to achieve the required levels of sensitivity and efficiency means that relay coils have to be wound with many turns of very fine wire. This wire is susceptible to damage under conditions of high mechanical stress - vibration and shock.
- **Mounting** - special assembly techniques are needed when dealing with automotive relays. Their outlines are not compatible with the common methods of automated assembly like auto insertion and surface mounting.
- **Dissipation** - the power loss in the coil of a relay is not negligible - the resulting temperature rise makes it unwise to mount other components in close proximity. In some multiple relay applications it is necessary to provide cooling by ventilation.
- **Temperature** - the maximum operating temperature of relays is typically in the range 70˚C - 85˚C.
- **Corrosion** - the unsealed mechanism of relays are vulnerable in contaminating and corrosive environments.
- **Overloads** - relays can also prove to be unreliable under high transient load conditions. The arcing which occurs when switching high currents and voltages causes contact wear leading eventually to high resistance or even the contacts welding together.
- **Hazardous Materials** - to achieve the prefered switching performance, relays need to use materials like cadmium. The use of such materials is becoming restricted by legislation on health and safety grounds.
- **Noise** - the operation of a relay is not silent. This is proving to be unacceptably intrusive when relays are sited in the passenger compartment.

Solid-state switches can overcome these limitations but can also give the designer the option of introducing the following useful features:-

- **Current limiting** - a relay has two states - on or off so the current which flows depends only on the load. There is no mechanism which allows a relay to regulate the current which flows through it. The best that a relay can do is to try and turn off, when a high current is detected, but because they are so slow, very large currents may be flowing before the relay can react and damage may have already been caused. However the characteristics of solid state devices like MOSFETs and bipolar transistors allow them to control the current. This allows designers the chance to introduce systems which can handle faults in a safe and controlled manner.

- **Control of switching rate** - the lack control that a relay has over the current proves to be a limitation not only during fault conditions but also during normal switching. Without control, the rate at which current changes, dI/dt, depends only on the external circuit and extremely high rates can result. The combination of high dI/dt and the contact bounce that relays are prone to, creates an 'electrically' noisy environment for surrounding systems. The control available with solid-state switches permits the designer to restrain the current and produce 'soft' switching eliminating any possible EMC problems.

Power MOSFET or Bipolar Transistor

All solid-state switches have significant advantages over relays but there are different types of solid-state switch and their particular characteristics need to be taken into account if an optimum choice is to be made. There are two major types of solid-state switches which are suitable for use in automotive applications - power MOSFETs and bipolar transistors - and several factors need to be considered if the optimum choice is to be made.

- **Overload** - The choice of device type can be influenced by the magnitude and duration of overload currents associated with the application - for example the inrush current of lamps. This factor is particularly important because the maximum current that can be safely conducted by a bipolar transistor is independent of its duration. Whereas the safe operating area of a MOSFET allows it to handle short duration currents very much greater than its DC rating.

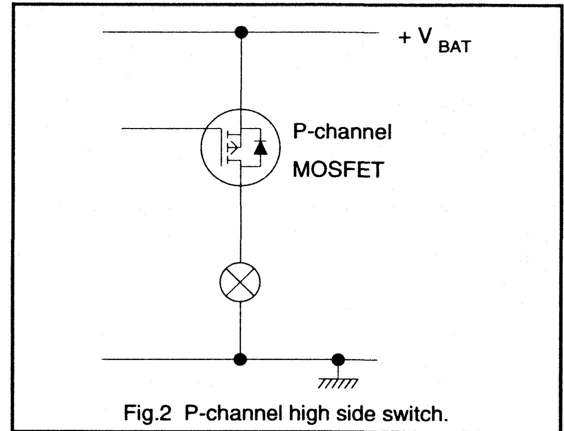


Fig.2 P-channel high side switch.

- **Drive power** - There can be a significant difference between the total power needed to drive bipolar and MOS transistors. A MOSFET's oxide insulation makes it a voltage controlled device whereas a bipolar needs current drive. However, most control circuits are voltage rather than current orientated and the conversion to current operation often involves the used of loss inducing resistors.

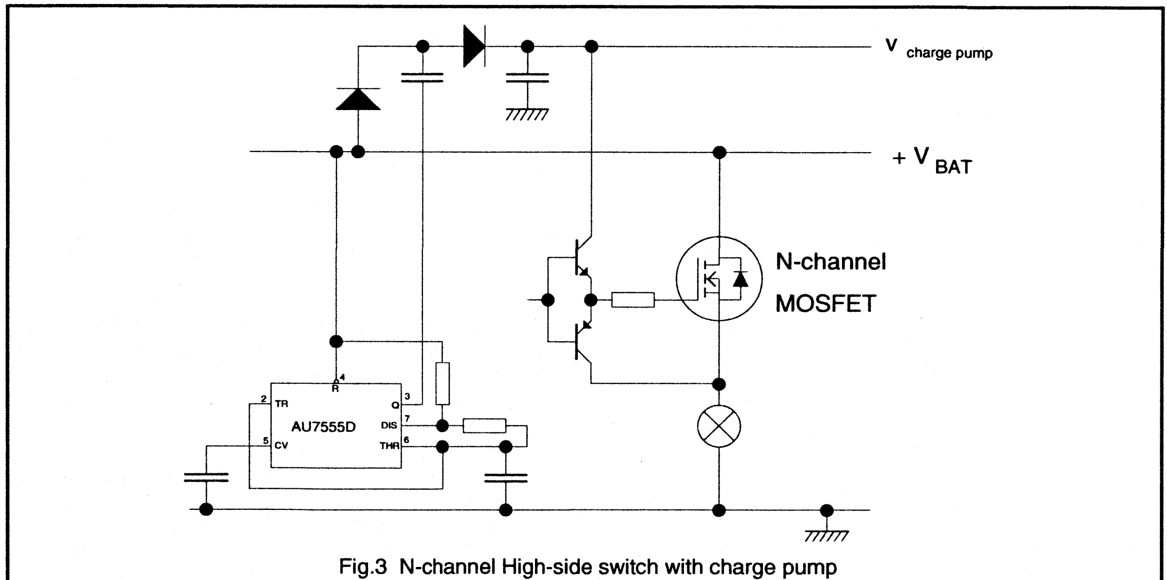


Fig.3 N-channel High-side switch with charge pump

- **Reverse protection** - If the switching device is required to survive reverse conduction conditions then it is necessary to have a diode, connected in anti parallel, around it. If the device is a bipolar transistor then an extra component will be needed. However the device is a MOSFET then it has an inherent body / drain diode which will perform this function without the additional expenditure in components or board space.

Logic level and standard mosfets

The battery voltage in a car is a nominal 12 V. This can vary from 10.5 V to 16 V under normal operation and can fall as low as 6 V during starting. It is important that MOSFET switches be fully turned on at these voltages, bearing in mind that for a high-side switches it may be necessary to derive the gate voltage from a charge pump circuit. While a V_{GS} of 6 V is usually sufficient to turn a standard MOSFET on, 10 V is required to achieve the lowest on-state resistance, $R_{DS(ON)}$. Thus the margin between available and required gate drive voltage may be quite tight in automotive drive applications. One way to overcome this problem is to use L^2FETs such as the BUK553-60A or BUK555-60A, which achieve a very low $R_{DS(ON)}$ with a V_{GS} of only 5 V.

Switch configuration

A load's control circuit can be sited in either its positive or negative feeds. These are referred to as high side and low side switching respectively. Which configuration is chosen often depends on the location of the load/switch and the wiring scheme of the vehicle but other factors like safety can be overriding. The use of semiconductor switches introduces another element into the decision process because of the need to ensure that they are being driven correctly.

Low Side Switch

In this arrangement the load is permanently connected (perhaps via a fuse and the ignition switch) to the positive supply. The switching device is connected between the negative terminal of the load and the vehicle ground. This, together with the almost universal practice of referencing control signals to the vehicle ground, makes the implementation of a low side switch with MOSFETs extremely simple. The circuit shown in Fig.1 shows a MOSFET connected as a low side switch to a lamp load. The Source terminal of the MOSFET is connected to ground so the control signal, which is also referenced to ground, can be connected to the Gate.

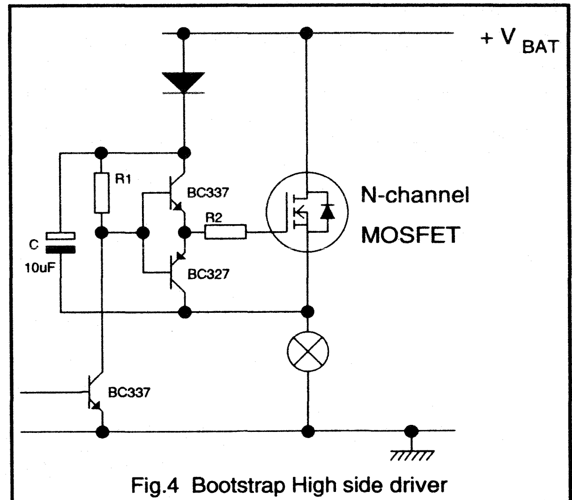


Fig.4 Bootstrap High side driver

High Side Drivers

Often, however, there is a requirement for the switch to be connected to the positive battery terminal with the load connected via the common chassis to the negative. This arrangement reduces electrochemical corrosion and the risk of accidentally activating the device during maintenance.

One method of creating such a high side switch is to use P-channel rather than N-channel MOSFETs. A typical arrangement is shown in Fig.2. In this the source is connected to the +ve feed and the drain to the load. The MOSFET can be turned ON by taking the control line to zero and it will be OFF when the gate is at +ve supply voltage. Unfortunately P-channel MOSFETs require almost three times the silicon area to achieve the same low on-state resistance as N-channel types and so are much more expensive. An additional problem is the difficulty of obtaining P-channel devices with low enough gate threshold voltage to operate reliably at low battery voltages.

Using N-channel devices overcomes these problems but involves a more complicated drive circuit.

To ensure that a n-channel MOSFET is fully turned on, the gate must be driven 10 V higher than its source, for conventional MOSFETs, or 5 V higher for Logic Level (L^2) FETs. With the source connected to the load and with most of the supply being dropped across the it, the gate has to taken to a voltage higher than the supply voltage. This higher voltage might be derived from an auxiliary supply, but the cost of 'bussing' this around the vehicle would be high. Fig.3 shows how this auxiliary supply could be produced locally. It consists of an oscillator - based around

the Philips AU7555D - running at approximately 100 kHz which is driving a charge pump which nearly doubles the supply voltage.

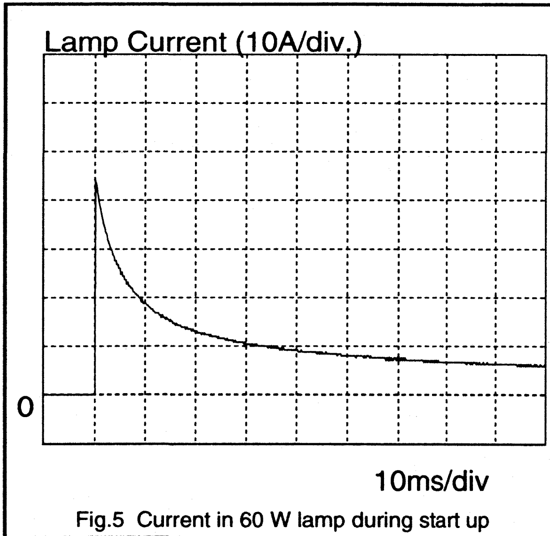


Fig.5 Current in 60 W lamp during start up

An alternative approach, which can be used when the device doesn't have to be continuously ON, for example PWM lamp dimming or lamp flashing, is shown in Fig.4. In this bootstrap arrangement capacitor C is charged to the supply voltage when the MOSFET is OFF. When the MOSFET is turned ON, its source terminal, and the negative end of C, rises to the supply voltage. The potential of the positive end of C is now higher than the +ve supply and diode D is reverse biased preventing C from being discharged. C can now act as the high voltage supply for the gate. The inevitable leakages will tend to discharge C and hence reduce the gate/source voltage, but with good components it is easy to ensure that a voltage high enough to keep the MOSFET fully ON is available for several seconds.

Inrush current

Any circuit or device which is intended to drive either a lamp or a heater must be able to handle not only the normal running current but also the inrush current at start up. All lamps and many heaters are essentially resistors made from metal conductors whose resistivity will increase with temperature.

In the case of lamps, the extremely high operating temperature (3000 K) means that the hot to cold resistance ratio is large. Typical values for a 60 W headlamp bulb are:-

	filament resistance	current
cold (-40°C)	0.17 Ω	70 A
hot	2.4 Ω	5 A

The figures given for the currents assume that there is 12 V across the lamp, in practice wiring and switch resistance will reduce the cold current somewhat, but the ratio will still be large. The actual ratio depends upon the size and construction of the lamp but figures between 10 and 14 are common. For safety, the higher Fig.should be used.

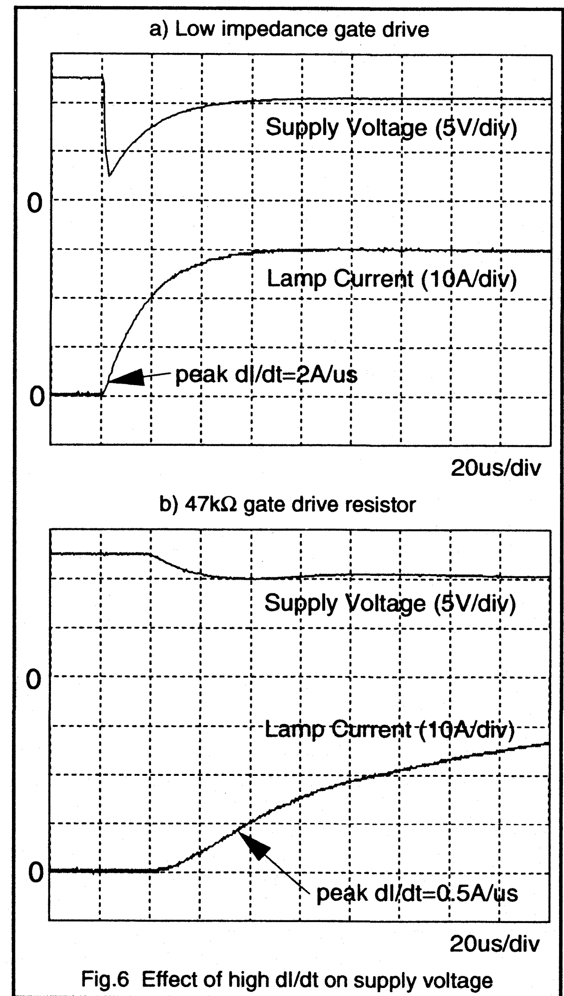


Fig.6 Effect of high dI/dt on supply voltage

TABLE 1 Automotive lamps - characteristics and recommended MOSFET drivers

Load	Typical Power	Nominal Current	Peak Inrush Current	Number of lamps /car	Recommended MOSFET[1] Standard FET SOT186	Standard FET TO220	Logic Level FET SOT186	Logic Level FET TO220
headlamp	60 W 55 W 45 W 40 W	5 A 4.6 A 3.8 A 3.3 A	70 A 64 A 53 A 47 A	2	BUK445-60A	BUK455-60A	BUK545-60A	BUK555-60A
spotlight	55 W	4.6 A	64 A	2	BUK445-60A	BUK455-60A	BUK545-60A	BUK555-60A
front fog light	55 W	4.6 A	64 A	2	BUK445-60A	BUK455-60A	BUK545-60A	BUK555-60A
rear fog light	21 W	1.8 A	25 A	2	BUK442-60A BUK443-60A[2]	BUK452-60A BUK453-60A[2]	BUK542-60A BUK543-60A[2]	BUK552-60A BUK553-60A[2]
front sidelight	5 W	0.4 A	6 A	2	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
rear sidelight	5 W 10 W	0.42 A 0.83 A	5.8 A 12 A	2 2	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
brake light	21 W	1.8 A	25 A	2	BUK442-60A BUK443-60A[2]	BUK452-60A BUK453-60A[2]	BUK542-60A BUK543-60A[2]	BUK552-60A BUK553-60A[2]
direction indicator light	21 W	1.8 A	25 A	4	BUK442-60A BUK443-60A[2]	BUK452-60A BUK453-60A[2]	BUK542-60A BUK543-60A[2]	BUK552-60A BUK553-60A[2]
side marker light	3 W 4 W 5 W	0.25 A 0.33 A 0.42 A	3.5 A 4.7 A 5.8 A	4 4 4	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
license plate light	3 W 5 W	0.25 A 0.42 A	3.5 A 5.8 A	2 1	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
reversing / backup light	21 W	1.8 A	25 A	2	BUK442-60A BUK443-60A[2]	BUK452-60A BUK453-60A[2]	BUK542-60A BUK543-60A[2]	BUK552-60A BUK553-60A[2]
instrument panel light	2.2 W	0.18 A	2.5 A	5	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
courtesy light	2.2 W	0.18 A	2.5 A	4	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
door light	2.2 W	0.18 A	2.5 A	4	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A
boot / bonnet light	2.2 W	0.18 A	2.5 A	4	BUK441-60A	BUK451-60A	BUK541-60A	BUK551-60A

Notes

[1] These are meant for general guidance only. Specific applications should be checked against individual users' requirements. In addition to standard and logic level MOSFETs, SensorFETs and IPS might also be considered.

[2] This device can be used to control two bulbs simultaneously.

TABLE 2 Automotive Resistive Loads - characteristics and recommended MOSFET drivers

Load	Typical Power	Nominal Current	Number /car	Recommended MOSFET[1]			Comments
				TO220	SOT186(A) F-pack	SOT227 ISOTOP	
screen heater	300-600 W	25-50 A	1			BUK516-100 AE	
seat heater	100-120 W	8-10 A	2	BUK452-60A[2]	BUK442-60A[2]		

Notes

[1] These are meant for general guidance only. Specific applications should be checked against individual users' requirements. In addition to standard MOSFETs, L^2FETs, SensorFETs and IPS might also be considered.

[2] To achieve on-state voltage drop of <1 V the BUKxx3-60A device should be used.

The low thermal mass and the high power dissipation (850 W peak in 60W lamp) means that the lamp heats up very quickly. This means that the current falls from its peak value equally quickly. The time it takes for the current to fall back to its normal value depends on the size and construction of the lamp - the larger the lamp the longer it will take to heat up. Typically the current will have an exponentially decay with a time constant of 1 - 10 ms. The waveforms in Fig.5 show the typical inrush current for a 60 W lamp being switched on by a MOSFET. The initial temperature of the lamp filament was 25˚C.

The normal operating temperature of a heater is not as high as that of a lamp, so the inrush current is rarely greater than twice the nominal current and often less. The duration of the 'inrush' can, however, last for many minutes and it may be this current which is used to define the 'normal' operating condition.

Being essentially resistive, lamps and heaters have very low inductance. This means that the current in the load will rise as quickly as the rest of the wiring will let it. This can lead to serious interference problems.

Switch rate

The inductance associated with the supply wires in a car, is not negligible - a Fig.of 5µH is often quoted. This inductance, combined with the high rates of change of current associated with the switching of resistive loads and lamps, results in transient voltage appearing on the supply leads. The magnitude of the transient is given by:-

$$V_{transient} = -L.\frac{dI}{dt}$$

For example a current which rises as slowly as 2 A/µs will cause a 10 V dip in the supply to the switching circuit. This effect can be clearly seen in the waveforms of Fig.6a. Such a perturbation can have an effect in two ways. In the first case the control circuit may be upset by having its supply reduced to only 2 V and may, if not specifically designed to cope with it, fail to function correctly. In the second case, it is easy for a transient as large as this, with its significant high frequency content, to be transmitted into adjacent conductors in the wiring loom. If some of the conductors are signal wires then false triggering of other functions could result.

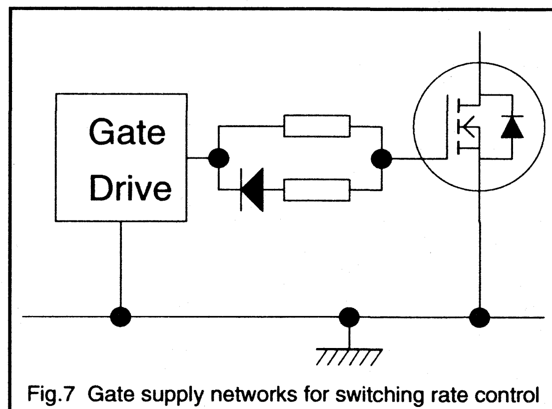


Fig.7 Gate supply networks for switching rate control

The dip will be reduced to manageable proportions if the dI/dt can be held to 0.5 A/µs. Since the loads are resistive, achieving this means reducing the rate that the voltage is applied to the load. This type of 'soft' starting is relatively easy to implement when the controlling device is a Power MOSFET. All that is needed is to put resistance in series with the gate drive.

The plots shown in Fig.6b illustrate the effect inserting 47 kΩ in series with the gate supply of a BUK455-60A. The load for these tests was a 60W lamp being supplied from a battery via a 5 µH inductor. The dip in voltage due to dI/dt is now lost in the voltage drop from the wiring resistance.

The rate at which current falls at turn off is also important. High negative dI/dt will result in a large positive spike on the supply rails. As with the negative dip, this spike could cause interference in adjacent wires but it could also cause overvoltage damage. Unlike the turn on dip which can never

TABLE 3 MOSFET Types and Features

MOSFET Type	Features
Standard	Wide range of current ratings from 5 to >100 A. Wide range of package styles Fast recovery anti-parallel diode (60 / 100 V types) Extremely fast switching.
L^2FET	as standard + Fully operational with low voltage supply
SensorFET	Lossless current sensing.
IPS	Single component providing:- high side switch device protection load protection status reporting CMOS/TTL compatible input

be greater than 12 V, the magnitude of the turn off spike is potentially unlimited. In practice, however, it is extremely unlikely that the voltage would exceed 30 V. Transient voltages of this magnitude are relatively common in the automotive environment and all circuits should be able to withstand them. It is still worthwhile keeping the turn off transient under control by ensuring that the dI/dt is low enough - a Fig.of <1 A/µs is standard.

Soft turn off, like soft turn on, is easy to implement if the controlling device is a Power MOSFET. In fact the same series resistor can be used to limit both the turn on and turn off rates. With a lamp load, however, this method will give a much slower turn off than is really necessary because of the large difference between the current at turn on and turn off. If this is a problem then an additional resistor and diode put in parallel with the first resistor - see Fig.7 - will speed up the turn off.

MOSFET selection

The type of device chosen for a particular application depends upon the features that the control circuit needs to have. For example, a circuit which needs current sensing, as part of a current controlling circuit, may use a SensorFET. Whereas a high side switching circuit with status reporting could, most easily, be implemented with an IPS. Table 3 lists the available MOSFET types and some of their features that would be useful in automotive applications.

Having chosen the type of MOSFET it becomes necessary to decided on the size of device. With MOSFETs this decision is made easier because, in its on-state, a MOSFET can be treated as a resistance and because its safe operating area (SOAR) is set by thermal considerations only (no second breakdown effects). The first stage of the selection process is to chose a device on the basis of the nominal current requirement. The next stage is to check that the inrush current, of the particular application and the drive method used, does not result in the MOSFET exceeding the transient thermal ratings. A fuller description of this technique is given in reference 1. Having selected a device that is capable of switching the load the designer can then use the quoted values for the on-state resistance ($R_{DS(ON)}$) to check that any on-state voltage drop requirements are being met. Tables 1 and 2 lists many of the different of lamps and resistive loads found in cars and suggests MOSFET types that can be used to control them.

The automotive environment

The environment that circuits and devices can be subjected to in automotive applications can prove to be extremely severe. Knowledge of the conditions that can exist is necessary to ensure that suitable devices and circuits are chosen. The two most stressful aspects of the environment are the temperature and voltage.

Table 4 Abnormal Supply Voltages

Voltage Level		Cause
12 V systems	24 V systems	
40 V - 50 V	60 V - 75 V	external spikes
30 V - 40 V	50 V - 60 V	clamped load dump
22 V - 30 V	22 V - 30 V	inductive load switch off
16 V - 22 V	32 V - 40 V	jump start
16 V - 22 V	32 V - 40 V	faulty regulator
8 V - 10.5 V	12 V - 20 V	faulty alternator
6 V - 8 V	9 V - 12 V	starting a petrol engine
0 V - 6 V	0 V - 6 V	starting a diesel engine

Temperature

The lowest temperature that is likely to be reached is -40˚C. This is related to the minimum outside temperature and may be lower under some special circumstances. The maximum temperature depends to a great extent upon the siting of circuits. The general ambient temperature in the engine compartment can be quite high and it is reasonable to assume that devices will see temperatures of 125˚C. Within the passenger area, conditions are somewhat more benign, but in areas where heat is generated and air flow is restricted, the temperature will be higher than might be

expected. For this reason it is necessary to assume that the circuits and devices will have to work in an ambient temperature of 85˚C.

Voltage

It is possible to split the voltage conditions that can occur into two groups - Normal and Abnormal. 'Normal' conditions are essentially those which can be present for very long periods of time. Under such conditions it is reasonable to expect devices and circuits to be completely operational and to suffer no ill effects. 'Abnormal' conditions are characterised by their temporary nature. They are not expected to persist for long periods and during them, some loss in device / circuit performance can be expected and, in some cases, is allowable.

Normal voltages

When considering the 'Normal' environment it is important to included both the typical and extreme cases. The crucial condition for most devices and circuits is when the engine is running. At this time the supply voltage can be anywhere between 10.5 and 16 V in '12 V' systems or between 20 and 32 V in '24 V' systems.

The other significant 'normal' operating mode is when engine not running. In this state the supply voltage could be very low but voltages below some level must be considered as a fault condition. However some circuits will have to operate with voltages as low as 6 V.

Abnormal voltages

It is possible to envisage a situation in which nearly any voltage could appear on the supply wires of a vehicle. How extreme the voltages get depends to a great extent upon the protection, both deliberate and incidental, built into the system. The actual voltage that appears at the terminals of a circuit is also influenced strongly by its location and the location of the protection. Analysis of the automotive environment has produced a list of expected abnormal conditions. The values of voltage that these conditions can be expected to produce are shown in Table 4.

References

1) Introduction to Power MOSFETs, Philips Components, chapter 1.

CHAPTER 6

Power Control With Thyristors and Triacs

6.1 Using Thyristors and Triacs

6.2 Thyristor and Triac Applications

Using Thyristors and Triacs

6.1.1 Introduction to thyristors and triacs

Brief summary of the thyristor family

The term thyristor is a generic name for a semiconductor switch having four or more layers and is, in essence, a p-n-p-n sandwich. Thyristors form a large family and it is helpful to consider the constituents which determine the type of any given thyristor. If an ohmic connection is made to the first p region and the last n region, and no other connection is made, the device is a diode thyristor. If an additional ohmic connection is made to the intermediate n region (n gate type) or the intermediate p region (p gate type), the device is a triode thyristor. If an ohmic connection is made to both intermediate regions, the device is a tetrode thyristor. All such devices have a forward characteristic of the general form shown in Fig.1.

There are three types of thyristor reverse characteristic: blocking (as in normal diodes), conducting (large reverse currents at low reverse voltages) and approximate mirror image of the forward characteristic (bidirectional thyristors). Reverse blocking devices usually have four layers or less whereas reverse conducting and mirror image devices usually have five layers.

The simplest thyristor structure, and the most common, is the reverse blocking triode thyristor (usually simply referred to as the 'thyristor' or SCR 'silicon controlled rectifier'). Its circuit symbol and basic structure is shown in Fig.2.

The most complex common thyristor structure is the bidirectional triode thyristor, or triac. The triac (shown in Fig.3) is able to pass current bidirectionally and is therefore an a.c. power control device. Its performance is that of a pair of thyristors in anti-parallel with a single gate terminal. The triac needs only one heatsink, but this must be large enough to remove the heat caused by bidirectional current flow. Triac gate triggering circuits must be designed with care to ensure that unwanted conduction, ie. loss of control, does not occur when triggering lasts too long.

Thyristors and triacs are both bipolar devices. They have very low on-state voltages but, because the minority charge carriers in the devices must be removed before they can block an applied voltage, the switching times are comparatively long. This limits thyristor switching circuits to low frequency applications. Triacs are used almost exclusively at mains supply frequencies.

The voltage blocking capabilities of thyristors and triacs are quite high: the highest voltage rating of Philips range of thyristors is 1200V, and 1000V for triacs. The Philips range of triacs covers currents ratings of $I_{T(RMS)}$=0.8A to 25A and up to 32A for thyristors. The devices are available as surface mount components, or as non-isolated or isolated discrete devices, depending on the device rating.

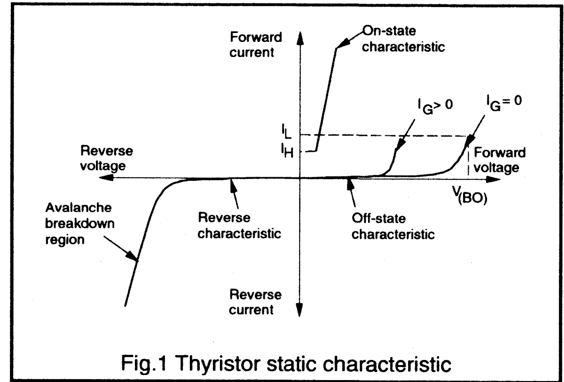


Fig.1 Thyristor static characteristic

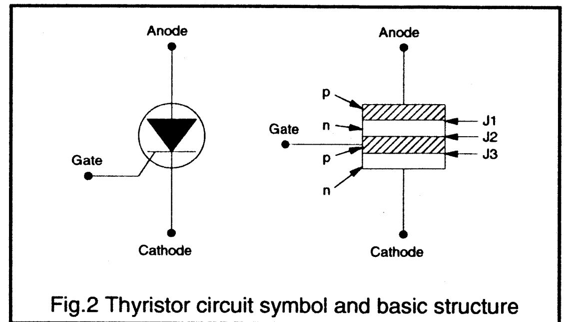


Fig.2 Thyristor circuit symbol and basic structure

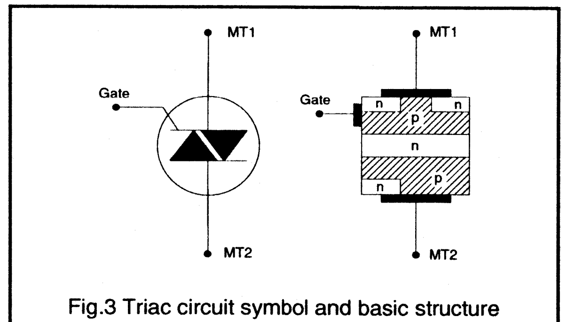


Fig.3 Triac circuit symbol and basic structure

Thyristor operation

The operation of the thyristor can be understood from Fig.2. When the thyristor cathode is more positive than the anode then junctions J1 and J3 are reverse biased and the device blocks. When the anode is more positive than the cathode, junctions J1 and J3 are forward biased. As J2 is reverse biased, then the device still blocks forward voltage. If the reverse voltage across J2 is made to reach its avalanche breakdown level then the device conducts like a single forward-biased junction.

The 'two transistor' model of Fig.4 can be used to consider the p-n-p-n structure of a thyristor as the interconnection of a npn transistor T_1 and a pnp transistor T_2. The collector of T_1 provides the base current for T_2. Base current for T_1 is provided by the external gate current in addition to the collector current from T_2. If the gain in the base-collector loop of T_1 and T_2 exceeds unity then the loop current can be maintained regeneratively. When this condition occurs then both T_1 and T_2 are driven into saturation and the thyristor is said to be 'latched'. The anode to cathode current is then only limited by the external circuit

There are several mechanisms by which a thyristor can be latched. The usual method is by a current applied to the gate. This gate current starts the regenerative action in the thyristor and causes the anode current to increase. The gains of transistors T_1 and T_2 are current dependent and increase as the current through T_1 and T_2 increases. With increasing anode current the loop gain increases sufficiently such that the gate current can be removed without T_1 and T_2 coming out of saturation.

Thus a thyristor can be switched on by a signal at the gate terminal but, because of the way that the current then latches, the thyristor cannot be turned off by the gate. The thyristor must be turned off by using the external circuit to break the regenerative current loop between transistors T_1 and T_2. Reverse biasing the device will initiate turn-off once the anode current drops below a minimum specified value, called the holding current value, I_H.

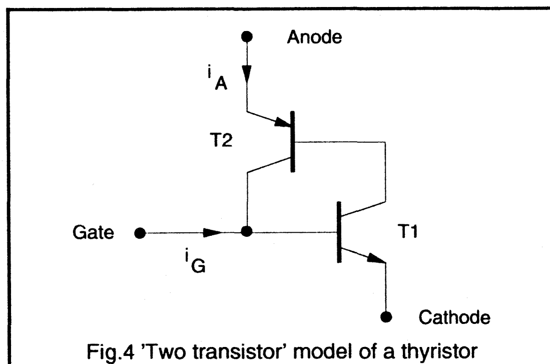


Fig.4 'Two transistor' model of a thyristor

Thyristor turn-on methods

Turn-on by exceeding the breakover voltage

When the breakover voltage, V_{BO}, across a thyristor is exceeded, the thyristor turns on. The breakover voltage of a thyristor will be greater than the rated maximum voltage of the device. At the breakover voltage the value of the thyristor anode current is called the latching current, I_L.

Breakover voltage triggering is not normally used as a triggering method, and most circuit designs attempt to avoid its occurrence. When a thyristor is triggered by exceeding V_{BO} the fall time of the forward voltage is quite low (about 1/20th of the time taken when the thyristor is gate-triggered). As a general rule, however, although a thyristor switches faster with V_{BO} turn-on than with gate turn-on, the permitted di/dt for breakover voltage turn-on is lower.

Turn-on by leakage current

As the junction temperature of a thyristor rises the leakage current also increases. Eventually, if the junction temperature is allowed to rise sufficiently, leakage current would become large enough to initiate latching of the regenerative loop of the thyristor and allow forward conduction. At a certain critical temperature (above $T_{j(max)}$) the thyristor will not support any blocking voltage at all.

Turn-on by dV/dt

Any p-n junction has capacitance - the larger the junction area the larger the capacitance. If a voltage ramp is applied across the anode-to-cathode of a p-n-p-n device, a current will flow in the device to charge the device capacitance according to the relation:

$$i_C = C.\frac{dv}{dt} \qquad (1)$$

If the charging current becomes large enough the density of moving current carriers in the device induces switch-on.

Turn-on by gate triggering

Gate triggering is the usual method of turning a thyristor on. Application of current to the thyristor gate initiates the latching mechanism discussed in the previous section. The characteristic of Fig.1 showed that the thyristor will switch to its on-state condition with forward bias voltages less than V_{BO} when the gate current is greater than zero. The gate current and voltage requirements which ensure triggering of a particular device are always quoted in the device data. As thyristor triggering characteristics are temperature dependant, the amplitude and duration of the gate pulse must be sufficient to ensure that the thyristor latches under all possible conditions.

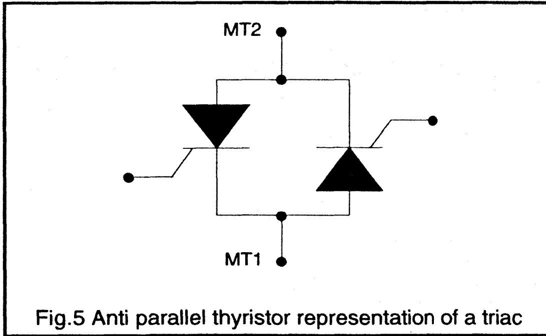


Fig.5 Anti parallel thyristor representation of a triac

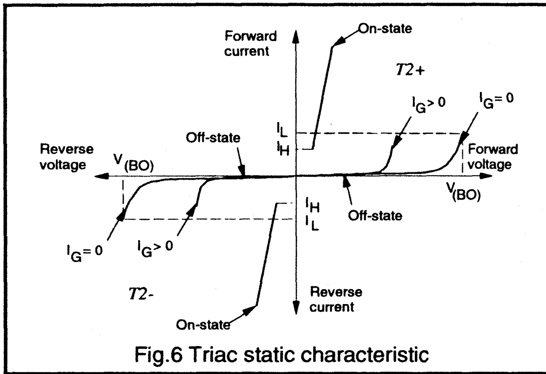


Fig.6 Triac static characteristic

During gate turn-on the rate of rise of thyristor anode current, dI_F/dt, is determined by the external circuit conditions. However the whole active area of the thyristor (or triac) cannot be turned on simultaneously: the area nearest to the gate turns on first, followed by the remainder of the device. At turn-on it is important that the rate of rise of current does not exceed the specified rating. If dI_F/dt is excessive then only a limited area of the device will have been turned on as the anode current increases. The resulting localised heating of the device will cause degradation and could lead to eventual device failure.

A suitably high gate current and large rate of rise of gate current (dI_G/dt) ensures that the thyristor turns on quickly (providing that the gate power ratings are not exceeded) thus increasing the thyristor turn-on di/dt capability. Once the thyristor has latched then the gate drive can be reduced or removed completely. Gate power dissipation can also be reduced by triggering the thyristor using a pulsed signal.

Triac operation

The triac can be considered as two thyristors connected in antiparallel as shown in Fig.5. The single gate terminal is common to both thyristors. The main terminals MT1 and MT2 are connected to both p and n regions of the device and the current path through the layers of the device depends upon the polarity of the applied voltage between the main terminals. The device polarity is usually described with reference to MT1, where the term MT2+ denotes that terminal MT2 is positive with respect to terminal MT1.

The on-state characteristic of the triac is similar to that of a thyristor and is shown in Fig.6. Table 1 and Fig.7 summarise the different gate triggering configurations for triacs.

Quadrant	Polarity of MT2 wrt MT1	Gate polarity
1 (1+)	MT2+	G+
2 (1-)	MT2+	G-
3 (3-)	MT2-	G-
4 (3+)	MT2-	G+

Table 1 Operating quadrants for triacs

Due to the physical layout of the semiconductor layers in a triac, the values of latching current (I_L), holding current (I_H) and gate trigger current (I_{GT}) vary slightly between the different operating quadrants. In general, for any triac, the holding current is slightly higher in the second (MT2+, G-) quadrant than the other quadrants, whilst the gate trigger current is slightly higher in fourth (MT2-, G+) quadrant.

For applications where the gate sensitivity is critical and where the device must trigger reliably and evenly for applied voltages in both directions it may be preferable to use a negative current triggering circuit. If the gate drive circuit is arranged so that only quadrants 2 and 3 are used (i.e. G- operation) then the triac is never used in the fourth quadrant where I_{GT} is highest.

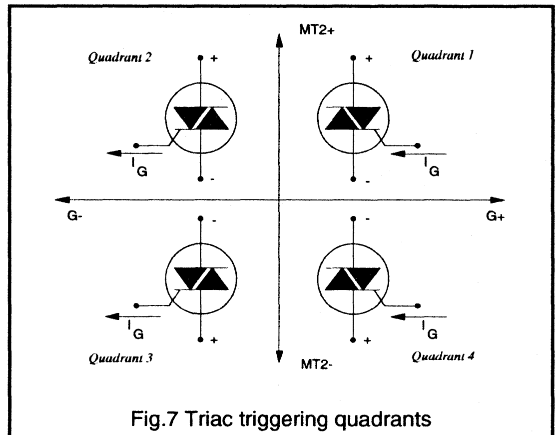


Fig.7 Triac triggering quadrants

For some applications it is advantageous to trigger triacs with a pulsating signal and thus reduce the gate power dissipation. To ensure bidirectional conduction, even with a very inductive load, the trigger pulses must continue until the end of each mains half-cycle. If single trigger pulses are used, one-way conduction (rectification) results when the trigger angle is smaller than the load phase angle.

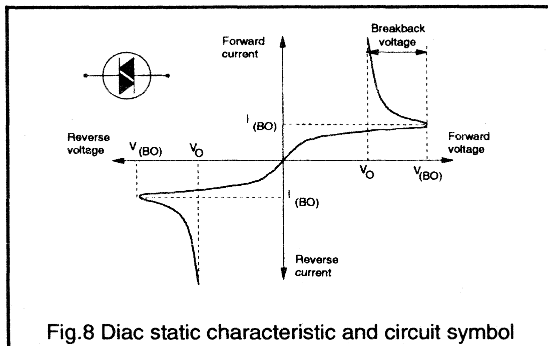


Fig.8 Diac static characteristic and circuit symbol

Philips produce ranges of triacs having the same current and voltage ratings but with different gate sensitivities. A device with a relatively insensitive gate will be more immune to false triggering due to noise on the gate signal and also will be more immune to commutating dv/dt turn-on. Sensitive gate triacs are used in applications where the device is driven from a controller IC or low power gate circuit.

The diac

It is also worthwhile to consider the operation and characteristics of the diac in the context of multilayer bipolar devices. The diac is more strictly a transistor than a thyristor, but has an important role in many thyristor and triac triggering circuits. It is manufactured by diffusing an n-type impurity into both sides of a p-type slice to give a two terminal device with symmetrical electrical characteristics. As shown in the characteristic of Fig.8, the diac blocks applied voltages in either direction until the breakover voltage, V_{BO} is reached. The diac voltage then breaks back to a lower output voltage V_O. Important diac parameters are breakover voltage, breakover current and breakback voltage as shown in the figure.

Gate requirements for triggering

To a first approximation, the gate-to-cathode junction of a thyristor or triac acts as a p-n diode. The forward characteristic is as shown in Fig.9. For a given thyristor type there will be a spread in forward characteristics of gate junctions and a spread with temperature.

The gate triggering characteristic is limited by the gate power dissipation. Fig.9 also shows the continuous power rating curve ($P_{G(AV)}$=0.5W) for a typical device and the peak gate power curve ($P_{GM(max)}$=5W). When designing a gate circuit to reliably trigger a triac or thyristor the gate signal must lie on a locus within the area of certain device triggering. Continuous steady operation would demand that the 0.5W curve be used to limit the load line of the gate drive circuit. For pulsed operation the triggering locus can be increased. If the 5W peak gate power curve is used, the duty cycle must not exceed

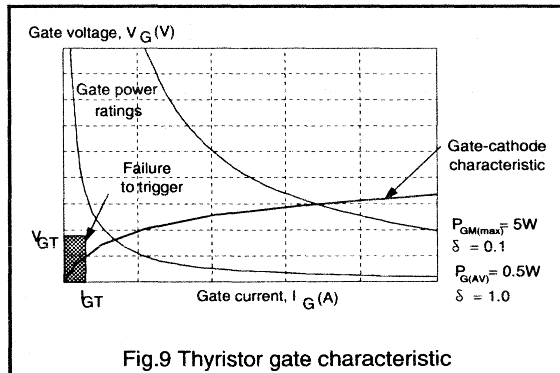


Fig.9 Thyristor gate characteristic

$$\delta_{max} = \frac{P_{G(AV)}}{P_{GM}} = \frac{0.5}{5} = 0.1 \qquad (2)$$

At the other end of the scale, the level below which triggering becomes uncertain is determined by the minimum number of carriers needed in the gate-cathode junction to bring the thyristor into conduction by regenerative action. The trigger circuit load line must not encroach into the failure to trigger region shown in Fig.9 if triggering is to be guaranteed. The minimum voltage and minimum current to trigger all devices (V_{GT} and I_{GT}) decreases with increasing temperature. Data sheets for Philips thyristors and triacs show the variation of V_{GT} and I_{GT} with temperature.

Thyristor commutation

A thyristor turns off by a mechanism known as 'natural turn off', that is, when the main anode-cathode current drops below the holding value. It is important to remember, however, that the thyristor will turn on again if the reapplied forward voltage occurs before a minimum time period has elapsed; this is because the charge carriers in the thyristor at the time of turn-off take a finite time to recombine. Thyristor turn-off is achieved by two main methods - self commutation or external commutation.

Self Commutation

In self-commutation circuits the thyristor will automatically turn off at a predetermined time after triggering. The thyristor conduction period is determined by a property of the commutation circuit, such as the resonant cycle of an LC-circuit or the Volt-Second capability of a saturable inductor. The energy needed for commutation is delivered by a capacitor included in the commutation circuit.

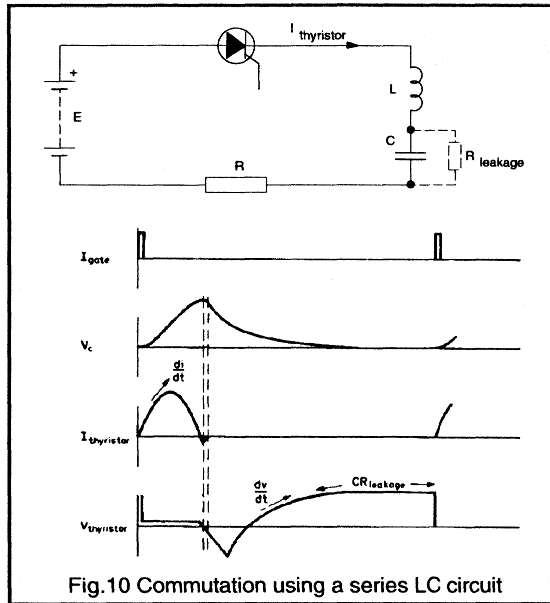


Fig.10 Commutation using a series LC circuit

LC circuit in series with the thyristor

When the thyristor is triggered, the resulting main current excites the resonant circuit. After half a resonant cycle, the LC circuit starts to reverse the anode current and turns the thyristor off. The thyristor conduction interval is half a resonant cycle. It is essential for proper commutation, that the resonant circuit be less than critically damped. Fig.10 shows the circuit diagram and the relevant waveforms for this arrangement.

LC Circuit in parallel with the thyristor

Initially the capacitor charges to the supply voltage. When the thyristor is triggered the load current flows but at the same time the capacitor discharges through the thyristor in the forward direction. When the capacitor has discharged (i.e. after one resonant half-cycle of the LC circuit), it begins to charge in the opposite direction and, when this charging current is greater than the thyristor forward current, the thyristor turns off. The circuit diagram and commutation waveforms are shown in Fig.11.

External commutation

If the supply is an alternating voltage, the thyristor can conduct only during the positive half cycle. The thyristor naturally switches off at the end of each positive half cycle. The circuit and device waveforms for this method of commutation is shown in Fig.12. It is important to ensure that the duration of a half cycle is greater than the thyristor turn off time.

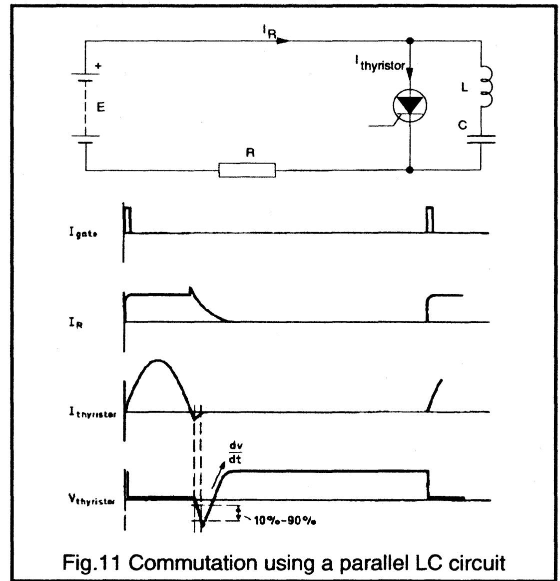


Fig.11 Commutation using a parallel LC circuit

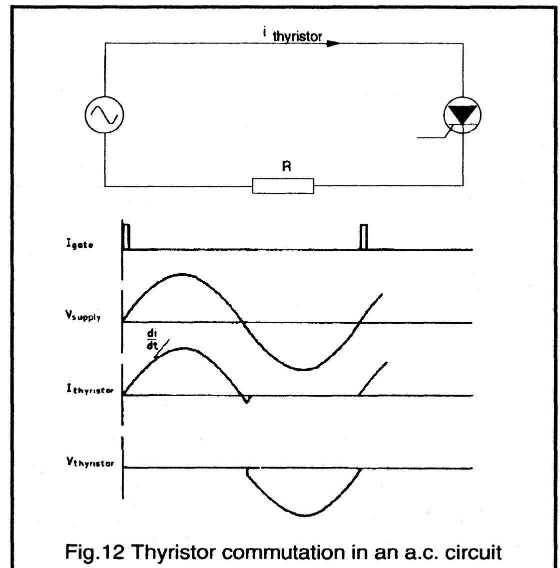


Fig.12 Thyristor commutation in an a.c. circuit

Reverse recovery

In typical thyristors the reverse recovery time is of the order of a few micro-seconds. This time increases with increase of forward current and also increases as the forward current decay rate, dI_T/dt, decreases. Reverse recovery time is the period during which reverse recovery current flows (t_1 to t_3 in Fig.13) and it is the period between the point at which

forward current ceases and the earliest point at which the reverse recovery current has dropped to 10% of its peak value.

Reverse recovery current can cause high values of turn-on current in full-wave rectifier circuits (where thyristors are used as rectifying elements) and in certain inverter circuits. It should also be remembered that, if thyristors are connected in series, the reverse voltage distribution can be seriously affected by mismatch of reverse recovery times.

Turn-off time

Turn-off time is the interval between the instant when thyristor current reverses and the point at which the thyristor can block reapplied forward voltage (t_1 to t_4 in Fig.13). If forward voltage is applied to a thyristor too soon after the main current has ceased to flow, the thyristor will turn on. The circuit commutated turn-off time increases with:

- -junction temperature
- -forward current amplitude
- -rate of fall of forward current
- -rate of rise of forward blocking voltage
- -forward blocking voltage.

Thus the turn-off time is specified for defined operating conditions. Circuit turn-off time is the turn-off time that the circuit presents to the thyristor; it must, of course, be greater than the thyristor turn-off time.

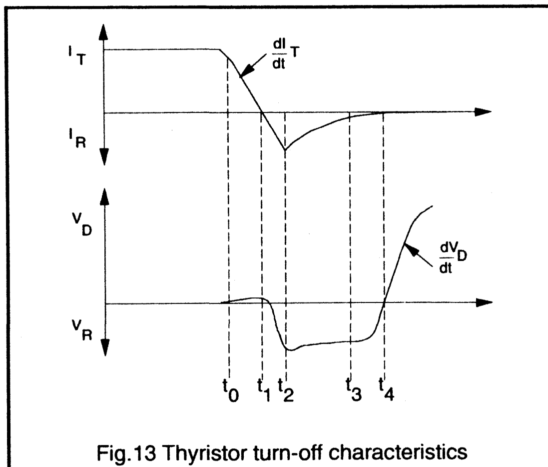


Fig.13 Thyristor turn-off characteristics

Triac commutation

Unlike the thyristor, the triac can conduct irrespective of the polarity of the applied voltage. Thus the triac does not experience a circuit-imposed turn-off time which allows each anti-parallel thyristor to fully recover from its conducting state as it is reverse biased. As the voltage across the triac passes through zero and starts to increase then the alternate thyristor or the triac can fail to block the applied voltage and immediately conduct in the opposite direction. Triac-controlled circuits therefore require careful design in order to ensure that the triac does not fail to commutate (switch off) at the end of each half-cycle as expected.

It is important to consider the commutation performance of devices in circuits where either dI/dt or dV/dt can be large. In resistive load applications (e.g. lamp loads) current surges at turn-on or during temporary over-current conditions may introduce abnormally high rates of change of current which may cause the triac to fail to commutate. In inductive circuits, such as motor control applications or circuits where a dc load is controlled by a triac via a bridge rectifier, it is usually necessary to protect the triac against unwanted commutation due to $dv_{(com)}/dt$.

The commutating $dv_{(com)}/dt$ limit for a triac is less than the static dv/dt limit because at commutation the recently conducting portion of the triac which is being switched off has introduced stored charge to the triac. The amount of stored charge depends upon the reverse recovery characteristics of the triac and is significantly affected by the rate of fall of anode current prior to commutation ($dI_{(com)}/dt$) and junction temperature. Following high rates of change of current the capacity of the triac to withstand high reapplied rates of change of voltage is reduced. Data sheet specifications for triacs give characteristics showing the maximum allowable rate of rise of commutating voltage against device temperature and rate of fall of anode current which will not cause a device to trigger.

Consider the situation when a triac is conducting in one direction and the applied ac voltage changes polarity. For the case of an inductive load the current in the triac does not fall to its holding current level until some time later. This is shown in Fig.14. At the time that the triac current has reached the holding current the mains voltage has risen to some value and so the triac must immediately block that voltage. The rate of rise of blocking voltage following commutation ($dv_{(com)}/dt$) can be quite high.

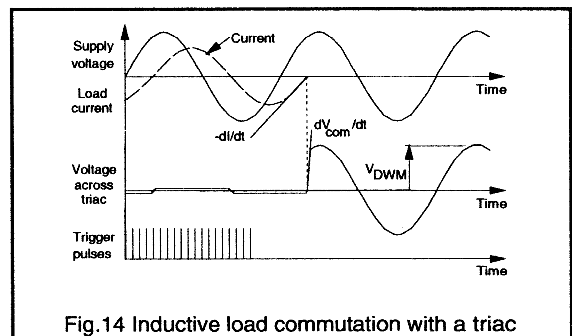


Fig.14 Inductive load commutation with a triac

The usual method is to place a dv/dt limiting R-C snubber in parallel with the triac. Additionally, because commutating dv/dt turn-on is dependent upon the rate of fall of triac current, then, in circuits with large rates of change of anode current, the ability of a triac to withstand high rates of rise of reapplied voltage is improved by limiting the di/dt using a series inductor. This topic is discussed more fully in the section entitled 'Triac control of DC inductive loads'

Conclusions

This article has presented the basic parameters and characteristics of triacs and thyristors and shown how the structure of the devices determines their operation. Important turn-on and turn-off conditions and limitations of the devices have been presented in order to demonstrate the capabilities of the devices and show the designer those areas which require careful consideration. The device characteristics which determine gate triggering requirements of thyristors and triacs have been presented.

Subsequent articles in this chapter will deal with the use, operation and limitations of thyristors and triacs in practical applications, and will present some detailed design and operational considerations for thyristors and triacs in phase control and integral cycle control applications.

6.1.2 Using thyristors and triacs

This chapter is concerned with the uses, operation and protection of thyristors and triacs. Two types of circuit cover the vast majority of applications for thyristors and triacs: static switching circuits and phase control circuits. The characteristics and uses of these two types of circuit will be discussed. Various gate drive circuits and protection circuits for thyristor and triacs are also presented. The use of these circuits will enable designers to operate the devices reliably and within their specified limits.

Thyristor and triac control techniques

There are two main techniques of controlling thyristors and triacs - on-off triggering (or static switching) and phase control. In on-off triggering, the power switch is allowed to conduct for a certain number of half-cycles and then it is kept off for a number of half-cycles. Thus, by varying the ratio of "on-time" to "off-time", the average power supplied to the load can be controlled. The switching device either completely activates or deactivates the load circuit. In phase control circuits, the thyristor or triac is triggered into conduction at some point after the start of each half-cycle. Control is achieved on a cycle-by-cycle basis by variation of the point in the cycle at which the thyristor is triggered.

Static switching applications

Thyristors and triacs are the ideal power switching devices for many high power circuits, such as heaters, enabling the load to be controlled by a low power signal, in place of a relay or other electro-mechanical switch.

In a high power circuit where the power switch may connect or disconnect the load at any point of the mains cycle then large amounts of RFI (radio frequency interference) are likely to occur at the instants of switching. The large variations in load may also cause disruptions to the supply voltage. The RFI and voltage variation produced by high power switching in a.c. mains circuits is unacceptable in many environments and is controlled by statutory limits. The limits depend upon the type of environment (industrial or domestic) and the rating of the load being switched.

RFI interference occurs at any time when there is a step change in current caused by the closing of a switch (mechanical or semiconductor). The energy levels of this interference can be quite high in circuits such as heating elements. However, if the switch is closed at the moment the supply voltage passes through zero there is no step rise in current and thus no radio frequency interference. Similarly, at turn-off, a large amount of high frequency interference can be caused by di/dt imposed voltage transients in inductive circuits.

Circuit-generated RFI can be almost completely eliminated by ensuring that the turn-on switching instants correspond to the zero-crossing points of the a.c. mains supply. This technique is known as synchronous (or zero voltage switching) control as opposed to the technique of allowing the switching points to occur at any time during the a.c. cycle, which is referred to as asynchronous control.

In a.c. circuits using thyristors and triacs the devices naturally switch off when the current falls below the device holding current. Thus turn-off RFI does not occur.

Asynchronous control

In asynchronous control the thyristor or triac may be triggered at a point in the mains voltage other than the zero voltage crossover point. Asynchronous control circuits are usually relatively cheap but liable to produce RFI.

Synchronous control

In synchronous control systems the switching instants are synchronised with zero crossings of the supply voltage. They also have the advantage that, as the thyristors conduct over complete half cycles the power factor is very good. This method of power control is mostly used to control temperature. The repetition period, T, is adjusted to suit the controlled process (within statutory limits). Temperature ripple is eliminated when the repetition period is made much smaller than the thermal time constant of the system.

Fig.1 shows the principle of time-proportional control. RFI and turn-on di/dt are reduced, and the best power factor (sinusoidal load current) is obtained by triggering synchronously. The average power delivered to a resistive load, R_L, is proportional to t_{on}/T (i.e. linear control) and is given by equation 1.

$$P_{out} = \frac{V_{(RMS)}^2}{R_L} \cdot \frac{t_{on}}{T} \qquad (1)$$

where: T is the controller repetition period
t_{on} is controller 'on' time
$V_{(RMS)}$ is the rms a.c. input voltage.

Elsewhere in this handbook the operation of a controller i.c. (the TDA1023) is described. This device is specifically designed to implement time-proportional control of heaters using Philips triacs.

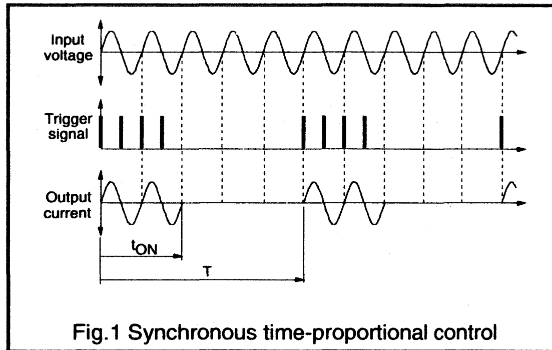


Fig.1 Synchronous time-proportional control

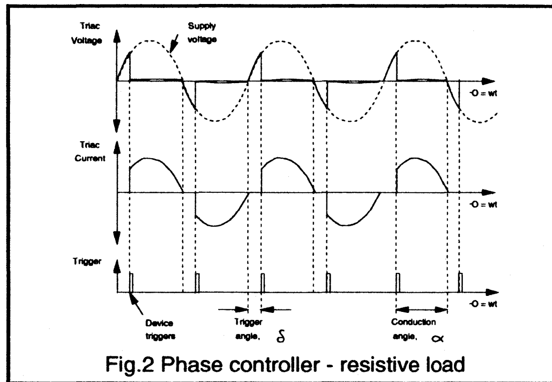


Fig.2 Phase controller - resistive load

Phase control

Phase control circuits are used for low power applications such as lamp control or universal motor speed control, where RFI emissions are not excessively large. The power delivered to the load is controlled by the timing of the thyristor (or triac) turn-on point.

The two most common phase controller configurations are 'half wave control', where the controlling device is a single thyristor and 'full wave control', where the controlling device is a triac or a pair of anti-parallel thyristors. These two control strategies are considered in more detail below:

Resistive loads

The operation of a phase controller with a resistive load is the simplest situation to analyse. Waveforms for a full wave controlled resistive load are shown in Fig.2. The triac is triggered at angle δ, and applies the supply voltage to the load. The triac then conducts for the remainder of the positive half-cycle, turning off when the anode current drops below the holding current, as the voltage becomes zero at θ=180˚. The triac is then re-triggered at angle (180+δ)˚, and conducts for the remainder of the negative half-cycle, turning off when its anode voltage becomes zero at 360˚.

The sequence is repeated giving current pulses of alternating polarity which are fed to the load. The duration of each pulse is the conduction angle α, that is (180-δ)˚, The output power is therefore controlled by variation of the trigger angle δ.

For all values of α other than α=180˚ the load current is non-sinusoidal. Thus, because of the generation of harmonics, the power factor presented to the a.c. supply will be less than unity except when δ=0.

For a sinusoidal current the rectified mean current, $I_{T(AV)}$, and the rms current, $I_{T(RMS)}$, are related to the peak current, $I_{T(MAX)}$, by equation 2.

$$I_{T(AV)} = \frac{2.I_{T(MAX)}}{\pi} = 0.637\, I_{T(MAX)}$$

$$I_{T(RMS)} = \frac{I_{T(MAX)}}{\sqrt{2}} = 0.707\, I_{T(MAX)} \qquad (2)$$

where

$$I_{T(MAX)} = \frac{V_{T(MAX)}}{R_L} = \frac{\sqrt{2}\,V_{(RMS)}}{R_L} \qquad (3)$$

From equation 2 the 'crest factor', *c*, (also known as the 'peak factor') of the current waveform is defined as:

$$\text{Crest factor,} \quad c = \frac{I_{T(MAX)}}{I_{T(RMS)}} \qquad (4)$$

The current 'form factor,' *a*, is defined by:

$$\text{Form factor,} \quad a = \frac{I_{T(RMS)}}{I_{T(AV)}} \qquad (5)$$

Thus, for sinusoidal currents:

$$a = \frac{I_{T(RMS)}}{I_{T(AV)}} = 1.111; \qquad c = \frac{I_{T(MAX)}}{I_{T(RMS)}} = 1.414 \qquad (6)$$

For the non-sinusoidal waveforms which occur in a phase controlled circuit the device currents are modified due to the delay which occurs before the power device is triggered. The crest factor of equation 4 and the form factor of equation 5 can be used to describe variation of the current waveshape from the sinusoidal case.

Half wave controller

Fig.3a) shows the simplest type of thyristor half-wave phase controller for a resistive load. The load current waveform is given in Fig.3b). The variation of average load current, $I_{T(AV)}$, rms load current, $I_{T(RMS)}$ and load power over the full period of the a.c mains, with trigger angle are given in equation 7.

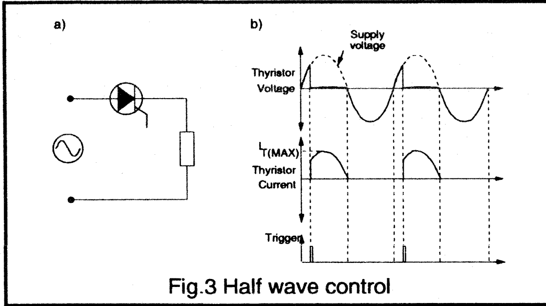


Fig.3 Half wave control

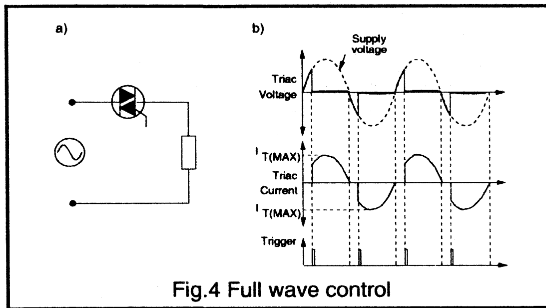


Fig.4 Full wave control

$$I_{T(AV)} = I_{T(AV)\max}\cdot\frac{(1-\cos\alpha)}{2} \qquad I_{T(AV)\max} = \frac{I_{T(\mathrm{MAX})}}{\pi}$$

$$I_{T(RMS)} = I_{T(RMS)\max}\cdot\left(\frac{\alpha-\frac{1}{2}\sin 2\alpha}{\pi}\right)^{\frac{1}{2}} \qquad I_{T(RMS)\max} = \frac{I_{T(\mathrm{MAX})}}{2}$$

$$P_{(out)} = P_{(out)\max}\cdot\left(\frac{\alpha-\frac{1}{2}\sin 2\alpha}{\pi}\right) \qquad P_{(out)\max} = \frac{I^2_{T(\mathrm{MAX})}R_L}{4} \qquad (7)$$

N.B. When using equation 7 all value of α must be in radians. For each case the maximum value occurs when α=180˚ ($\alpha=\pi$ radians).

At α=180˚ the crest factor and form factor for a half wave controller are given by:

$$a = \frac{I_{T(RMS)}}{I_{T(AV)}} = 1.571; \qquad c = \frac{I_{T(\mathrm{MAX})}}{I_{T(RMS)}} = 2.0 \qquad (8)$$

Full wave controller

Fig.4 shows the circuit and load current waveforms for a full-wave controller using two antiparallel thyristors, or a triac, as the controlling device. The variation of rectified mean current, $I_{T(AV)}$, rms current, $I_{T(RMS)}$, and load power with trigger angle are given by equation 9.

$$I_{T(AV)} = I_{T(AV)\max}\cdot\frac{(1-\cos\alpha)}{2} \qquad I_{T(AV)\max} = \frac{2I_{T(\mathrm{MAX})}}{\pi}$$

$$I_{T(RMS)} = I_{T(RMS)\max}\cdot\left(\frac{\alpha-\frac{1}{2}\sin 2\alpha}{\pi}\right)^{\frac{1}{2}} \qquad I_{T(RMS)\max} = \frac{I_{T(\mathrm{MAX})}}{\sqrt{2}}$$

$$P_{(out)} = P_{(out)\max}\cdot\left(\frac{\alpha-\frac{1}{2}\sin 2\alpha}{\pi}\right) \qquad P_{(out)\max} = \frac{I^2_{T(\mathrm{MAX})}R_L}{2} \qquad (9)$$

N.B. When using equation 9 all value of α must be in radians. For each case the maximum value occurs when α=180˚ ($\alpha=\pi$ radians).

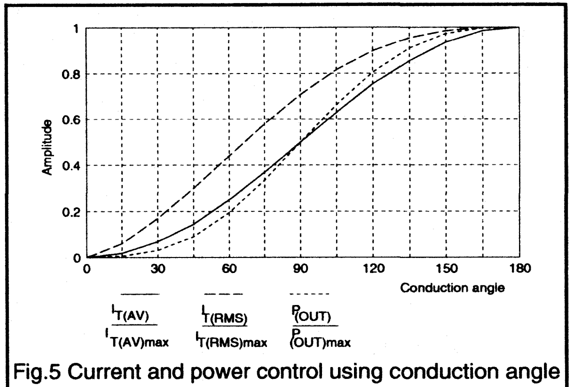


Fig.5 Current and power control using conduction angle

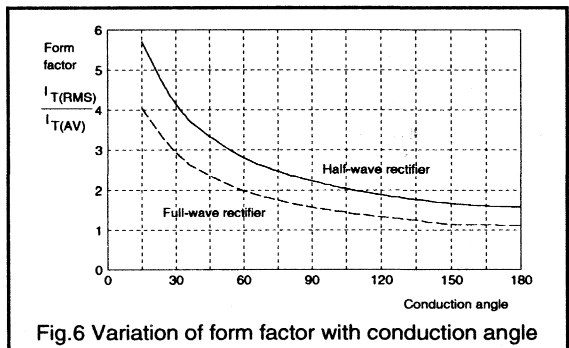


Fig.6 Variation of form factor with conduction angle

The variation of normalised average current, $I_{T(AV)}/I_{T(AV)max}$, rms current $I_{T(RMS)}/I_{T(RMS)max}$, and power, $P_{(out)}/P_{(out)max}$, for equations 7 and 9 are plotted in Fig.5.

Fig.6 shows the variation of current form factor with conduction angle for the half wave controller and the full wave controller of Figs 3 and 4.

Inductive loads

The circuit waveforms for a phase controller with an inductive load or an active load (for example, a motor) are more complex than those for a purely resistive load. The circuit waveforms depend on the load power factor (which may be variable) as well as the triggering angle.

For a bidirectional controller (i.e triac or pair of anti-parallel thyristors) maximum output, that is, sinusoidal load current, occurs when the trigger angle equals the phase angle. When the trigger angle, δ, is greater than the load phase angle, φ, then the load current will become discontinuous and the triac (or thyristor) will block some portion of the input voltage until it is retriggered.

If the trigger angle is less than the phase angle then the load current in one direction will not have fallen back to zero at the time that the device is retriggered in the opposite direction. This is shown in Fig.7. The triac fails to be triggered as the gate pulse has finished and so the triac then acts as a rectifier. In Fig.7 the triac is only triggered by the gate pulses when the applied positive voltage is positive (1+ quadrant). However the gate pulses which occur one half period later have no effect because the triac is still conducting in the opposite direction. Thus unidirectional current flows in the main circuit, eventually saturating the load inductance.

This problem can be avoided by using a trigger pulse train as shown in Fig.8. The triac triggers on the first gate pulse after the load current has reached the latching current I_L in the 3+ quadrant. The trigger pulse train must cease before the mains voltage passes through zero otherwise the triac will continue to conduct in the reverse direction.

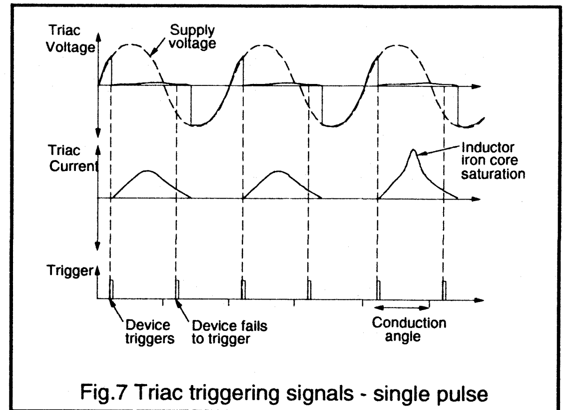


Fig.7 Triac triggering signals - single pulse

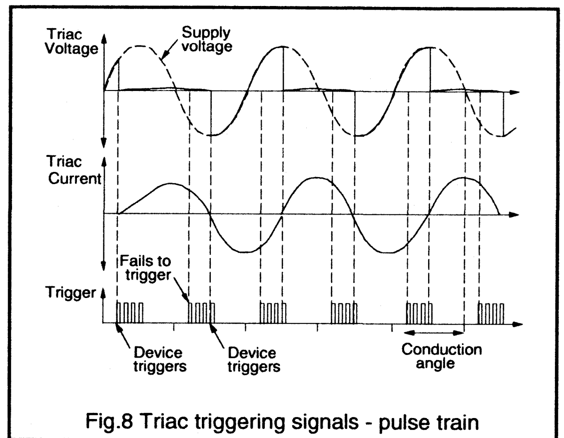


Fig.8 Triac triggering signals - pulse train

Gate circuits for thyristors and triacs

As discussed in the introductory article of this chapter, a thyristor or triac can be triggered into conduction when a voltage of the appropriate polarity is applied across the main terminals and a suitable current is applied to the gate. This can be achieved using a delay network of the type shown in Fig.9a) Greater triggering stability and noise immunity can be achieved if a diac is used (see Fig.9b), This gives a trigger circuit which is suitable for both thyristors and triacs.

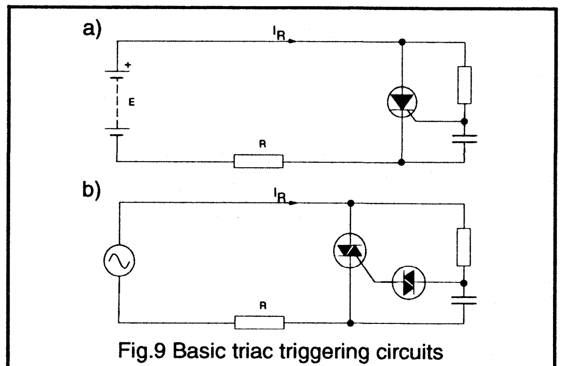


Fig.9 Basic triac triggering circuits

Fig.10 shows several alternative gate drive circuits suitable for typical triac and thyristor applications. In each circuit the gate-cathode resistor protects the device from false triggering due to noise - this is especially important for sensitive gate devices. In addition opto-isolated thyristor and triac drivers are available which are compatible with the Philips range of devices.

In some applications it may be necessary to cascade a sensitive gate device with a larger power device to give a sensitive gate circuit with a high power handling capability. A typical solution which involves triggering the smaller device (BT169) from a logic-level controller to turn on the larger device (BT151) is shown in Fig.11.

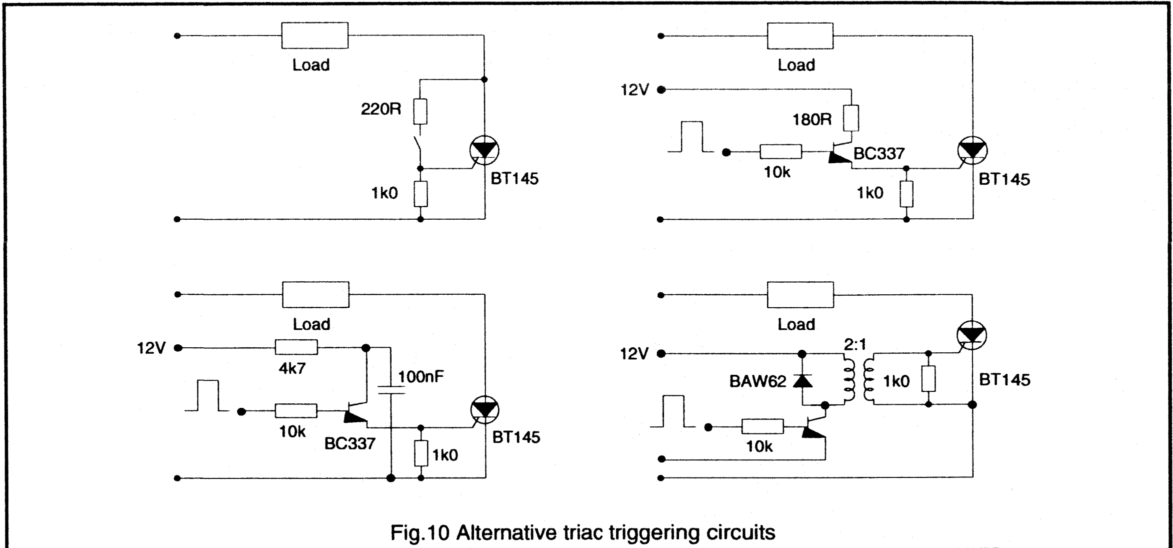


Fig.10 Alternative triac triggering circuits

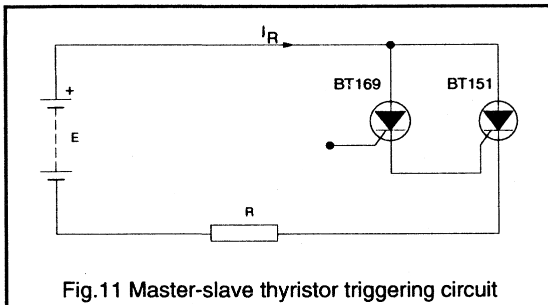


Fig.11 Master-slave thyristor triggering circuit

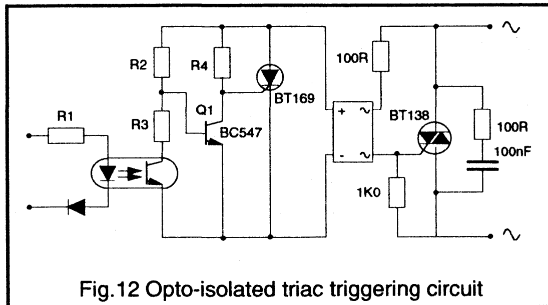


Fig.12 Opto-isolated triac triggering circuit

Fig.12 shows an isolated triac triggering circuit suitable for zero voltage switching applications. This type of circuit is also known as a solid state relay (SSR). The function of the Q1/R2/R3 stage is that the BC547 is on at all instants in time when the applied voltage waveform is high and thus holds the BT169 off. If the BT169 is off then no gate signal is applied to the triac and the load is switched off.

If the input signal is swiched high then the photo-transistor turns on. If this occurs when the mains voltage is high then Q1 remains on. When the line voltage passes through its next zero crossing in either direction the the photo transistor ensures that Q1 stays off long enough for the BT169 to trigger. This then turns the triac on. Once the thyristor turns on the drive circuit is deprived of its power, due to the lower voltage drop of the BT169. The triac is retrigered every half cycle.

Voltage transient protection

There are three major sources of the type of transients which may affect thyristor and triac circuits:

-the mains supply (e.g. lightning)
-other mains and load switches (opening and closing)
-the rectifying and load circuit (commutation)

In order to ensure reliable circuit operation these transients must be suppressed by additional components, removed at source or allowed for in component ratings.

Three types of circuit are commonly employed to suppress voltage transients - a snubber network across the device, a choke between the power device and external circuit or an overvoltage protection such as a varistor.

Series line chokes

A series choke may be used to limit peak fault currents to assist in the fuse protection of thyristors and triacs. If the choke is used in conjunction with fuse protection, it must retain its inductance to very large values of current, and so for this reason it is usually an air-cored component.

Alternatively, if the choke is only required to reduce the dv/dt across non-conducting devices then the inductance needs only to be maintained upto quite low currents. Ferrite-cored chokes may be adequate provided that the windings are capable of carrying the full-load current. Usually only a few microhenries of inductance are required to limit the circuit di/dt to an acceptable level. This protects the devices from turning on to quickly and avoids potential device degradation.

For instance, a 220V a.c. supply with 20µH source inductance gives a maximum di/dt of (220√2)/20=16A/µs. Chokes used to soften commutation should preferably be saturable so as to maintain regulation and avoid deterioration of the power factor. As their impedance reduces at low current, they have very little effect on the inrush current.

The addition of di/dt limiting chokes is especially important in triac circuits where the load is controlled via a bridge rectifier. At the voltage zero-crossing points the conduction transfers between diodes in the bridge network, and the rate of fall of triac current is limited only by the stray inductance in the a.c. circuit. The large value of commutating di/dt may cause the triac to retrigger due to commutating $dv_{(com)}/dt$. A small choke in the a.c circuit will limit the $di_{(com)}/dt$ to acceptable level. An alternative topology which avoids triac commutation problems is to control the load on the d.c. side.

Snubber networks

Snubber networks ensure that the device is not exposed to excessive rates of change of voltage during transient conditions. This is particularly important when considering the commutation behaviour of triacs, which has been discussed elsewhere.

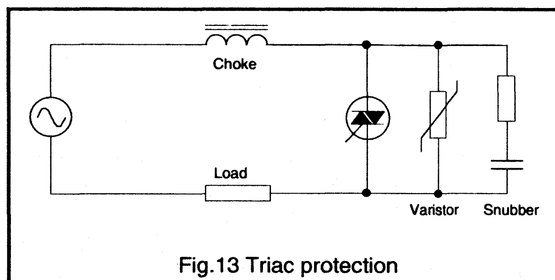


Fig.13 Triac protection

The following equations can be used to calculate the values of the snubber components required to keep the reapplied dv/dt for a triac within the $dv_{(com)}/dt$ rating for that device. The parameters which affect the choice of snubber components are the value of load inductance, frequency of the a.c. supply and rms load current. The value of the snubber resistor needs to be large enough to damp the circuit and avoid voltage overshoots. The snubber capacitor should be rated for the full a.c. voltage of the system; the snubber resistor needs to be rated at 0.5W.

For circuits where the load power factor, cosφ, ≥ 0.7 the snubber values are given approximately by:

$$C \geq 25L\left(\frac{fI_{T(RMS)}}{dV_{(com)}/dt}\right)^2$$

$$R = \sqrt{\frac{3L}{C}} \qquad (9)$$

where: L is the load inductance
f is the supply frequency
$I_{T(RMS)}$ is the rms device current
$dv_{(com)}/dt$ is the device commutating dv/dt rating.

The presence of a snubber across the device can improve the turn-on performance of the triac by using the snubber capacitor discharge current in addition to the load current to ensure that the triac latches at turn-on. The value of the snubber resistor must be large enough to limit the peak capacitor discharge current through the triac to within the turn-on di/dt limit of the device.

Varistor

The use of a metal oxide varistor (MOV), as shown in Fig.13 protects the device from transient overvoltages which may occur due to mains disturbances.

Overcurrent protection

Like all other semiconductor devices, triacs have an infinite life if they are used within their ratings. However, they rapidly overheat when passing excessive current because the thermal capacitance of their junction is small. Overcurrent protective devices (circuit breakers, fuses) must, therefore, be fast-acting.

Inrush condition

Motors, incandescent lamp or transformer loads give rise to an inrush condition. Lamp and motor inrush currents are avoided by starting the control at a large trigger angle. Transformer inrush currents are avoided by adjusting the initial trigger angle to a value roughly equal to the load phase angle. No damage occurs when the amount of inrush current is below the inrush current rating curve quoted in the device data sheet (see the chapter 'Understanding thyristor and triac data').

Short-circuit condition

Fuses for protecting triacs should be fast acting, and the amount of fuse I^2t to clear the circuit must be less than the I^2t rating of the triac. Because the fuses open the circuit rapidly, they have a current limiting action in the event of a

short-circuit. High voltage fuses exhibit low clearing I^2t but the fuse arc voltage may be dangerous unless triacs with a sufficiently high voltage rating are used.

Conclusions

This paper has outlined the most common uses and applications of thyristor and triac circuits. The type of circuit used depends upon the degree of control required and the nature of the load. Several types of gate circuit and device protection circuit have been presented. The amount of device protection required will depend upon the conditions imposed on the device by the application circuit. The protection circuits presented here will be suitable for the majority of applications giving a cheap, efficient overall design which uses the device to its full capability with complete protection and confidence.

6.1.3 The peak current handling capability of thyristors

The ability of a thyristor to withstand peak currents many times the size of its average rating is well known. However there is little information about the factors affecting the peak current capability. This section will investigate the effect of pulse duration on the peak current capability of thyritors.

Data sheets for thyristors always quote a figure for the maximum surge current that the device can survive. This figure assumes a half sine pulse with a width of either 8.3 ms or 10 ms, which are the conditions applicable for 50/60 Hz mains operation. This limit is not absolute - narrow pulses with much higher peaks can be handled without damage but little information is available to enable the designer to determine how high this current is. This section will discuss some of the factors affecting a thyristors peak current capability and review the existing prediction methods. It will go onto present the results of an evaluation of the peak current handling capabilities for pulses as narrow as 10 µs for the BT151, BT152 and BT145 thyristors. It will also propose a method for estimating a thyristors peak current capability for a half sine pulse with a duration between 10 µs and 10 ms from it quoted surge rating.

Energy Handling

In addition to the maximum surge current, data sheets often quote a figure called "I^2t for fusing". This number is used to select appopriate fuses for device protection. I^2t represents the energy that can be passed by the device without damage. In fact it is not the passage of the energy which causes damage, but the heating of the crystal by the energy absorbed by the device which causes damage.

If the period over which the energy is delivered is long, the absorbed energy has time to spread to all areas of the device capable of storing it - like the edges of the crystal, the plastic encapsulation, the mounting tab and for very long times the heatsink - therefore the temperature rise in the crystal is moderated. If, however, the delivery period is short - say a single half sine pulse of current with a duration of <10 ms - the areas to which the energy can spread, during the actual duration of the pulse, are limited. This means that the crystal keeps all the energy giving a much bigger temperature rise. For very short pulses (<0.1 ms) and large crystal the problem is even worse because not all of the active area of a thyristor crystal is turned on simultaneously - conduction tends to spread out from the gate area - so the current pulse passes through only part of the crystal resulting in a higher level of dissipation and an even more restricted area for absorbing it.

Expected Results

I^2t is normally quoted at 10 ms, assuming that the surge is a half sine pulse, and is derived from the surge current from:

$$I^2t = \left(\frac{I_{TSM}}{\sqrt{2}}\right)^2 \cdot 0.01$$

This calculates the RMS current by dividing I_{TSM} by $\sqrt{2}$

Under the simplest of analyses I^2t would be assumed to be constant so a device's peak current capability could be calculated from:

$$I_{pk} = I_{TSM} \cdot \left(\frac{0.01}{t_p}\right)^{\frac{1}{2}}$$

where I_{pk} is the peak of a half sine current pulse with a duration of t_p. However experience and experiments have shown that such an approach is inaccurate. To overcome this other 'rules' have been derived.

One of these 'rules' suggests that it is not I^2t which is constant but I^3t or I^4t. Another suggestion was that the 'constancy' continuously changes from I^2t to I^4t as the pulses became shorter. However all these rules are expressed in the general equation:

$$I_{pk} = I_{TSM} \cdot \left(\frac{0.01}{t_p}\right)^{\frac{1}{N}}$$

where is N is either constant or a function of the pulse width, for example:

$$N = \log\left(\frac{1}{t_p}\right)$$

The graph shown in Fig.1 shows what several of these 'rules' predict would happen to the peak current capability if they were true. Unfortunately little or no real information currently exists to indicate the validity of these rules. Tests have been performed on three groups of devices - BT151, BT152 and BT145 - to gather the data which would, hopefully, decide which was correct.

Test Circuit

The technique chosen to measure the peak current capability of the devices was the stepped surge method. In this the device is subjected to a series of current pulses of increasing magnitude until it receives a surge which causes measurable degradation.

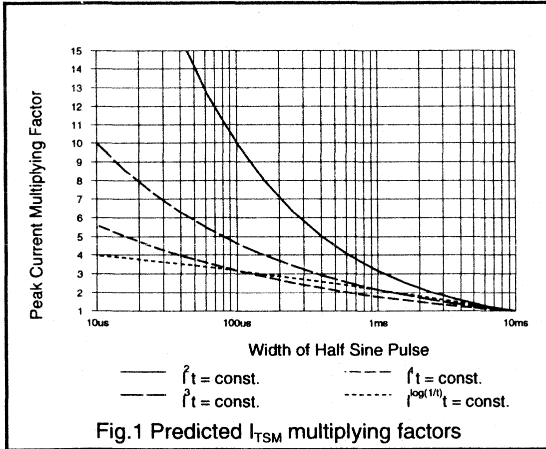


Fig.1 Predicted I_{TSM} multiplying factors

Circuit Description

The circuits used to perform the required measurements were of the form shown in Fig.2. They produce half sine pulses of current from the resonant discharge of C via L. Triggering of the device under test (DUT) itself, is used to initiate the discharge. The gate signal used for all the tests was a 100 mA / 1 µs pulse fed from a pulse generator in single-shot mode.

The magnitude of the current pulse is adjusted by changing the voltage to which C is initially charged by varying the output of the PSU. The pulse is monitored by viewing the voltage across R3 on an digital storage oscilloscope. R1 and D protect the power supply. R1 limits the current from the supply when DUT fails and during the recharging of C. D attempts to prevent any high voltage spikes being fed back into the PSU.

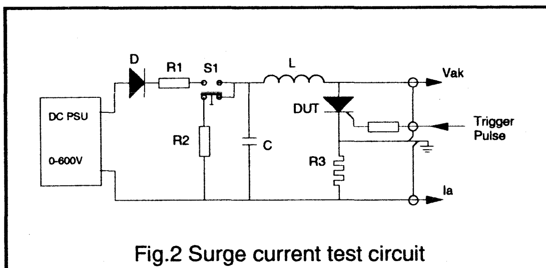


Fig.2 Surge current test circuit

Pushbutton S1 and resistor R2 are a safety feature. R2 keeps C discharged until S1 is pressed. The trigger pulse needs a button on the pulse generator to be pressed which means both hands are occupied and kept away from the test circuit high voltages.

Choice of L & C

The width of the half sine pulse from an LC circuit is:

$$t_{pulse} = \pi \cdot \sqrt{L \cdot C}$$

and the theoretical peak value of the current by:

$$I_{peak} = V \cdot \sqrt{\frac{C}{L}}$$

These equations assume that the circuit has no series resistance to damp the resonant action which would result in a longer but lower pulse. Minimising these effects was considered to be important so care was taken during the building of the circuits to keep the resistance to a minimum. To this end capacitors with low ESR were chosen, the inductors were wound using heavy gauge wire and the loop C / L / DUT / R3 was kept as short as possible

It was decided to test the devices at three different pulse widths - 10 µs, 100 µs and 1 ms - so three sets of L and C were needed. The values were selected with the help of a 'spreadsheet' program running on an PC compatible computer. The values which were finally chosen are shown in Table 1. Also given in Table 1 are the theoretical peak currents that the L / C combination would produce for a initial voltage on C of 600 V.

Test Procedure

As was mentioned earlier the test method called for each device to be subjected to a series of current pulses of increasing amplitude. The resolution with which the current capability is assessed is defined by the size of each increase in current. It was decided that steps of approximately 5% would give a reasonably resolution.

Experimentation indicated that the clearest indication of device damage was obtained by looking for changes in the off-state breakdown voltage. So after each current pulse the DUT was removed from the test circuit and checked on a curve tracer. This procedure did slow the testing but it was felt that it would result in greater accuracy.

Pulse Width	C (µF)	L (µH)	Ipeak (A)
10 µs	13.6	0.75	2564
100 µs	100	10	1885
1 ms	660	154	1244

Table 1 Inductor and Capacitor Values

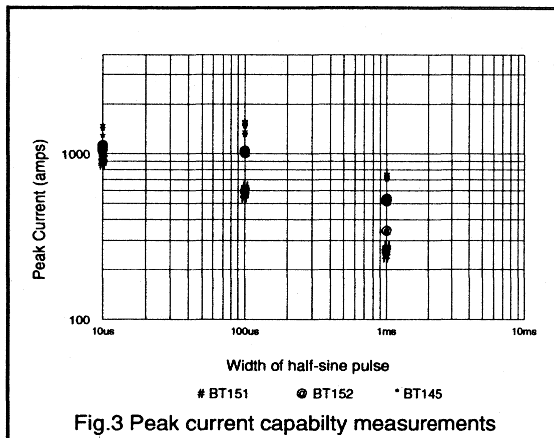


Fig.3 Peak current capabilty measurements

It was also decided that, since this work was attempting to determine the current that a device could survive - not which killed it, the figure actually quoted in the results for a device's current capability would be the value of the pulse prior to the one which caused damage.

Test Results

Figure 3 is a graph showing the measured current capabilities of all of the tested devices. Table 2 summarises the measurements by giving the mean of the results for the three device types at each of the pulse widths. Table 3 expresses the mean values as factors of the device I_{TSM} rating. This table also gives the factors that the various 'rules' would have predicted for the various pulse widths.

	Mean Peak Current Capability (Amps)		
Pulse Width	BT151	BT152	BT145
10 µs	912	1092	1333
100 µs	595	1021	1328
1 ms	264	490	697

Table 2 Measured Current Capability

	Measured Factor			Predicted Factor (by I^nt rule)			
Pulse Width	BT 151	BT 152	BT 145	n=2	n=3	n=4	n= log(1/t)
10 µs	9.1	5.5	4.4	31.6	10.0	5.6	4.0
100 µs	6.0	5.1	4.4	10.0	4.6	3.2	3.2
1 ms	2.6	2.4	2.3	3.2	2.2	1.8	2.2

Table 3 Measured and Predicted I_{TSM} Multiplication Factors

Interpretation of Results

It had been hoped that the measurements would give clear indication of which of the 'rules' would give the most accurate prediction of performance. However, an inspection of Table 3 clearly shows that there is no correlation between any of the predicted factors and the measured factors. In fact the variation in the factors between the various device types would indicated that no rule based on an I^nt function alone can give an accurate prediction. This implies that something else will have to be taken into account.

Further study of Fig.3 reveals that the difference in the peak current capability of the three device types is becoming less as the pulses become shorter. This could be explained by a reduction in the active area of the larger crystals, making them appear to be smaller than they actually are. This is consistent with the known fact that not all areas of a thyristor turn-on simultaneously - the conduction region tends to spread out from the gate. If the pulse duration is less than the time it takes for all areas of the device to turn-on, then the current flows through only part of the crystal, reducing the effective size of the device. If the rate at which the conduction area turns-on is constant then the time taken for a small device to be completely ON is shorter than for a large device. This would explain why the performance increase of the BT145 starts falling off before that of the BT151.

Proposed Prediction Method

The above interpretation leads one to believe that the original energy handling rule, which says that I^2t is a constant, may still be correct but that the performance it predicts will 'roll-off' if the pulse duration is less than some critical value. The equation which was developed to have the necessary characteristics was:

$$I_{pk} = I_{TSM} \cdot \left(\frac{0.01}{t_p}\right)^{\frac{1}{2}} \cdot \left(\frac{t_p}{t_p + t_{crit}}\right)^{\frac{1}{2}}$$

which simplifies to:-

$$I_{pk} = I_{TSM} \cdot \sqrt{\left(\frac{0.01}{t_p + t_{crit}}\right)}$$

where t_{crit} is proportional to - but not necessarily equal to - the time taken to turn-on all the active area of the crystal and is calculated from:-

$$t_{crit} = \frac{A}{R}$$

where: A = crystal area
R = constant expressing the rate at which the area is turned-on.

Preferably A should be the area of the cathode but this information is not always available. As an alternative the total crystal area can be used if the value of R is adjusted accordingly. This will inevitably introduce an error, because cathode and crystal areas are not directly proportional, but it should be relatively small.

R was determined empirically to be approximately 0.02 m^2/s Using this value of R gives the values of t_{crit} shown in Table 3. Using these values in the above equation predicts that the peak current handling capability of the BT151, BT152 and BT145 would be as shown in Fig.4.

Device	t_{crit}
BT151	148 µs
BT152	410 µs
BT145	563 µs

Table 3. Calculated Values of t_{crit}

Conclusions

The first conclusion that can be drawn from this work is that a thyristor, with average rating of only 7.5A, is capable of conducting, without damage, a peak current greater than 100 times this value in a short pulse. Furthermore the power required to trigger the device into conducting this current can be <1 µW. This capability has always been known and indeed the surge rating given in the data sheet, gives a value for it at pulse widths of around 10 ms. What has been missing is a reliable method of predicting what the peak current capability of a device is for much shorter pulses.

The results obtained using the test methods indicate that the previously suggested 'rules' fail to take into account the effect that crystal size has on the increase in performance.

In this section, an equation has been proposed which takes crystal size into account by using it to calculate a factor called t_{crit}. This time is then used to 'roll-off' the performance increase predicted by the original energy handling equation - I^2t = constant. This results, in what is believed to be, a more accurate means of estimating of the capability of a device for a half sine pulse with a duration between 10 µs and 10 ms.

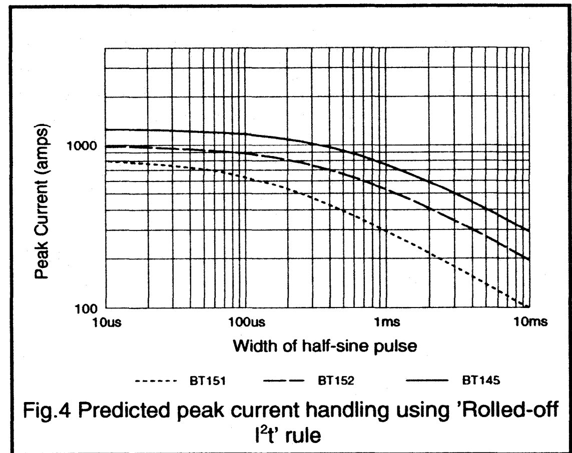


Fig.4 Predicted peak current handling using 'Rolled-off I^2t' rule

6.1.4 Understanding thyristor and triac data

The importance of reliable and comprehensive data for power semiconductor devices, together with the advantages of the absolute maximum rating system is clear. This present article describes the data sheet descriptions of Philips thyristors and triacs, and aims to enable the circuit designer to use our published data to the full and to be confident that it truly describes the performance of the devices.

A brief survey of short-form catalogues is an insufficient method of comparing different devices. Published ratings and characteristics require supporting information to truly describe the capabilities of devices; thus comparisons between devices whose performance appears to be similar should not be made on economic grounds alone. Manufacturers have been known to quote ratings in such a way as to give a false impression of the capabilities of their devices.

Ratings and characteristics given in published data should always be quoted with the conditions to which they apply, and these conditions should be those likely to occur in operation. Furthermore, it is important to define the rating or characteristic being quoted. Only if data is both complete and unambiguous can a true comparison be made between the capabilities of different types.

Thyristors

Thyristor is a generic term of a semiconductor device which has four semiconductor layers and operates as a switch, having stable on and off states. A thyristor can have two, three, or four terminals but common usage has confined the term thyristor to three terminal devices. Two-terminal devices are known as switching diodes, and four-terminal devices are known as silicon controlled switches. The common, or three-terminal, thyristor is also known as the reverse blocking triode thyristor or the silicon controlled rectifier (SCR). Figure 1 shows the circuit symbol and a schematic diagram of the thyristor. All Philips thyristors are p-gate types; that is, the anode is connected to the stud (or heatsink) of the encapsulation.

The thyristor will conduct a load current in one direction only, as will a rectifier diode. However, the thyristor will only conduct this load current when it has been 'triggered'; this is the essential property of the thyristor.

Figure 2 shows the static characteristic of the thyristor. When a small negative voltage is applied to the device, only a small reverse leakage current flows. As the reverse voltage is increased, the leakage current increases until avalanche breakdown occurs. If a positive voltage is applied, then again a small forward leakage current flows which increases as the forward voltage increases. When the forward voltage reaches the breakover voltage $V_{(BO)}$, turn-on is initiated by avalanche breakdown and the voltage across the thyristor falls to the on state voltage V_T.

However, turn-on can occur when the forward (anode-to-cathode) voltage is less than $V_{(BO)}$ if the thyristor is triggered by injecting a pulse of current into the gate. If the device is to remain in the on-state, this trigger pulse must remain until the current through the thyristor exceeds the latching current I_L. Once the on state is established, the holding current I_H is the minimum current that can flow through the thyristor and still maintain conduction. The load current must be reduced to below I_H to turn the thyristor off; for instance, by reducing the voltage across the thyristor and load to zero.

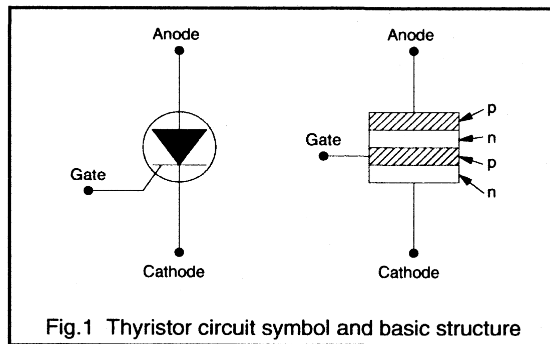


Fig.1 Thyristor circuit symbol and basic structure

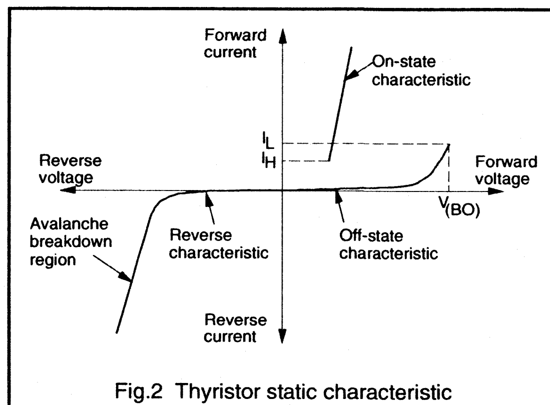


Fig.2 Thyristor static characteristic

Thyristors are normally turned on by triggering with a gate signal but they can also be turned on by exceeding either the forward breakover voltage or the permitted rate or rise of anode voltage dV_D/dt. However, these alternative methods of switching to the conducting state should be avoided by suitable circuit design.

Triacs

The triac, or bidirectional triode thyristor, is a device that can be used to pass or block current in either direction; it is therefore an a.c. power control device. It is equivalent to two thyristors in anti-parallel with a common gate electrode. However, it only requires one heatsink compared to the two heatsinks required for the anti-parallel thyristor configuration. Thus the triac saves both cost and space in a.c. applications.

Figure 3 shows the triac circuit symbol and a simplified cross-section of the device. The triac has two main terminals MT1 and MT2 (the load connections) and a single gate. The main terminals are connected to both p and n regions since current can be conducted in both directions. The gate is similarly connected, since a triac can be triggered by both negative and positive pulses.

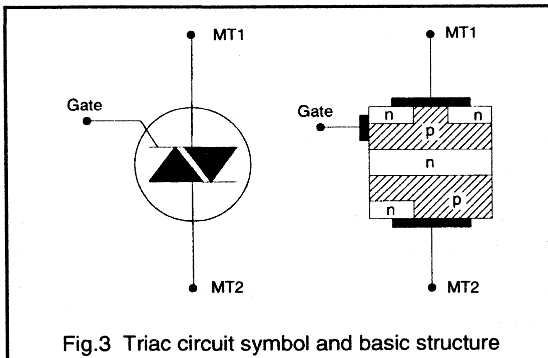


Fig.3 Triac circuit symbol and basic structure

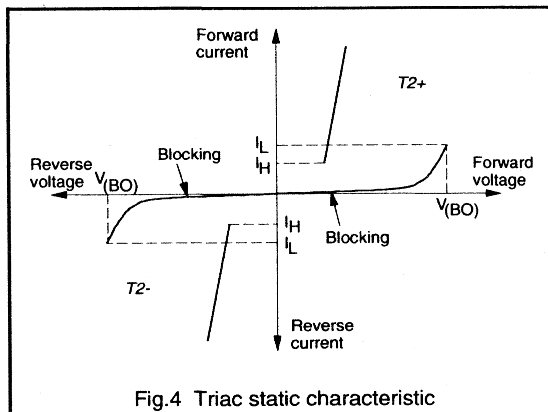


Fig.4 Triac static characteristic

The on-state voltage/current characteristic of a triac resembles that of a thyristor. The triac static characteristic of Fig.4 shows that the triac is a bidirectional switch. The condition when terminal 2 of the triac is positive with respect to terminal 1 is denoted in data by the term 'T2+'. If the triac is not triggered, the small leakage current increases as the voltage increases until the breakover voltage $V_{(BO)}$ is reached and the triac then turns on. As with the thyristor, however, the triac can be triggered below $V_{(BO)}$ by a gate pulse, provided that the current through the device exceeds the latching current I_L before the trigger pulse is removed. The triac, like the thyristor, has holding current values below which conduction cannot be maintained.

When terminal 2 is negative with respect to terminal 1 (T2-) the blocking and conducting characteristics are similar to those in the T2+ condition, but the polarities are reversed. The triac can be triggered in both directions by either negative (G-) or positive (G+) pulses on the gate, as shown in Table 1. The actual values of gate trigger current, holding current and latching current may be slightly different in the different operating quadrants of the triac due to the internal structure of the device.

Quadrant	Polarity of T2 wrt T1	Gate polarity
1 (1+)	T2+	G+
2 (1-)	T2+	G-
3 (3+)	T2-	G-
4 (3-)	T2-	G+

Table 1 Operating quadrants for triacs

Device data

Anode to cathode voltage ratings

The voltage of the a.c. mains is usually regarded as a smooth sinewave. In practice, however, there are a variety of transients, some occurring regularly and others only occasionally (Fig.5). Although some transients may be removed by filters, thyristors must still handle anode to cathode voltages in excess of the nominal mains value.

The following reverse off-state voltage ratings are given in our published data:

V_{RSM}: the non-repetitive peak reverse voltage. This is the allowable peak value of non-repetitive voltage transients, and is quoted with the maximum duration of transient that can be handled (usually t < 10ms).

V_{RRM}: the repetitive peak reverse voltage. This is the allowable peak value of transients occurring every cycle.

V_{RWM}: the peak working reverse voltage. This is the maximum continuous peak voltage rating in the reverse direction, neglecting transients. It corresponds to the peak negative value (often with a safety factor) of the sinusoidal supply voltage.

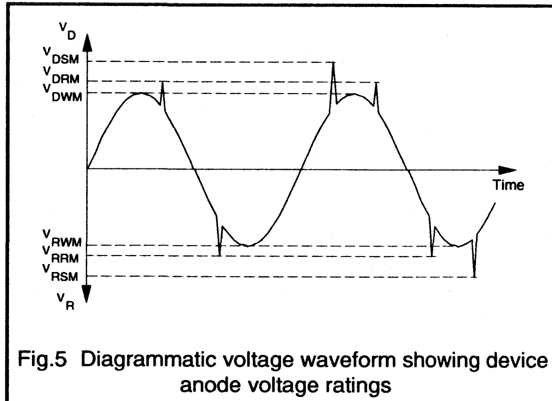


Fig.5 Diagrammatic voltage waveform showing device anode voltage ratings

The forward off-state voltages corresponding to V_{RSM}, V_{RRM} and V_{RWM} are listed below.

V_{DSM}: the non-repetitive peak off-state voltage applied in the forward direction.

V_{DRM}: the repetitive peak off-state voltage applied in the forward direction.

V_{DWM}: the peak working off-state voltage applied in the forward direction.

Both the repetitive and non-repetitive voltage ratings are determined partly by the voltage limit that prevents the thyristor being driven into forward or reverse breakdown, and partly by the instantaneous energy (resulting from an increase in leakage current) that can be dissipated in the device without exceeding the rated junction temperature.

When a thyristor is to operate directly from the mains supply, it is advisable to choose a device whose repetitive peak voltage ratings V_{RRM} and V_{DRM} are at least 1.5 times the peak value of the sinusoidal supply voltage. This figure forms part of the device type number; for example BTW38-600R where 600 corresponds to V_{DRM}, V_{RRM}=600V and the final R (for Reverse) indicates that the anode of the device is connected to the stud/heatsink.

Anode-to-cathode current ratings

The following current ratings, described by the waveforms shown in Fig.6, are given in our published data. Note that the suffix $_T$ implies that the thyristor is in the on state.

$I_{T(AV)}$: the average value of the idealised mains current waveform taken over one cycle, assuming conduction over 180˚. For devices mounted on heatsinks, the $I_{T(AV)}$ rating should be quoted for a particular mounting-base temperature T_{mb}; our devices are generally characterised at a mounting-base temperature of at least 85˚C. A device can have an artificially high current rating if the mounting-base temperature is unrealistically low; ratings with no associated mounting-base temperature should be regarded with suspicion.

$I_{T(RMS)}$: the rms on-state current. This rating gives the maximum rms current that the thyristor can handle. It is important for applications when the device current waveform is described by a high value form factor. For such conditions the rms current rather than the average current may be the limiting rating.

I_{TRM}: the repetitive peak forward current. This rating is the peak current that can be drawn each cycle providing that the average and rms current ratings are not exceeded.

I_{TSM}: the non-repetitive (surge) peak forward current. This rating is the peak permitted value of non-repetitive transients, and depends on the duration of the surge. Our published data quotes the I_{TSM} rating for t=10ms, the duration of a half-cycle of 50Hz mains. However some manufacturers quote I_{TSM} for t=8.3ms (half-cycle of 60Hz mains), and thus surge ratings for devices quoted at t=8.3ms should be approximately uprated (divided by 0.83) before comparing them with t=10ms surge ratings.

The surge rating also depends on the conditions under which it occurs. Our data sheets quote I_{TSM} rating under the worst probable conditions that is, T_j=$T_{j(max)}$ immediately prior to the surge, followed by reapplied $V_{RWM(max)}$ immediately after the surge. An unrealistically high I_{TSM} rating could be quoted if, for example, T_j<$T_{j(max)}$ prior to the surge and then the full rated voltage is not reapplied.

Published data also includes curves for I_{TSM} against time which show the maximum allowable rms current which can occur during inrush or start-up conditions. The duration of the inrush transient and the mounting base temperature prior to operation determine the maximum allowable rms inrush current.

dI/dt: the rate of rise of on-state current permissible after triggering. An excessive rate of rise of current causes local heating and thus damage to the device. The rate of rise of current is determined by both the supply and load impedances, and can be limited by additional series inductance in the circuit.

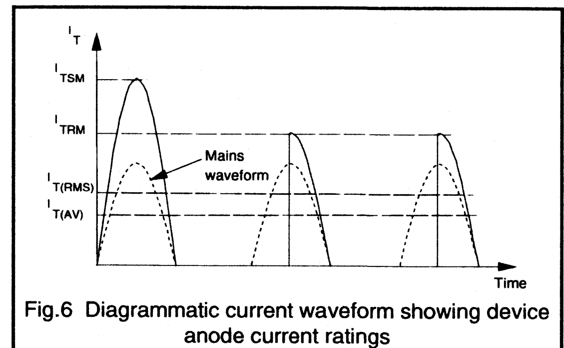


Fig.6 Diagrammatic current waveform showing device anode current ratings

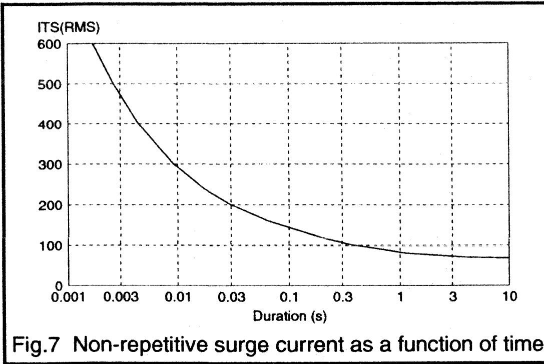


Fig.7 Non-repetitive surge current as a function of time

I^2t: a dimensional convenience specifying the capability of a thyristor to absorb energy. This rating is required for the selection of fuses to protect the thyristor against excessive currents caused by fault conditions. It is normally only valid over the range 3 to 10ms. In our published data, a value is quoted for 10ms, in which case:

$$I^2t = \int i^2.dt \qquad (1)$$

$$= \left(\frac{I_{TSM}}{\sqrt{2}}\right)^2 \times 10.10^{-3} \quad (A^2s)$$

The user should match the minimum I^2t capability of the thyristor to the worst case I^2t let-through of a range of nominally rated fuses in order to select a fuse that will protect the device under worst probable conditions.

Values of I^2t other than those quoted for 10ms can be estimated by referring to the appropriate published curves of non-repetitive surge current against time. For example, Fig.7 is the non repetitive surge current curve for a thyristor whose I^2t at 10ms is 800A^2s. From Fig.7, $I_{TS(RMS)}$ at 3ms is 470A and therefore I^2t at 3ms is given by:

$$I^2t\,(3ms) = I^2_{TS(RMS)} \times t$$

$$= 470^2 \times 3.10^{-3}$$

$$= 662.7A^2s$$

To summarise, when selecting an appropriate fuse the following conditions must be taken into account.

1. The fuse must have an rms current rating equal to, or less than, that of the thyristor it is to protect.
2. The I^2t at the rms working voltage must be less than that of the thyristor taken over the fuse operating time.
3. The arc voltage of the fuse must be less than the V_{RSM} rating of the thyristor.

Gate-to-cathode ratings

The following gate-to-cathode ratings are given in the published data.

V_{RGM}: the gate peak reverse voltage.

$P_{G(AV)}$: the mean gate power, averaged over a 20ms period.

P_{GM}: the peak gate power dissipation.

The gate-to-cathode power ratings should not be exceeded if over-heating of the gate-cathode junction is to be avoided.

Temperature ratings

Two temperature ratings are given in the published data.

T_{stg}: the storage temperature. Both maximum and minimum values of the temperature at which a device can be stored are given.

T_j: the junction temperature. This is one of the principal semiconductor ratings since it limits the maximum power that a device can handle. The junction temperature rating quoted in our published data is the highest value of junction temperature at which the device may be continuously operated to ensure a long life.

Thermal characteristics

The following thermal resistances and impedances are given in our data.

$R_{th(j-a)}$: the thermal resistance between the junction of the device and ambient (assumed to be the surrounding air).

$R_{th(j-mb)}$: the thermal resistance between the junction and mounting base of the device.

$R_{th(mb-a)}$: the thermal resistance between the mounting base of the device and the heatsink (contact thermal resistance).

$Z_{th(j-mb)}$: the transient thermal impedance between the junction and mounting-base of the device. The value given in the published data is for non-repetitive conditions and a particular pulse duration. Under pulse conditions, thermal impedances rather than thermal resistances should be considered. Higher peak power dissipation is permitted under pulse conditions since the materials in a thyristor have a definite thermal capacity, and thus the critical junction temperature will not be reached instantaneously, even when excessive power is being dissipated in the device. The published data also contains graphs of $Z_{th(j-mb)}$ against time (for non-repetitive conditions) such as those shown in Fig.8.

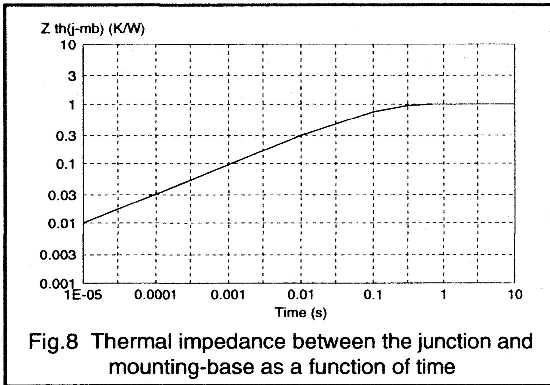


Fig.8 Thermal impedance between the junction and mounting-base as a function of time

The values of the various thermal resistances between the thyristor junction and the surroundings must be considered to ensure that the junction temperature rating is not exceeded. The heat generated in a semiconductor chip flows by various paths to the surroundings. Fig.9 shows the various thermal resistances to be taken into account in this process. With no heatsink, the thermal resistance from the mounting-base to the surroundings is given by $R_{th(mb-a)}$. When a heatsink is used, the heat loss direct to the surroundings from the mounting-base is negligible owing to the relatively high value of $R_{th(mb-a)}$ and thus:

$$R_{th(mb-a)} = R_{th(mb-h)} + R_{th(h-a)} \qquad (2)$$

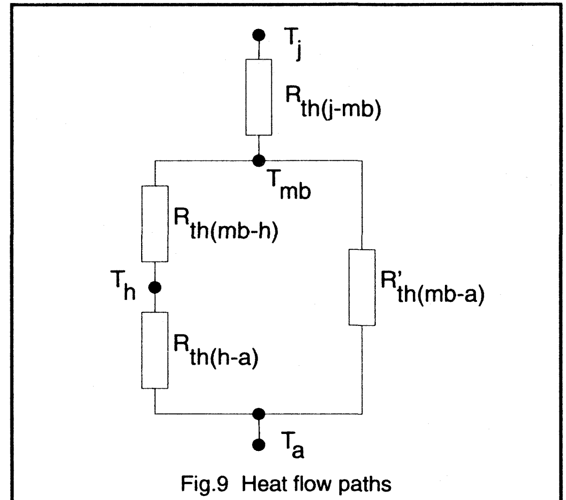


Fig.9 Heat flow paths

Where appropriate, our published data contains power graphs such as that in Fig.10. These characteristics relate the total power dissipated in the thyristor P, the average forward current $I_{T(AV)}$, the ambient temperature T_a, and the thermal resistance $R_{th(mb-a)}$, with the form factor, *a*, as a parameter. They enable the designer to work out the required mounting arrangement from the conditions under which the thyristor is to be operated.

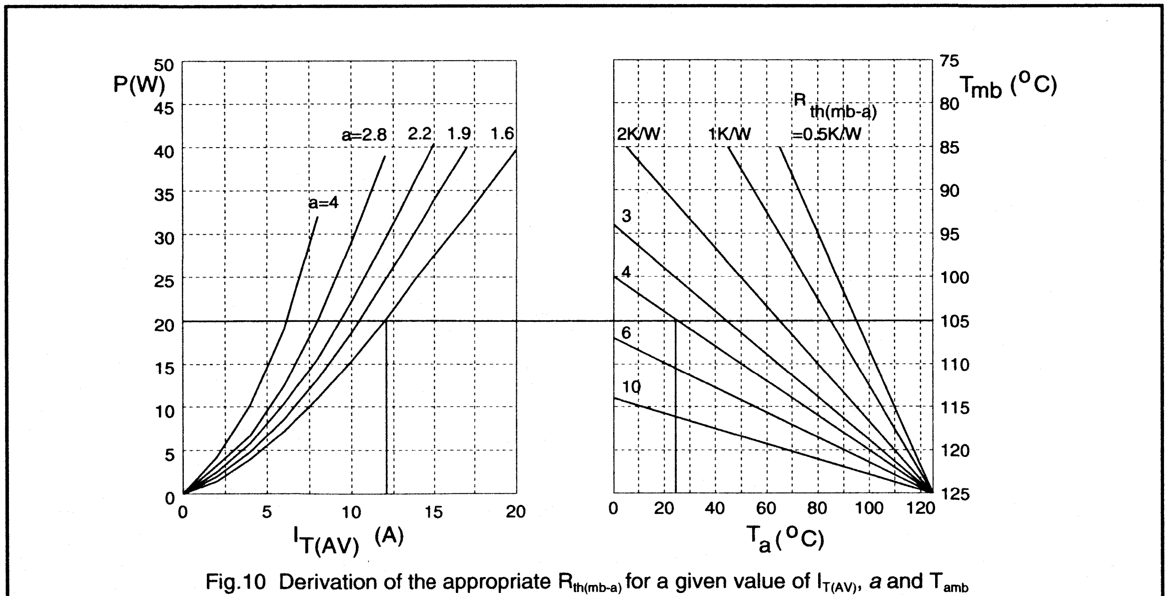


Fig.10 Derivation of the appropriate $R_{th(mb-a)}$ for a given value of $I_{T(AV)}$, *a* and T_{amb}

Usually, the characteristics are designed for use in 50Hz sinusoidal applications, when the procedure below should be followed.

1. Determine the values of $I_{T(AV)}$ and $I_{T(RMS)}$ for the relevant application.
2. Determine the form factor, which is given by:

$$a = \frac{I_{T(RMS)}}{I_{T(AV)}} \quad (3)$$

3. Starting from the appropriate value of $I_{T(AV)}$ on a curve such as Fig.10, move vertically upwards to intersect the appropriate form factor curve (interpolating if necessary).
4. This intersection gives the power dissipated in the thyristor on the left-hand axis of the combined graph and the mounting base temperature on the right hand axis.
5. Moving horizontally across from this intersection to the appropriate value of ambient temperature gives the required mounting base to ambient thermal resistance $R_{th(mb-a)}$.
6. The required heatsink thermal resistance $R_{th(h-a)}$ can now be calculated from Equation 2 since the mounting base to heatsink thermal resistance $R_{th(mb-h)}$ is given in the published data.

Example

The thyristor to which Fig.10 applies is operated at an average forward current $I_{T(AV)}$ of 12A and an rms forward current $I_{T(RMS)}$ of 19.2A. The maximum anticipated ambient temperature is 25˚C. Now, Equation 3 gives,

$$a = \frac{19.2}{12} = 1.6$$

Figure 10 gives the power as P=20W and the mounting-base temperature as T_{mb}=105˚C. Also, at this power and ambient temperature of 25˚C, Fig.10 gives the value of $R_{th(mb-a)}$ to be 4˚C/W. The published data gives the value of $R_{th(mb-h)}$ (using a heatsink compound) to be 0.2˚C/W and then Equation 2 gives

$$R_{th(h-a)} = 4 - 0.2 = 3.8\ °C/W$$

Mounting torque

Two values of mounting torque (for stud-mounted devices) are given in the published data. A minimum value is quoted below which the contact thermal resistance rises owing to poor contact, and a maximum value is given above which the contact thermal resistance again rises owing to deformation of the stud or cracking of the crystal.

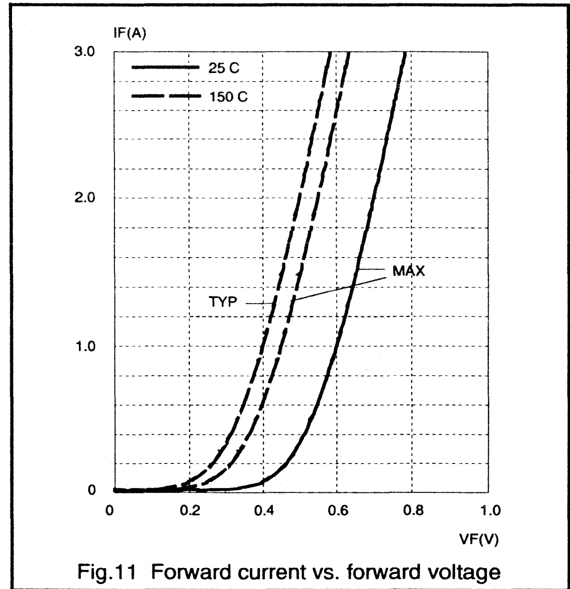


Fig.11 Forward current vs. forward voltage

The surface of a device case and heatsink cannot be perfectly flat, and thus contact will take place on several points only, with a small air-gap over the rest of the contact area. The use of a soft substance to fill this gap will lower the contact thermal resistance. We recommend the use of proprietary heatsinking compounds which consist of a silicone grease loaded with an electrically insulating and good thermal conducting powder such as alumina.

Anode-to-cathode characteristics

The following anode-to-cathode characteristics are included in the published data.

I_R: the reverse current. This parameter is given for the worst probable conditions; that is, the reverse voltage V_R=$V_{RWM(max)}$ and a high T_j.

I_D: the off-state current. This parameter is again given for the worst probable conditions; that is, the forward voltage V_D=$V_{DWM(max)}$ and a high T_j.

I_L: the latching current (Fig.2). This parameter is quoted at a particular value of junction temperature.

I_H: the holding current (Fig.2). This parameter is quoted at a particular value of junction temperature.

V_T: the forward voltage when the thyristor is conducting. This parameter is measured at particular values of forward current and junction temperature. The junction temperature is usually low (T_j=25˚C, for example) since this is the worst case. The measurement must be performed under pulse conditions to maintain the low junction temperature. The

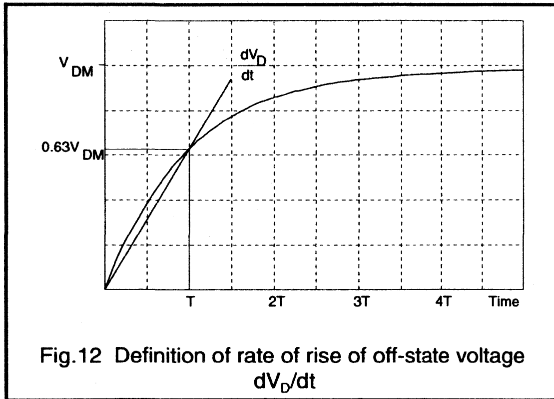


Fig.12 Definition of rate of rise of off-state voltage dV_D/dt

published data also contains curves of forward current against forward voltage, usually for two values of the junction temperature: 25˚C and $T_{j(max)}$ (Fig.11).

dV/dt: the rate of rise of off-state voltage that will not trigger any device. This parameter is given at maximum values of junction temperature $T_{j(max)}$ and forward voltage V_D=$V_{DRM(max)}$.

The values of dV_D/dt quoted in our published data are normally specified assuming an exponential waveform. This facilitates the design of RC snubber circuits for device protection when required. Fig.12 illustrates the definition of dV_D/dt. The final voltage applied to the device V_{DM} is chosen as $V_{DRM(max)}$ and the junction temperature is T_j=$T_{j(max)}$.

Fig.12 shows that dV_D/dt is given by the expression:

$$\frac{dV_D}{dt} = \frac{0.63V_{DM}}{T}$$

$$= \frac{0.63 \times 2/3V_{DRM(max)}}{T}$$

$$= \frac{0.42V_{DRM(max)}}{T} \qquad (V/\mu s)$$

where T is the exponential time constant.

The dV_D/dt capability of a thyristor increases as the junction temperature decreases. Thus curves such as those shown in Fig.13a) are provided in the published data so that designers can uprate devices operated at lower junction temperatures.

The dV_D/dt characteristic can also be increased by operating the device at a low supply voltage. Thus the published data also contains curves such as Fig.13b) which shows how dV_D/dt increases as the ratio V_{DM}/V_{DRM} max decreases. Note that V_{DM} is unlikely to be greater than $^2/_3V_{DRM(max)}$ (usually owing to the restriction of $V_{DWM(max)}$) and therefore the fact that dV_D/dt approaches zero as V_{DM} increases above the value of $^2/_3V_{DRM(max)}$ does not cause problems.

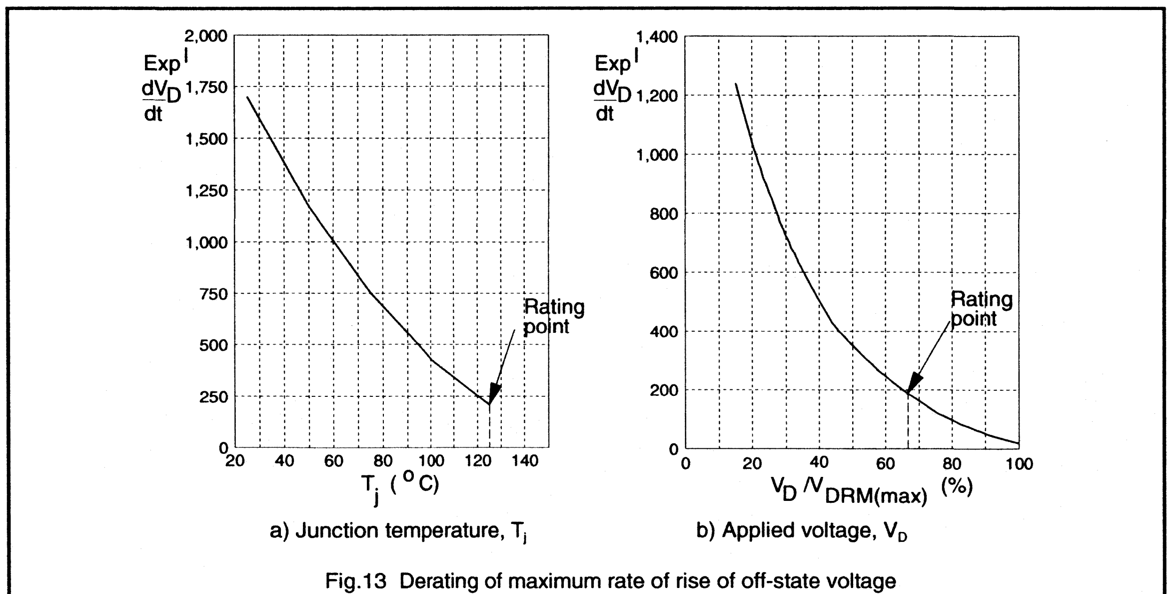
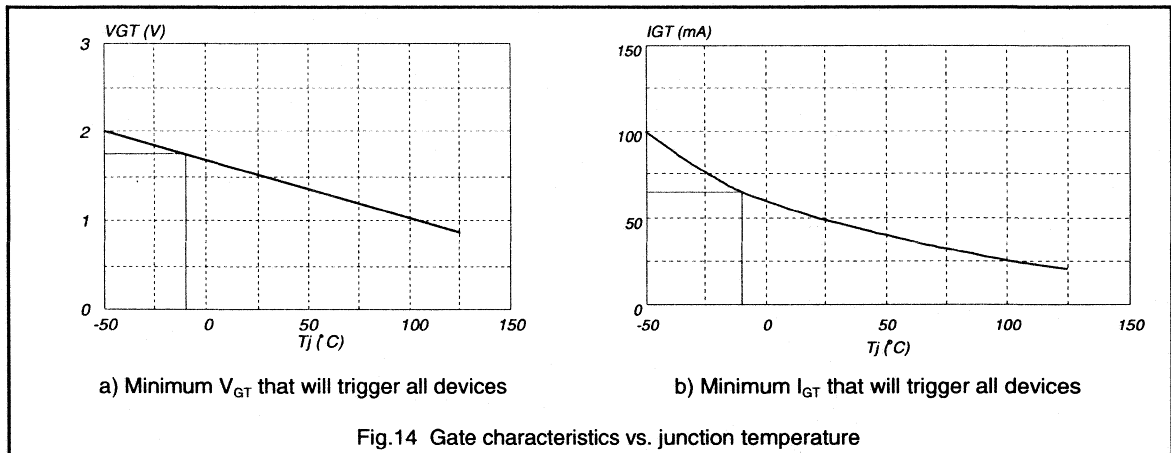


Fig.13 Derating of maximum rate of rise of off-state voltage



a) Minimum V_{GT} that will trigger all devices

b) Minimum I_{GT} that will trigger all devices

Fig.14 Gate characteristics vs. junction temperature

Gate-to-cathode characteristics

The following gate-to-cathode characteristics are given in the published data.

V_{GT}: the gate-to-cathode voltage that will trigger all devices. This characteristic should be quoted for particular values of applied voltage V_D and junction temperature.

I_{GT}: the gate-to-cathode current that will trigger all devices. This characteristic should be quoted under the worst probably conditions; that is, forward voltage V_D=$V_{DRM(max)}$ and junction temperature T_j=$T_{j(max)}$.

A gate drive circuit must be designed which is capable of supplying at least the required minimum voltage and current without exceeding the maximum power rating of the gate junction. Curves such as those shown in Fig.14 (which relate the minimum values of V_{GT} and I_{GT} for safe triggering to the junction temperature) are provided in data. The following design procedure is recommended to construct a gate drive circuit load-line on the power curves shown in Fig.15.

1. Determine the maximum average gate power dissipation $P_{G(AV)}$ from the published data (normally 0.5W, 1.0W, or 2.0W) and then use the appropriate choice of x-axis scaling in Fig.15.
2. Estimate the minimum ambient temperature at which the device will operate, and then determine the minimum values of V_{GT} and I_{GT} from curves such as Figs 14a) and 14b) in the published data. Note that it is assumed that at switch-on T_j=T_a.
3. Determine the minimum open-circuit voltage of the trigger pulse drive circuit: this is the first co-ordinate on the load line at I_G=0.
4. Using the appropriate horizontal scaling for the device ($P_{G(AV)}$=0.5W, 1.0W or 2.0W), plot a second point on the power curve whose co-ordinates are given by $V_{GT(min)}$ and 5x$I_{GT(min)}$. Construct a load line between these two points. The slope of this load gives the maximum allowable source resistance for the drive unit.
5. Check the power dissipation by ensuring that the load line must not intersect the curve for the maximum peak gate power $P_{GM(max)}$ which is the outermost (δ=0.1) curve of Fig.15. The load line must also not intersect the curve which represents the maximum average gate power $P_{G(AV)}$ modified by the pulse mark-space ratio where:

$$P_{GM(\max)} = \frac{P_{AV}}{\delta} \quad (5)$$

For instance, in Fig.15 for a thyristor with $P_{G(AV)}$=1W, the δ=0.25 curve can be used for a gate drive with a 1:3 mark-space ratio giving an allowable maximum gate power dissipation of $P_{GM(max)}$=4W.

An illustration of how the above design procedure operates to give an acceptable gate drive circuit is presented in the following example.

Example

A thyristor has the V_{GT}/T_j and I_{GT}/T_j characteristics shown in Fig.14 and is rated with $P_{G(AV)}$=0.5W and $P_{GM(max)}$=5W. A suitable trigger circuit operating with δ_{max}=0.25, $V_{GT(min)}$=4.5V, $I_{GT(max)}$=620mA and $T_{a(min)}$=-10˚C is to be designed. Determine its suitability for this device.

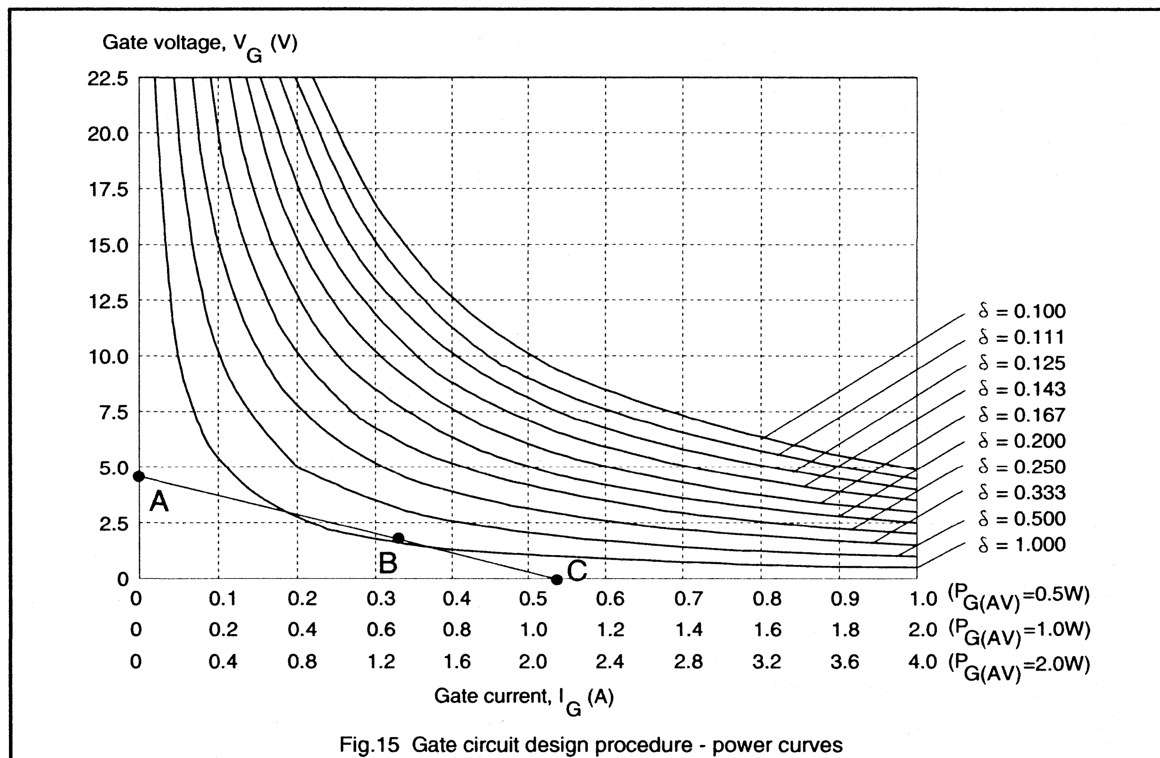


Fig.15 Gate circuit design procedure - power curves

1. Select the top x-axis scale of Fig.15 ($P_{G(AV)}$=0.5W).
2. From Fig.14 $V_{GT(min)}$=1.75V, and IGT(min)=66mA.
3. At minimum supply voltage the open-circuit gate voltage is 4.5V giving point 'A' in Fig.15. Point B is plotted at the co-ordinates $V_{GT(min)}$ and 5x$I_{GT(min)}$, that is at 1.75V and 330mA, and load line ABC is constructed as shown. Note that point C is the maximum current required at I_G=570mA and is within the capability of the drive circuit.
4. As required the load line does not intersect the $P_{G(max)}$ (δ=0.1). The gate drive duty cycle, δ, is 0.25. Therefore $P_{GM(max)} = P_{G(AV)}/\delta = 0.5/0.25 = 2W$. As required, the load line ABC does not intersect the δ=0.25 curve.

Switching characteristics

Two important switching characteristics are usually included in our published data. They are the gate-controlled turn-on time t_{gt} (divided into a turn-on delay time, t_d, and a rise time, t_r) and the circuit-commutated turn-off time, t_q.

Gate-controlled turn-on time, t_{gt}

Anode current does not commence flowing in the thyristor at the instant that the gate current is applied. There is a period which elapses between the application of the trigger pulse and the onset of the anode current which is known as the delay time t_d (Fig.16). The time taken for the anode voltage to fall from 90% to 10% of its initial value is known as the rise time t_r. The sum of the delay time and the rise time is known as the gate-controlled turn-on time t_{gt}.

The gate controlled turn-on time depends on the conditions under which it is measured, and thus the following conditions should be specified in the published data.

-Off-state voltage; usually V_D=$V_{DWM(max)}$.
-On-state current.
-Gate trigger current; high gate currents reduce t_{gt}.
-Rate of rise of gate current; high values reduce t_{gt}.
-Junction temperature; high temperatures reduce t_{gt}.

Circuit-commutated turn-off time

When a thyristor has been conducting and is reverse-biased, it does not immediately go into the forward blocking state: minority charge carriers have to be cleared away by recombination and diffusion processes before the device can block reapplied off-state voltage. The time from when the instant that the anode current passes through zero to the instant that the thyristor is capable of block reapplied off-state voltage is the circuit-commutated

turn-off time t_q (Fig.17).

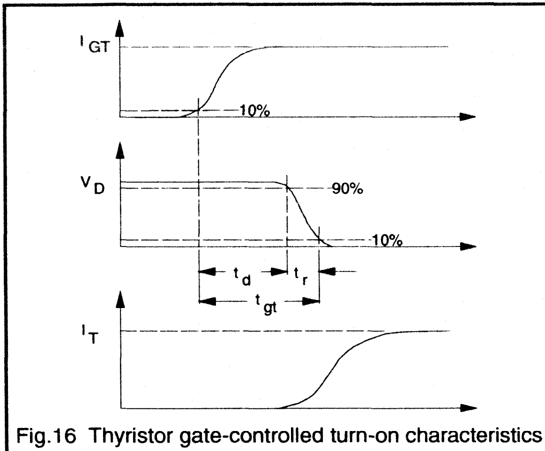


Fig.16 Thyristor gate-controlled turn-on characteristics

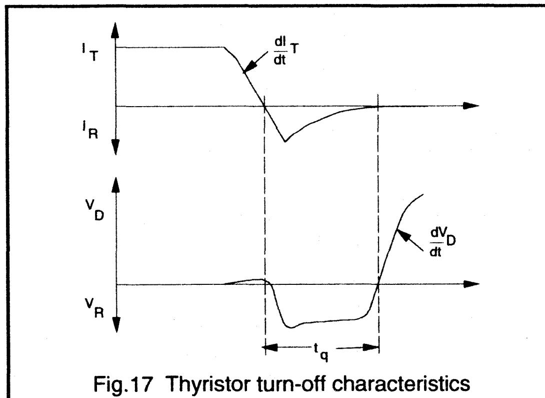


Fig.17 Thyristor turn-off characteristics

The following conditions should be given when t_q is quoted.

-On-state current; high currents increase t_q.
-Reverse voltage; low voltages increase t_q.
-Rate of fall of anode current; high rates increase t_q.
-Rate of rise of reapplied off-state voltage; high rates increase t_q.
-Junction temperature; high temperatures increase t_q.
-Gate bias; negative voltages decrease t_q.

Triac ratings

The ratings and characteristics of the triac are similar to those of the thyristor, except that the triac does not have any reverse voltage ratings (a reverse voltage in one quadrant is the forward voltage in the opposite quadrant). However, one characteristic requires special attention when choosing triacs; the rate of re-applied voltage that the triac will withstand without uncontrolled turn-on.

If a triac is turned off by simply rapidly reversing the supply voltage, the recovery current in the device would simply switch it on in the opposite direction. To guarantee reduction of the current below its holding value, the supply voltage must be reduced to zero and held there for a sufficient time to allow the recombination of any stored charge in the device. To ensure turn-off, the rate of fall of current during the commutation interval (turn-off period) and the rate of rise of re-applied voltage after commutation must both be restricted. An excessive rate of fall of current creates a large number of residual charge carriers which are then available to initiate turn-on when the voltage across the triac rises.

With supply frequencies up to around 400Hz and a sinusoidal waveform, commutation does not present any problems when the load is purely resistive, since the current and voltage are in phase. As shown in Fig.18 the rate of fall of on-state current -dI/dt, given by Equation 6, and the rate of rise of commutating voltage dV_{com}/dt, given by equation 7, are sufficiently low to allow the stored charge in the device to fully recombine. The triac is thus easily able to block the rising reapplied voltage dV_{com}/dt.

$$dI/dt = 2\pi f.\sqrt{2}I_{T(RMS)} \tag{6}$$

$$dV_{com}/dt = 2\pi f.\sqrt{2}V_{(RMS)} \tag{7}$$

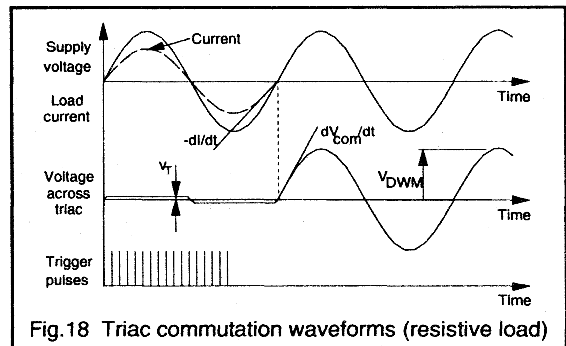


Fig.18 Triac commutation waveforms (resistive load)

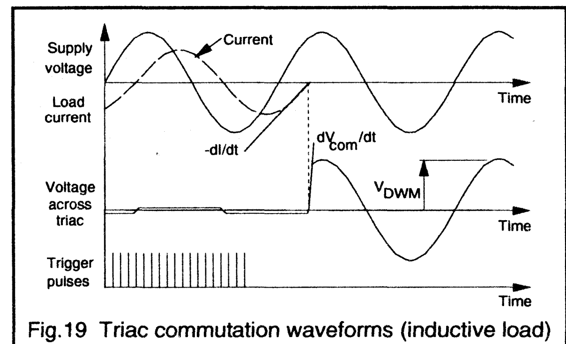


Fig.19 Triac commutation waveforms (inductive load)

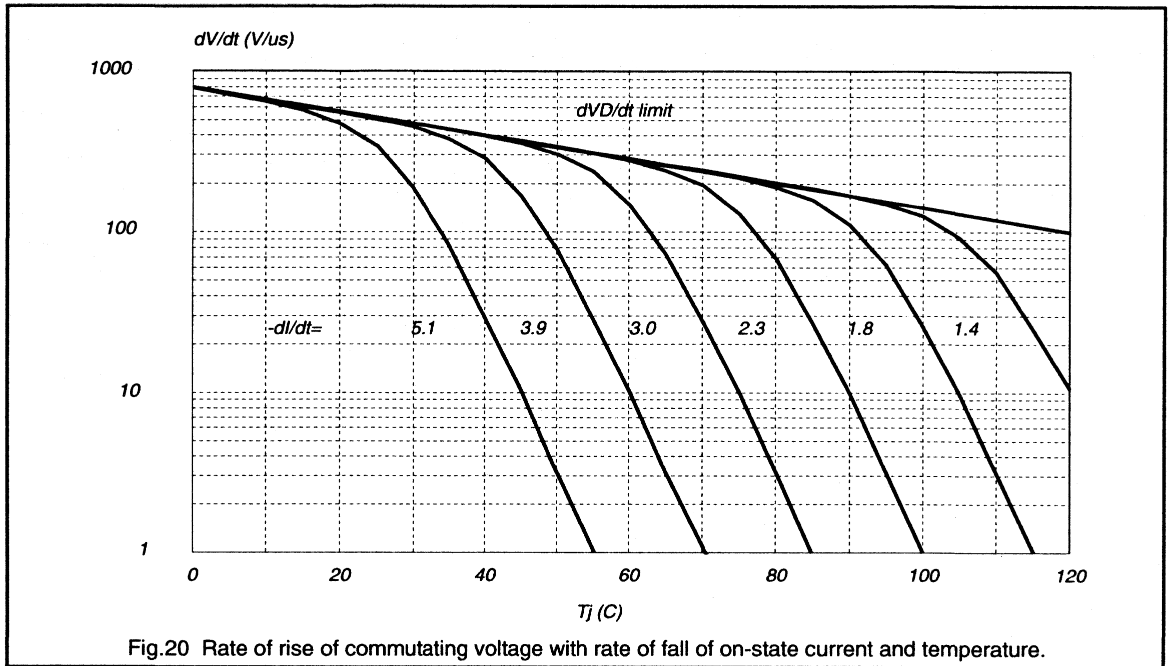


Fig.20 Rate of rise of commutating voltage with rate of fall of on-state current and temperature.

However, with an inductive load (Fig.19) the current lags behind the voltage and consequently commutation can present special difficulties. When the on-state current has fallen to zero after a triac has been conducting in one direction the supply voltage in the opposite direction will have already reached a significant value. The rate of fall of triac current will still be given by Equation 6 but the rate of rise of reapplied voltage, dV_{com}/dt will be very large. The triac may switch on immediately unless dV/dt is held less than that quoted in the published data by suitable circuit design.

The maximum rate of rise of commutating voltage which will not cause the device to trigger spuriously is an essential part of the triac published data. However, dV_{com}/dt is meaningless unless the conditions which are applicable are provided, particularly the rate of fall of on-state current $-dI_T/dt$. Our published data also contains graphs such as Fig.20 which relate dV_{com}/dt to junction temperature with $-dI_T/dt$ as a parameter. The characteristic dV_{com}/dt is specified under the worst probable conditions; namely:

-mounting base temperature, $T_{mb}=T_{mb(max)}$
-reapplied off-state voltage, $V_D=V_{DWM(max)}$
-rms current, $I_{T(RMS)} = I_{T(RMS)(max)}$.

In order that designers may economise their circuits as far as possible, we offer device selections with the same current ratings but with different values of dV_{com}/dt (at the same value of $-dI_T/dt$) for some of our triac families. The dV/dt capability can be traded off against the gate sensitivity ($I_{GT(max)}$) of the device. Sensitive gate triacs (i.e. those which require only a small amount of gate current to trigger the device) have less ability to withstand high values of dV_{com}/dt before sufficient current flows within the device to initiate turn-on. These different device selections are differentiated by suffices which are added to the device type number eg. BT137-600F.

Detailed design considerations for dV_{com}/dt limiting in inductive circuits when using triacs are considered in separate articles in this handbook.

Thyristor and Triac Applications

6.2.1 Triac control of DC inductive loads

The problem of inductive loads

This publication investigates the commutation problem encountered when triacs are used in phase control circuits with inductive loads. Commutation failure is likely to occur owing to circuit inductance imposing a sudden rise of voltage on the triac after conduction. Control of transformers supplying an inductively loaded bridge rectifier is particularly troublesome because of the added effect of rapid current decay during commutation. For a better understanding of the nature of the problem, the commutation behaviour is summarised here.

Triacs are bipolar power control elements that may turn on with either polarity of voltage applied between their main terminals. Unlike thyristors there is no circuit-imposed turn-off time. To ensure commutation the decay rate of current before turn-off and the rate of rise of reapplied voltage must both be held below specified limits. An excessive current decay rate has a profound effect on the maximum rate of rise of voltage that can be sustained, as then a large amount of stored charge is available to initiate the turn-on in the next half cycle.

Fig.1 shows the condition for a triac controlled transformer followed by a rectifier with inductive load. The load inductance forces the rectifier diodes into conduction whenever the instantaneous dc output voltage drops to zero. The transformer secondary is thus shorted for some time after the zero transitions of the mains voltage and a reverse voltage is applied to the triac, turning it off. Because of transformer leakage inductance the triac does not turn off immediately but continues to conduct over what is called the commutation interval. (see Fig.1)

During the commutation interval a high rate of decay of current (dI_{com}/dt) results for two reasons. Firstly the rate of fall of current is high because the leakage inductance of most transformers is low. This is necessary to achieve a small dc output voltage loss (represented by the shaded areas in the voltage waveform of Fig.1) in the transformer. Secondly, with an inductive rectifier load a substantial current flows when commutation starts to occur.

The large value of dI_{com}/dt results in a high rate of rise of voltage, dv/dt. Since the current decays rapidly the peak reverse recovery current I_{RRM} is fairly large. Upon turn-off I_{RRM} is abruptly transferred to the snubber elements R and C so the voltage abruptly rises to the level $R.I_{RRM}$ (C is initially discharged). Owing to the high value of both dI_{com}/dt and dv/dt loss of control follows unless measures are taken to prevent it.

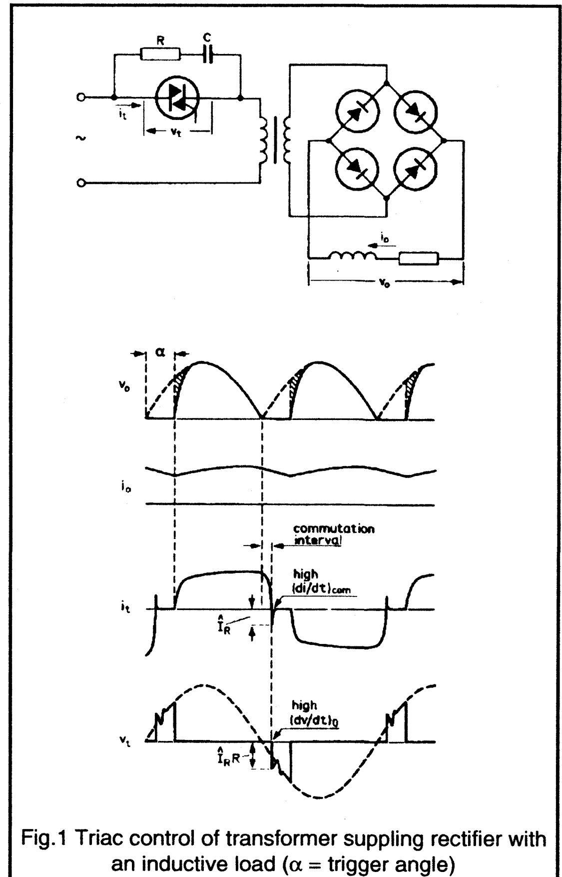


Fig.1 Triac control of transformer suppling rectifier with an inductive load (α = trigger angle)

Obtaining reliable commutation

A saturable choke in series with the transformer primary proves effective in achieving reliable commutation (Fig.2). Saturation should occur at a fraction of the rated load current so that the loss in the rectifier output voltage is minimised. At low currents the total inductance is large, thus softening the commutation and eliminating transients. The choke delays the rise in voltage so a quiescent period of a few tens of microseconds is introduced, during which time the triac can recover. There is usually no difficulty in designing a choke such that the decay rate of current (dI_{com}/dt) and the rate of rise of voltage (dv/dt) are sufficiently reduced to ensure reliable control.

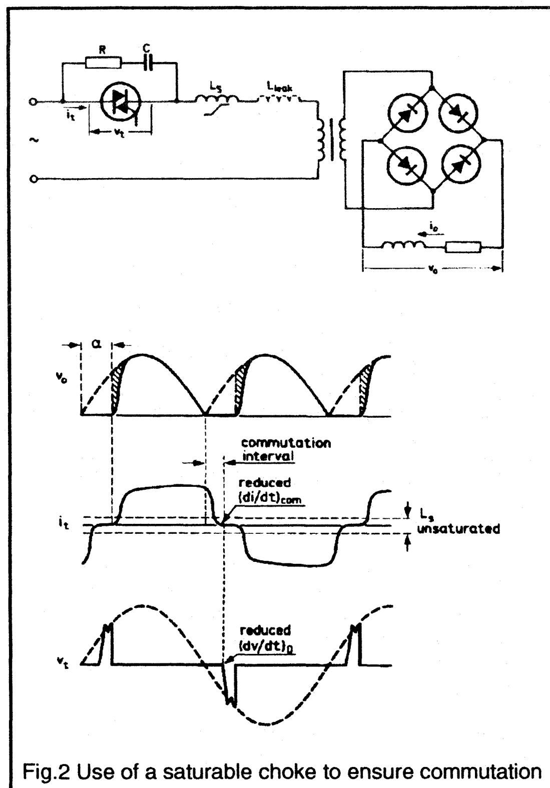


Fig.2 Use of a saturable choke to ensure commutation

Circuit analysis

Over the commutation interval the transformer secondary is shorted as the load inductance keeps the rectifier diodes in conduction, so the simplified diagram of Fig.3 applies. If the load time constant is much larger than the mains period then the load current can be assumed to be purely dc. The waveforms of triac voltage and current are given in Fig.4. The mains voltage is given by v_i= Vsinωt. As the commutation interval is a fraction of the ac period then the rate of change of voltage during the commutation interval can be assumed to be linear, giving:

$$v_i = -\hat{V}\omega t \quad (1)$$

Over the period 0 to t_2 the voltage across the saturable choke L_s and leakage inductance L_{leak} is equal to v_i (assuming the triac on-state voltage to be negligible). Assuming for this analysis that L_s remains in saturation (dashed portion in i_t waveform) then if L_{sat} is the saturated inductance, the following expression can be derived:

$$(L_{leak} + L_{sat}).di/dt = -\hat{V}\omega t \quad (2)$$

where *di/dt* is the rate of change of triac current.

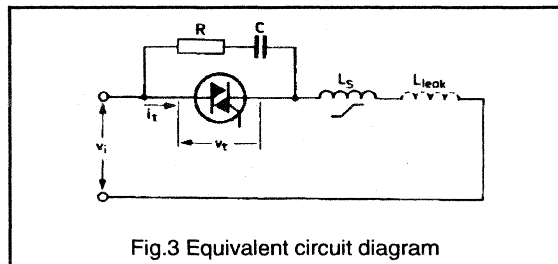


Fig.3 Equivalent circuit diagram

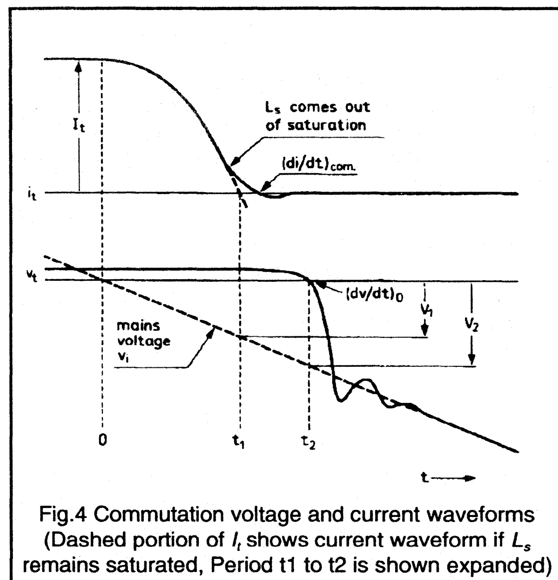


Fig.4 Commutation voltage and current waveforms (Dashed portion of I_t shows current waveform if L_s remains saturated, Period t1 to t2 is shown expanded)

Integrating equation (2) gives:

$$i_t = I_t - \frac{\hat{V}\omega t^2}{2(L_{leak} + L_{sat})} \quad (3)$$

where I_t is the current prior to commutation.

At time t_1, current i_t passes through zero, so, from (3):

$$t_1 = \sqrt{\frac{2I_t(L_{leak} + L_{sat})}{\hat{V}\omega}} \quad (4)$$

At t_1 the mains voltage has attained the value V_1 which is found by combining equations (1) and (4) to give:

$$V_1 = -\sqrt{2\omega\hat{V}I_t(L_{leak} + L_{sat})} \quad (5)$$

Choke L_s comes out of saturation at low current levels so the triac turn-off point is delayed to time t_2. Since in a practical circuit the delay is only of the order of 50µs, the mains voltage V_2 at the instant of turn-off is very nearly equal to V_1. Thus from equation 5:

$$V_2 \approx -\sqrt{2\omega\hat{V}I_t(L_{leak} + L_{sat})} \qquad (6)$$

The triac conducts until time t_2. Denoting the value of unsaturated inductance as L_{unsat}, the current decay rate at zero current is given by:

$$\frac{di_c}{dt} = \frac{V_2}{(L_{leak} + L_{unsat})}$$

$$= -\frac{\sqrt{2\omega\hat{V}I_t(L_{leak} + L_{sat})}}{L_{leak} + L_{unsat}} \qquad (7)$$

The initial rate of rise of off-state voltage, dv_{com}/dt, can now be derived. This parameter is decisive for the behaviour of the triac, since a much greater *dv/dt* can be sustained after carrier recombination, that is, when the off-state voltage has reached a substantial value.

At time t_2 the triac turns off but the voltage across it is still zero. The voltage drop across L_s and L_{leak} is equal to V_2 and the rate of rise of current carried by these inductances, di_L/dt, is given in equation (7). The rate of rise of triac voltage *dv/dt* is determined by di_L/dt and the values of the snubber components R and C.

$$\frac{dv}{dt} = R.\frac{di_L}{dt} + \frac{i}{C} \qquad (8)$$

When the interval t_1 to t_2 is long enough, the triac has fully recovered at time t_2, and so the current *i* to be taken over by the parallel RC snubber network is zero. At time t_2 *dv/dt* is equal to the initial rate of rise of voltage dv_0/dt. From equations (7) and (8):

$$\frac{dv_0}{dt} = \frac{R}{L_{leak} + L_{unsat}}\sqrt{2\omega\hat{V}I_t(L_{leak} + L_{sat})} \qquad (9)$$

In circuits where no transformer is interposed between the triac and rectifier then some series inductance is still needed to restrict turn-on di/dt. In that case Equations (7) and (9) are still valid by omitting L_{leak}.

Example - DC motor load

The motor control circuit of Fig.5 illustrates the use of the design method proposed in the previous section. Since the motor has a fairly high inductance it may be considered as a constant current source, giving a severe test condition for triac commutation.

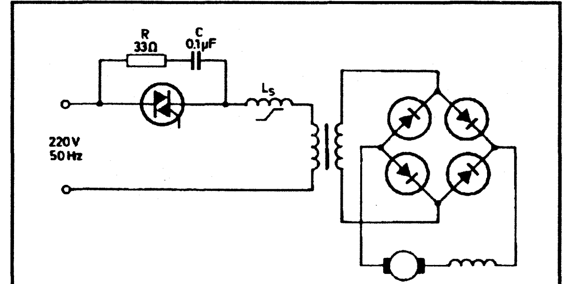


Fig.5 DC Motor test circuit.

Choke	L_{unsat}=2.25mH, 30 turns on 36x23x10mm³ toriod core
Transformer	220V/150V, 6kVA, 0.9mH leakage inductance
Motor	Series wound DC motor, Leakage inductance = 30mH

With L_{leak} = 0.9mH, L_{unsat} = 2.25mH and L_{sat}<<L_{leak} the circuit conditions can be calculated for a triac current of I_t = 20A and a 220V, 50Hz supply. Using equations (7) and (9) gives di_c/dt = -18.3A/ms and dv_0/dt = 0.6V/μs. These values can be compared with the commutation limits of the device to ensure that reliable commutation can be expected.

The inductance in the ac circuit also restricts turn-on di/dt which, for a continuous dc load current is:

$$\frac{di_{on}}{dt} \approx \frac{v_i}{t_{on}R} + \frac{v_i}{L_{leak} + L_{unsat}} \qquad (10)$$

where v_i is the instantaneous ac input voltage, t_{on} is the turn-on time of the triac and R is the snubber resistance. Maximum turn-on di/dt occurs at the peak value of input voltage, v_i. The initial rise of on-state current depends on the snubber discharge current through R as well as the limiting effect of the circuit inductance.

The oscillograms of Figs 6 to 10 illustrate circuit performance. With no choke added a large dv/dt was observed (Figs 6 and 7) and so consequently commutation failed when motor current was increased to around 9A. As seen from Figs 8 to 10 the choke softens commutation so that dependable control results even at 23A motor current. At this current (Fig.10) the quiescent interval is about 30μs, which is adequate time for the triac to recover.

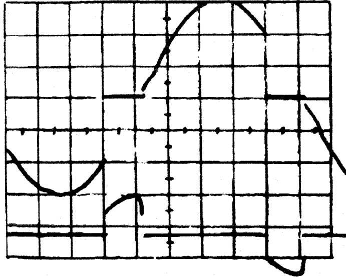


Fig.6 Triac voltage and current. No series choke.
7A motor current. Timebase: 2ms/div
Upper trace: Triac voltage, v_t (100V/div)
Lower trace: Triac current, i_t (5A/div)

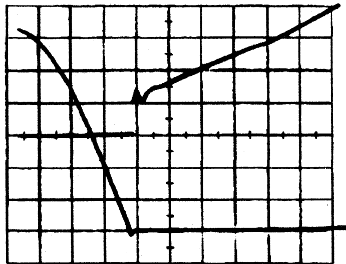


Fig.7 Triac voltage and current. No series choke.
7A motor current. N.B. Snap-off current
Timebase: 100µs/div
Upper trace: Triac voltage, v_t (20V/div)
Lower trace: Triac current, i_t (1A/div)

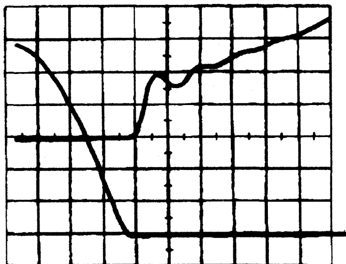


Fig.8 Triac voltage and current. Series choke added.
7A motor current. Timebase: 100µs/div
Upper trace: Triac voltage, v_t (20V/div)
Lower trace: Triac current, i_t (1A/div)

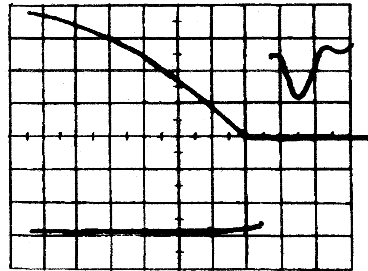


Fig.9 Triac voltage and current. Series choke added.
23A motor current. Timebase: 100µs/div
Upper trace: Triac voltage, v_t (10V/div)
Lower trace: Triac current, i_t (5A/div)

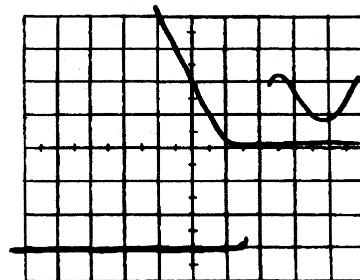


Fig.10 Triac voltage and current.Series choke added
23A motor current. N.B. slight reverse recovery current
Timebase: 50µs/div
Upper trace: Triac voltage, v_t (10V/div)
Lower trace: Triac current, i_t (1A/div)

6.2.2 Domestic Power Control With Triacs and Thyristors

The increasing demand for more sophisticated domestic products can, in part, be met by providing the user with some form of electronic power control. This control can be used, for example, to adjust the suction of a vacuum cleaner, the brightness of room lighting or the speed of food mixers and electric drills.

It may appear that the cost of this electronics would be high but this is not necessarily the case. With triacs and thyristors it is possible to produce high performance mains controllers which use only a few simple components. The following notes give details of some typical control circuits and highlight areas for special attention when adapting the designs for specific applications.

Vacuum cleaner suction control

The competitive nature of the vacuum cleaner market has led to the development of a wide variety of machine types and accessories. In many cases however, the speed of the motor remains constant and, if suction control is attempted, it consists merely of an adjustable vent in the air flow path. Electronic suction control sounds somewhat expensive and unnecessarily complicated for such an elementary application. In fact, by using a BT138 triac, a simple but nevertheless effective and reliable suction control circuit (Fig. 1) can be constructed very economically, and is suitable for all types of cleaner with a power consumption of up to 900W.

The heart of the circuit is the BT138. This is a glass passivated triac which can withstand high voltage bidirectional transients and has a very high thermal cycling performance . Furthermore its very low thermal impedance minimizes heatsink requirements.

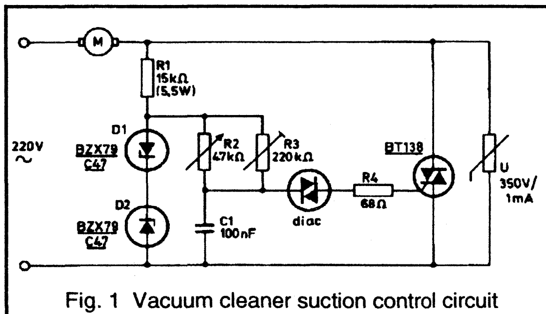
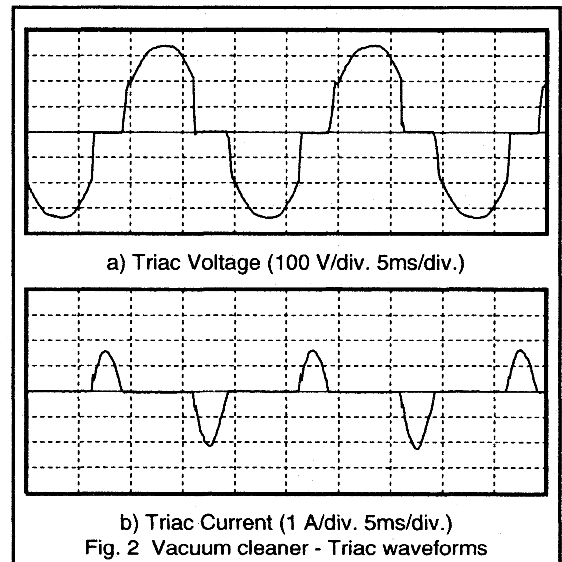


Fig. 1 Vacuum cleaner suction control circuit

Circuit Description

In Fig. 1 the BT138 is the power control element. Its action is controlled by a diac which is switched on by a charge on C_1 under the control of potentiometer R_2. The resistance of the diac is virtually infinite as long as the voltage across it remains within the breakover voltage limits, $-V_{BO}$ to $+V_{BO}$. During each half cycle of the mains sinewave, C_1 charges until the voltage across it exceeds the diac breakover voltage. The diac then switches on and C_1 discharges itself into the gate of the triac and switches it on. Diodes D_1 and D_2 stabilise the supply voltage to the charging circuit so that its operation is independent of mains voltage fluctuations. If $-V_{BO}$ and $+V_{BO}$ are equal and opposite, the triac will be triggered at the same time after the start of either a positive or negative half cycle. The conduction angle, and therefore the speed of the motor and the cleaner suction, is determined by the adjustment of R_2. Preset potentiometer R_3 is used to set the minimum suction level. The width and amplitude of the trigger pulses are kept constant by gate resistor R_4. The zinc oxide voltage dependent resistor (U) minimises the possibility of damage to the triac due to very high voltage transients that may be superimposed on the mains supply voltage. Figure 2 shows the current and voltage waveforms for the triac when the conduction angle is 30˚.



a) Triac Voltage (100 V/div. 5ms/div.)

b) Triac Current (1 A/div. 5ms/div.)

Fig. 2 Vacuum cleaner - Triac waveforms

Circuit Performance

A laboratory model of the circuit has been tested to determine the range of control that it has over the suction power of a typical vacuum cleaner. For the test, the cleaner was loaded with a water column. The result of the test is shown graphically in Fig. 3. The measured range of water column height (100 to 1100 mm) translates into a wide air flow range - from little more than a whisper to full suction.

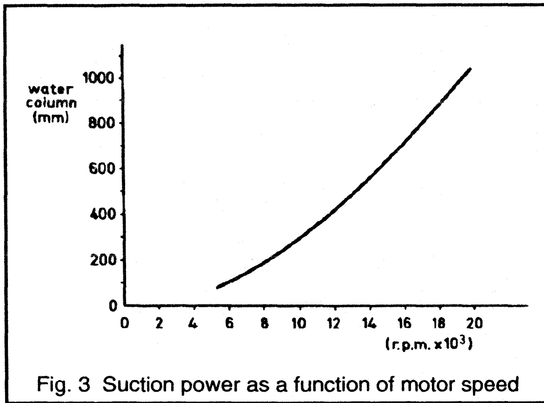


Fig. 3 Suction power as a function of motor speed

As suction power is a function of the speed of the vacuum cleaner motor, a second test was carried out to determine the range of motor speed control under conditions of minimum and maximum air flow (i.e. with the suction blocked and unrestricted). This test also checked the motor speed variation due to ±10% variation of a nominal 220 V AC mains supply. The initial test conditions were: unrestricted flow; mains supply 198 V (220 V - 10%); R_2 at maximum resistance, and R_3 set so that the motor just ran. Table 1 shows the results of the test. N_{min} is the speed at which the motor just runs and N_{max} is the speed of the motor with R_2 set at minimum resistance.

mains voltage (V)	blocked air flow N_{min} (rpm)	blocked air flow N_{max} (rpm)	unrestricted air flow N_{min} (rpm)	unrestricted air flow N_{max} (rpm)
198	5300	17100	4300	15400
220	6250	19000	5000	17100
242	7400	20000	6000	18200

Table 1 Motor speed figures for circuit of Fig. 1

The table shows that the speed setting range is wide. The ratio of N_{max} to N_{min} is 3.42:1, for 220 V mains and unrestricted airflow. The variation of motor speed due to variation of the mains input is quite small and represents a negligible change of suction. If D_1 and D_2 are omitted from the circuit, the speed setting ratio is reduced to 1.82:1 under the same conditions. The table also shows that the difference between the N_{min} for minimum and maximum air flow is quite small. This implies that speed stabilisation is unnecessary.

Special Design Considerations

The circuit shown in Fig. 1 has been shown to work well in a typical vacuum cleaner application. But motors and environments do vary, so some aspects of the design should be looked at carefully before it is finalised.

cycle number.	time (ms)	peak current (A)	rms current (A)	'limit' current (A)
1	20	49	22	24
2	40	41	18	21
3	60	35	13	19.5
4	80	32	14	18.5
5	100	29	13	18
10	200	20	9	15.5
20	400	14	6.3	14

Table 2 Currents during starting

Circuit positioning

The siting of the circuit, within the case of the cleaner, is particularly important. In some areas within the cleaner the temperature can be quite high. The circuit, and in particular the triac and its heatsink, should not be placed in one of these areas if the designer is to avoid problems keeping the temperature of the triac below T_{jmax}.

Starting current

Another factor that may lead to thermal problems is that of inrush current. The starting current of a vacuum cleaner motor is typically as shown in Fig. 4. The rms current during the first 20 ms could be 20 A or more. The current decays to its steady state value in about 1 s. To ensure that the triac does not overheat, reference should be made to the inrush current curves in the triac data sheet, the curve for the BT138 is reproduced in Fig. 5.

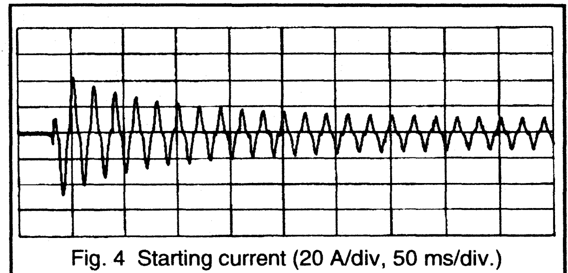


Fig. 4 Starting current (20 A/div, 50 ms/div.)

The first step in checking for a problem is to estimate the mounting base temperature, T_{mb}, prior to starting. A reasonable figure would be the worst case steady state value of T_{mb} during normal running.

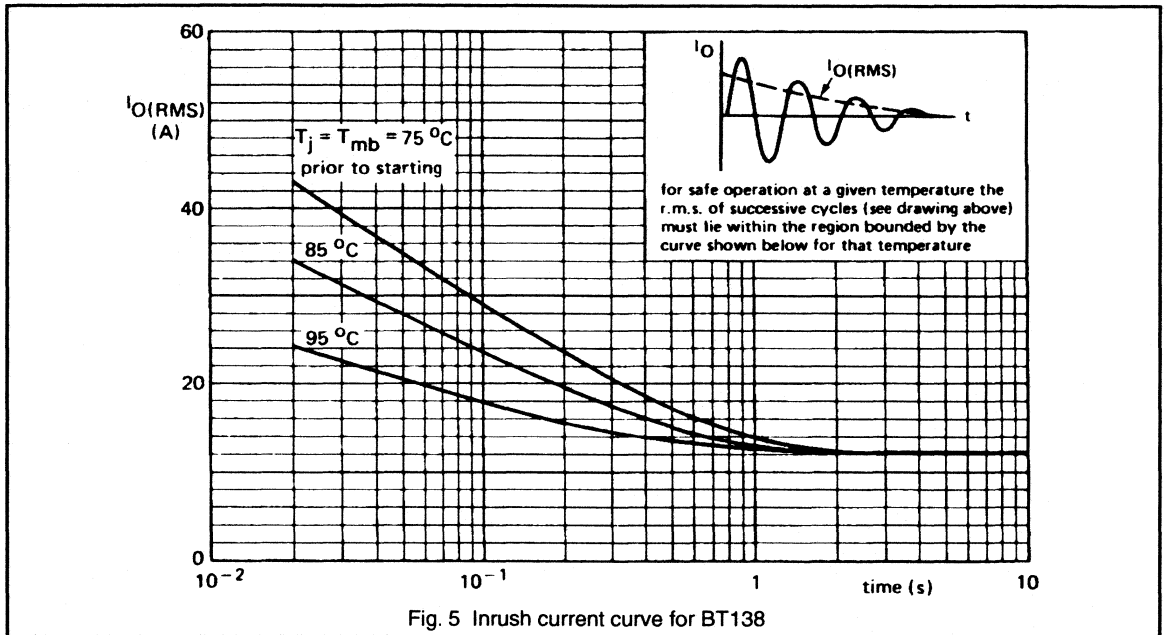


Fig. 5 Inrush current curve for BT138

Step 2 is to calculate the rms value of one cycle of the starting current at several times during start up and step 3 is to compare these figures with the values taken from the appropriate line of the inrush current curve.

As an example consider the performance of the BT138 driving a motor whose starting current is shown in Fig. 4. Direct measurement indicated that during normal running the T_{mb} of a BT138 mounted on a particular heatsink, would be no more than 22˚C above ambient. From other measurements it was estimated that the ambient temperature would not exceed 73˚C. These figures give a worst case steady state T_{mb} of 95˚C. It can be assumed that this is the highest temperature that the mounting base could be, prior to starting - a reasonable assumption which covers the case where the motor has been running for a long time, is turned off and then started again before there has been any cooling.

The rms values of cycles 1 to 5, 10 and 20 of the starting current are given in Table 2. Since the current is not an ideal sine wave these have been calculated from the peak current by assuming a crest factor (peak to rms) of 2.23. Also shown are the relevant $I_{O(RMS)}$ figures from the 95˚C line of Fig. 5. Since 'actual' inrush current is always less than the 'allowed' current it is safe to use the BT138 under the proposed conditions to control the motor. It should be noted that because the crest factor is $>\sqrt{2}$ the dissipation of the BT138 will be less than assumed by the inrush current curves of Fig. 5.

Commutation

The circuit shown in Fig. 1 has no RC snubber. This was because the values of dI/dt and dV/dt generated by the circuit were well within the capability of the BT138. This will often be the case with vacuum cleaner motors for two reasons:

- these motors introduce only a small phase shift in the current, so the voltage step is small and the dV/dt is low,
- the steady state value of the current is much less than the maximum rating of the BT138, this amounts to a dI/dt well within the capability of the BT138.

However care must be taken to ensure that this is true in all applications. In particular, care should be taken to ensure that the triac switches correctly even during starting. If a snubber is found to be necessary then a 100 Ω 0.5 W resistor in series with a 0.1µF capacitor will be more than adequate in most circumstances.

Interference

It is, of course, necessary to check that the overall equipment complies with local regulations for conducted and radiated interference. However, the measures taken to suppress the electrical 'noise' of the motor combined with the motor itself will often be more than sufficient to overcome the interference generated by the switching of the triac but this must be checked in all applications.

Domestic lamp dimmer

The use of light dimmers, once the prerogative of entertainment centres, has now become widespread in the home. It is necessary to ensure that the component parts of these units are simple and reliable so that they are compatible with the domestic environment.

The glass passivated BT138 triac meets these requirements. Firstly, it has a peak non-repetitive on-state current handling capability of up to 90 A which means it can easily withstand the inrush current that occurs when a cold lamp is switched on. It can also withstand high voltage bidirectional transients and a its low thermal impedance minimizes heatsink requirements.

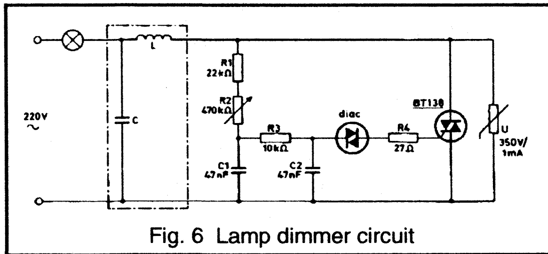


Fig. 6 Lamp dimmer circuit

Circuit Description

A simple circuit of a light dimmer using the BT138 is given in Fig. 6. The BT138 is the power control element, triggered via the diac. The setting of potentiometer R_2 determines the phase difference between the mains sine wave and the voltage across C_2. This in turn sets the triac triggering angle and the lamp intensity.

The resistance of the diac is very high as long as the voltage across it remains within its breakover voltage limits, $-V_{BO}$ to $+V_{BO}$. Each half cycle of the mains charges C_2 via R_1, R_2 and R_3 until the voltage being applied to the diac reaches one of its breakover levels. The diac then conducts and C_2 discharges into the gate of the triac, switching it on. If $-V_{BO}$ and $+V_{BO}$ are equal and opposite, the triac will be triggered at the same time after the start of either a positive or negative half cycle. If C_1 were not included in the circuit, the voltage across C_2 would change abruptly after triggering and cause the phase relationship between the mains voltage and voltage across C_2 to progressively alter. This would cause an undesirable hysteresis effect. The voltage across C_1 partially restores the voltage across C_2 after triggering and thereby minimizes the hysteresis effect. The width and amplitude of the trigger pulses are kept constant by gate resistor R_4. The VDR minimizes the possibility of the triac being damaged by high voltage transients that may be superimposed on the mains supply voltage.

Special Design Considerations

Circuit rating

The BT138 has an rms current rating of 12 A, it is, therefore, capable of controlling loads with a rating of 2 kW or more. However, the load of this circuit must be restricted to a much lower level. There are two reasons for this. The first is to keep mains distortion within the allowed limits, without the necessity of expensive filter networks. The second reason is to limit dissipation. If, as is likely, the circuit is to be mounted in the wall in place of a conventional switch, then air circulation is going to be very restricted and the ambient temperature around the circuit will be quite high. It is important, for reliability reasons to ensure that the temperature of the BT138 never exceeds T_{jmax}, so the dissipation of the triac must be kept to a low level.

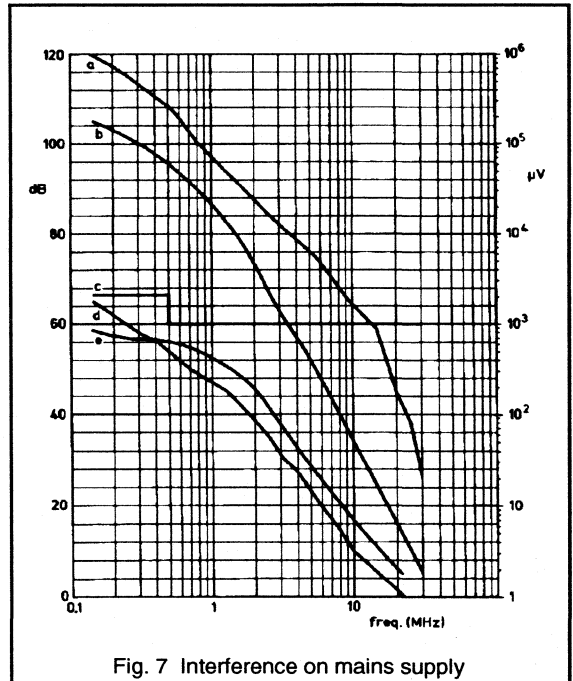


Fig. 7 Interference on mains supply

Interference

Regulations concerning conducted and radiated interference vary considerably form country to country but it is likely that some form of filter will be needed. The simple LC filter shown within the dashed-lined box in Fig. 6 is often all that is needed. The values of the filter components will vary, but a combination of 0.15 μF capacitor and a low Q inductor of 2.5 μH was found to be sufficient for the circuit to meet the C.I.S.P.R. limits. This is illustrated by the plots shown in Fig. 7. Curves (a) and (b) show the level of noise

on the mains supply for the circuit, without filter, when controlling 550 W and 25 W loads respectively. Curves (d) and (e) are for the circuit with filter connected showing that the C.I.S.P.R. limit, which is curve (c), has been met.

Filter inductor

Having selected the value of filter inductor, the designer has then to decide how to make it. Construction will not be too critical - it is not necessary to achieve a high Q - and there will be considerable room for reducing its size. However, care must be taken to ensure that the inductor does not saturate when the inrush current, of a cold lamp, flows through it. If the inductor does saturate then the filter capacitor will, effectively, be shorted out by the triac. In this case the triac current could rise faster than the dI/dt rating allows. This could cause progressive damage to the triac resulting in premature failure.

Speed control for food mixers and electric drills

Food mixers and electric hand drills are products whose usability is improved by the addition of electronic speed control. But they are products where costs have to be tightly controlled so the choice of circuit is very important. This decision is made harder by the need to have a good speed regulation under the widely varying loads that these products are subjected to.

The circuits to be described provide continuous control of motor speed over a wide speed range by adjusting the conduction angle of a BT151 thyristor. They compensate for load variation by adjusting the firing angle when there is a change in the motor speed - as indicated by a change in its remnant back EMF.

Back EMF Feedback Circuits

A simple motor speed control circuit that employs back EMF to compensate for changes in motor load and mains voltage is shown in Fig. 8(a). The resistor chain R_1, R_2,R_3 and diode D_1 provide a positive going reference potential to the thyristor gate via diode D_2. Diode D_1 is used to reduce the dissipation in the resistor chain by some 50% and diode D_2 isolates the trigger circuit with the thyristor in the on-state. When the thyristor is not conducting the motor produces a back EMF voltage across the armature proportional to residual flux and motor speed. This appears as a positive potential at the thyristor cathode.

A thyristor fires when its gate potential is greater than cathode potential by some fixed amount. Depending on the waveform shape and amplitude at the gate, the circuit may function in several modes.

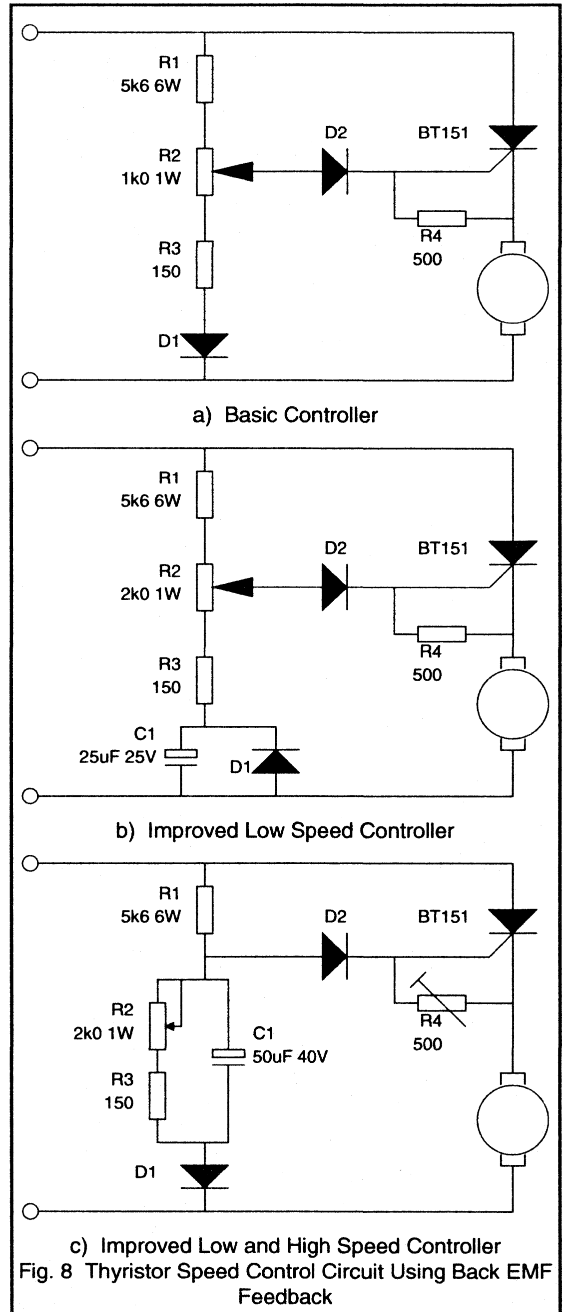


Fig. 8 Thyristor Speed Control Circuit Using Back EMF Feedback

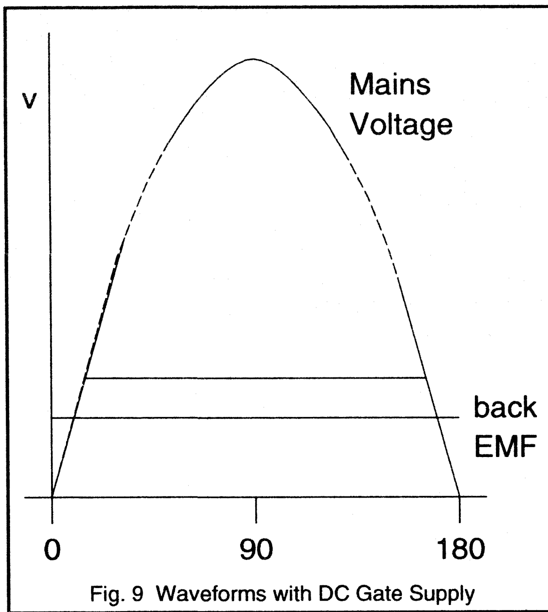


Fig. 9 Waveforms with DC Gate Supply

If, for example, during positive half cycles a constant DC potential was applied at the gate, see Fig. 9, the thyristor would continue to fire at the beginning of each cycle until the back EMF was large enough to prevent firing. Thyristor firing would then continue intermittently at the beginning of the positive cycles to maintain some average motor speed.

Referring to Fig. 8(a) the waveform appearing at the thyristor gate will approximate to a half sine wave, Fig. 10(a). As a result it is impossible for the firing angle to be later than 90˚ - the most positive value of the trigger potential. At lower motor speeds the firing angle might need to be 130˚ for smooth operation. If the maximum firing angle is limited to 90˚ then intermittent firing and roughness of motor operation will result.

If, however, the waveform at the gate has a positive slope value to an angle of at least 130˚ then it will be possible to have a stable firing point at low speeds. Such a waveform can be produced if there is some phase shift the in the trigger network.

Stable Firing at Small Conduction Angles

The trigger network of the circuit shown in Fig. 8(b) has been modified by the addition of a capacitor C_1 and diode D_1. The diode clamps the capacitor potential at zero during the negative going half cycles of the mains input. The waveform developed across the capacitor has a positive slope to some 140˚, allowing thyristor triggering to be delayed to this point.

a) Basic Controller

b) Improved Low Speed Controller

c) Improved Low and High Speed Controller

Fig. 10 Gate Voltage Waveforms

As the slider of R_2 is moved towards R_1 the peak of the waveform at the gate will move towards 90˚, as shown in Fig. 10(b). As the speed increases the no load firing angle will also advance by a similar amount so stability will be maintained. This circuit will give smoother and more stable performance than the circuit of Fig. 8(a). It will, however, give a marginally greater speed drop for a given motor loading at low speed settings. At the maximum speed settings the circuit of Fig. 8(a) approximates to that of Fig. 8(b).

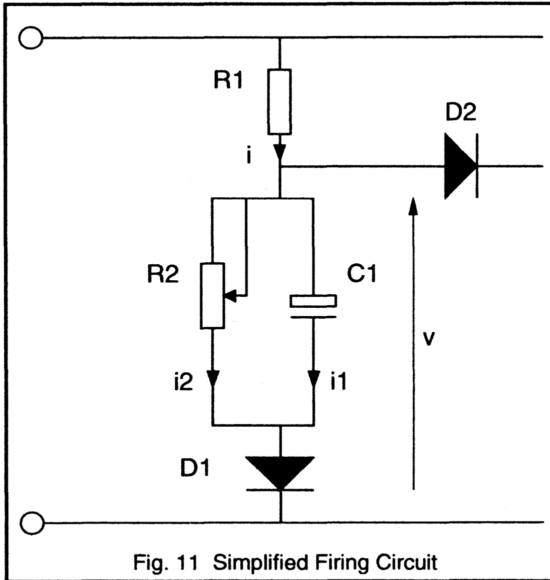


Fig. 11 Simplified Firing Circuit

Improved Motor Performance With Stable Firing

Both the circuits so far discussed have gate voltage waveforms that are of near linear slope from the zero point of each positive half cycle, see Figs. 10(a) and (b). This means that the only time that the thyristor can be fired early in the mains cycle, say at 20˚, is when the back EMF and hence motor speed is very low. This effect tends to prevent smooth running at high speeds and high loads.

Stable triggering, at low angles, can be achieved if the gate voltage ramp starts each cycle at a small positive level. This means that the time to reach the minimum trigger voltage is reduced. The circuit of Fig. 8(c) is one way of achieving this. In this circuit capacitor C_1 is charged during positive half cycles via resistor R_1 and diode D_1. During negative half cycles the only discharge path for capacitor C_1 is via resistors R_2 and R_3.

Diode D_1 also prevents C_1 from being discharged as the thyristor switches off by the inductively generated pulse from the motor. As the value of resistor R_2 is increased capacitor C_1 is discharged less during negative half cycles, but its charging waveform remains substantially unchanged. Hence the result of varying R_2 is to shift the DC level of the ramp waveform produced across C_1.

Diode D_2 isolates the triggering circuit when the thyristor is ON. Resistor R_4 adjusts minimum speed, and by bleeding, effectively, a constant current, in conjunction with the gate current from the triggering circuit, enables resistor R_2 to give consistent speed settings.

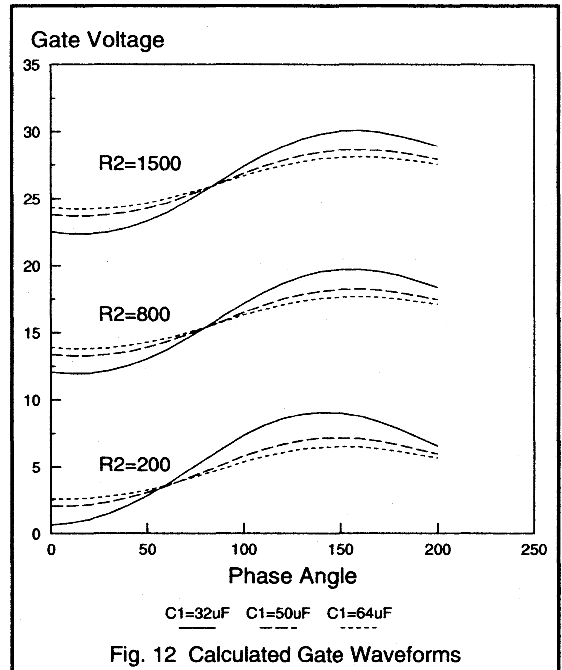


Fig. 12 Calculated Gate Waveforms

Circuit Design

If the speed controller is to be effective it must have stable thyristor firing angles at all speeds, and give the best possible speed regulation with variations of motor load. The circuit of Fig. 8(c) gives a motor performance that satisfies both of the above requirements.

There are two factors that are important in the circuit operation in order to obtain the above requirements.

- The value of positive slope of the waveform appearing at the thyristor gate.
- The phase angle at which the positive peak gate voltage is reached during a positive half cycle of mains input.

As previously described the charging of capacitor C_1 by resistor R_1 determines the rate of rise of voltage at the thyristor gate during the positive half cycle. However, resistor R_1 must also have a value such that several times the maximum thyristor gate current passes through the RC network to D_1. This current will then give consistent speed settings with the spread of thyristor gate currents when the minimum speed is set by resistor R_4.

The positive slope value of the thyristor gate voltage will have to be fixed according to the motor used. A motor that gives a smooth back EMF voltage will allow a low slope value to be used, giving good torque speed characteristics. Some motors have coarser back EMF waveforms, with voltage undulations and spikes, and a steeper slope of thyristor gate voltage must be used in order to obtain stable motor operation. The value of capacitor C_1 is chosen to provide the required positive slope of the thyristor gate voltage.

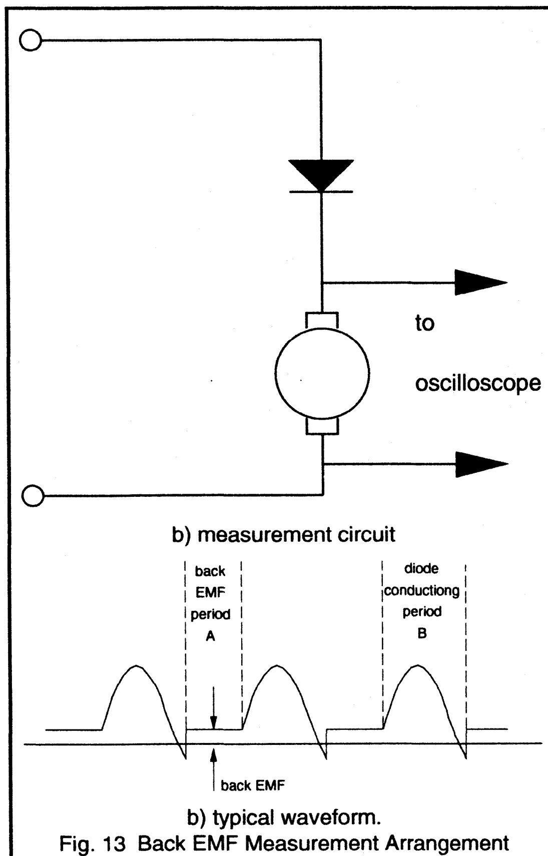


Fig. 13 Back EMF Measurement Arrangement

Some calculations have been made on the circuit of Fig. 8(c) simplified to the form of Fig. 11, where it is assumed that current flowing to the thyristor gate is small compared with the current flowing through resistor R_1. An expression has been derived for the voltage that would appear at the anode of D_2 in terms of R_1, R_2 and C_1 and is given later. Component values have been substituted into the expression to give the thyristor gate waveforms shown in Fig. 12.

In order to adjust the circuit to suit a given motor, the remnant back EMF of the motor must be known. This may be measured using the arrangement shown in Fig. 13. The voltage appearing across the motor is measured during the period when the series diode is not conducting (period A). The voltage so obtained will be the motor back EMF at its top speed on half wave operation, and corresponds to the back EMF that would be obtained from the unloaded motor at its highest speed when thyristor controlled. In practice, since the mains input is a sine wave, there is little increase in the 'no load' speed when the firing angle is reduced to less than about 70˚.

The value of resistor R_2 in Fig. 8(c) determines the motor 'no load' speed setting. The waveforms of Fig. 12 may be used as a guide to obtaining the value of this resistor. It must be chosen so that at 70˚ and at its highest value, the gate voltage is higher than the measured back EMF by about 2 V - the forward gate/cathode voltage of the thyristor.

The thyristor is turned ON when a trigger waveform, shown in Fig. 12, exceeds the back EMF by the gate/cathode voltage. So, if the back EMF varies within a cycle then there will be a cycle to cycle variation in the firing angle. Normally, random variations of the firing angle by 20˚ are tolerable. If, for example, there were variations in the back EMF of 1 V, then with a firing angle of 70˚and a capacitor of 32 µF, the variation of firing angle would be about 12˚. With capacitor values of 50 µF and 64 µF the firing angles variations would be 19˚ and 25˚ respectively. Therefore, a capacitor value of 50 µF would be suitable.

Performance

The torque speed characteristics of the three circuits, when used to drive an electric drill, are compared in Fig. 14. It may be seen that the circuit of Fig. 8(b) has a poorer performance than the two other circuits. That of Fig. 8(c) may be seen to give a similar performance to the circuit of Fig. 8(a) at low speeds but, at high speeds and torques, it is better. It should be noted that the circuits of Figs. 8(b) and (c) provide low speed operation free from the intermittent firing and noise of the Fig. 8(a) circuit. Figure 15 compares the circuits of Fig. 8(a) and 8(c) when the load is a food mixer motor.

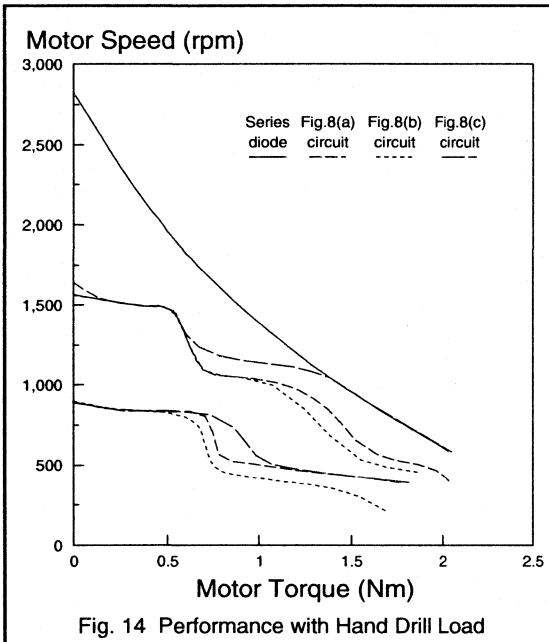


Fig. 14 Performance with Hand Drill Load

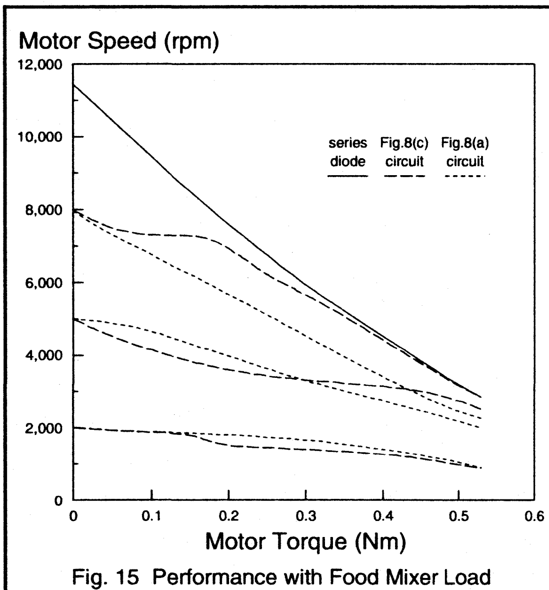


Fig. 15 Performance with Food Mixer Load

Circuit Calculations

The following analysis derives an expression for voltage 'v' at the anode of D_2. This expression can be used to produce the gate voltage waveforms shown in Fig. 12. The analysis assumes that the current drawn by the thyristor gate is negligible in comparison with the current flowing in R_1.

The charging current i_1 for capacitor C_1 in Fig. 11, is given by:

$$i_1 = \frac{dq}{dt} = C_1\frac{dv}{dt}$$

and

$$i_2 = \frac{v}{R_2}$$

Representing a mains half sine wave by $f(E)$ where E is the peak mains voltage.

$$i = \frac{f(E) - v}{R_1} = i_1 + i_2$$

therfore

$$\frac{f(E) - v}{R_1} = C_1\frac{dv}{dt} + \frac{v}{R_2}$$

where i, i_1, i_2 are instantaneous currents.

Simplifying:-

$$C_1\frac{dv}{dt} + v\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{f(E)}{R_1}$$

Fourier analysis of a half sinewave gives:-

$$f(E) = E\left\{\frac{1}{\pi} + \frac{1}{2}\sin(\theta) - \frac{2}{\pi}\sum_{n=2,4,6...}^{n=0}\frac{\cos(n\theta)}{n^2 - 1}\right\}$$

neglecting terms of the Fourier series with n > 2, then

$$C_1\frac{dv}{dt} + v\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{E}{R_1}\left\{\frac{1}{\pi} + \frac{1}{2}\sin(\omega t) - \frac{2}{3\pi}\cos(2\omega t)\right\}$$

then

$$C_1\frac{dv}{dt} + v\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{E}{R_1\pi} = \frac{E}{R_1}\left\{\frac{1}{2}\sin(\omega t) - \frac{2}{3\pi}\cos(2\omega t)\right\} \qquad (1)$$

simplifies to

$$A\frac{dv}{dt} + Bv - D = X\sin(\omega t) - Y\cos(2\omega t) \qquad (2)$$

where A, B, D, X, Y are constants.

Put

$$v = a\sin(\omega t) + b\cos(\omega t) + c\sin(2\omega t) + d\cos(2\omega t) + \frac{D}{B} \qquad (3)$$

where a, b, c, d are constants.

$$\frac{dv}{dt} = a\omega\cos(\omega t) - b\omega\sin(\omega t)$$

$$+2c\omega\cos(2\omega t) - 2d\omega\sin(2\omega t) \qquad (4)$$

substituting (3) and (4) in equation (2) and equating terms in $\cos(\omega t), \cos(2\omega t), \sin(\omega t), \sin(2\omega t)$, then

$$v = \frac{BX}{A^2\omega^2 + B^2}.\sin(\omega t) - \frac{A\omega X}{A^2\omega^2 + B^2}.\cos(\omega t)$$

$$-\frac{2A\omega Y}{4A^2\omega^2 + B^2}.\sin(2\omega t)$$

$$-\frac{BY}{4A^2\omega^2 + B^2}.\cos(2\omega t) + \frac{D}{B}$$

substituting for the constants in equation (2) gives:

$$v = R_2E.\frac{(R_1+R_2)\sin(\omega t) - \omega C_1R_1R_2\cos(\omega t)}{2\omega^2C_1^2R_1^2R_2^2 + (R_1+R_2)^2}$$

$$+R_2E.\frac{1}{\pi(R_1+R_2)}$$

$$-R_2E.\frac{4\omega C_1R_1R_2\sin(2\omega t) + 4(R_1+R_2)\cos(2\omega t)}{3\pi[4\omega^2C_1^2R_1^2R_2^2 + (R_1+R_2)^2]}$$

This may be simplified since

$$(R_1+R_2)^2 \ll 2\omega^2C^2R_1^2R_2^2$$

So the voltage that the trigger circuit would apply to the gate (assuming the gate draws no current) is given by:

$$v = \frac{R_2E}{\pi(R_1+R_2)}$$

$$+\frac{R_2E}{2\omega^2C_1^2R_1^2R_2^2}\{(R_1+R_2)\sin(\omega t)$$

$$-\omega C_1R_1R_2\cos(\omega t)$$

$$-\frac{2}{3\pi}\omega C_1R_1R_2\sin(2\omega t)$$

$$-\frac{1}{3\pi}(R_1+R_2)\cos(2\omega t)\}$$

Solving this equation for a different values of C_1 and positions of R_2 gives the curves shown in Fig. 12.

Conclusions

The addition of electronic control can enhance the overall usability of many domestic products. Cost and performance requirements are major factors when determining the type of control circuit to be used in these applications. It is possible, using thyristors and triacs, to construct a range of phase control circuits which can meet many of these cost and operational requirements.

Although these circuits are not complex and use only simple components, it is still important to design with care to ensure that the best performance is achieved. This report has given examples of some of these circuits and has highlighted the areas of their design requiring particular care.

6.2.3 Design of a Time-proportional temperature controller

Electronic temperature control is no longer new: phase and on/off controls for heaters have been widely used to replace mechanical switches. However, both phase control and on/off control have disadvantages. Conventional phase control allows fully-proportional control of the power dissipated in the load, but the high rates of change of current and voltage cause RFI and transients on the mains supply. Because of this effect, phase control is not allowed to be used for domestic heaters. Simple on/off control with zero-voltage switching avoids generation of RFI but the amount of hysteresis required to prevent temperature oscillations does not give the required control accuracy.

The principle of time-proportional control

Time proportional control combines the zero-voltage switching of on/off control with the accuracy of proportional control and so eliminates the disadvantages of these two alternative systems. Time-proportional control regulates the load power such that there will be no overshoot or undershoot of the desired temperature as is the case with normal on/off systems. The TDA1023 has been designed to provide time-proportional control for room heaters and electric heating elements using a minimum number of external components. It incorporates additional features to provide fail-safe operation and fine control of the temperature.

There are three states of operation when using time-proportional control:

- load switched fully off,
- load power proportional to the difference between actual and desired temperatures,
- load switched fully on.

Figure 1 illustrates the principle; the load is switched on once and off once in a fixed repetition period, the ratio of the on and off periods providing the proportional control. This method of control can cause mains flicker; the mains voltage changes slightly each time the load is switched on or off.

CENELEC, the European Committee for Electro-technical Standardisation, has published rules which limit the rate at which domestic heating apparatus may be switched on and off. Table 1 gives the minimum repetition period for a range of load powers and common mains voltages from CENELEC publication EN50.006.

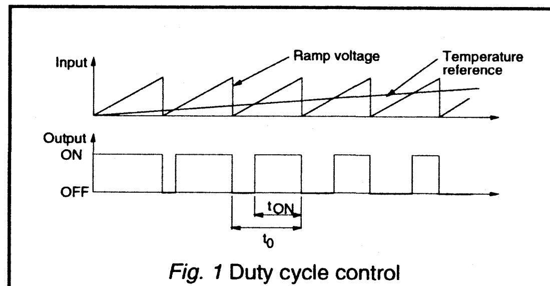


Fig. 1 Duty cycle control

Appliance Power (W)	Repetition period, t_o (s) 220V	240V	380V
600	0.2	0.2	
800	0.8	0.3	0.1
1000	2.0	1.0	0.2
1200	4.6	2.0	0.2
1400	7.0	4.3	0.2
1600	10.0	6.3	0.3
1800	16.0	8.9	0.5
2000	24.0	13.0	0.9
2200	32.0	17.0	1.3
2400	40.0	24.0	1.9
2600		31.0	2.6
2800			3.6

Table 1 CENLEC minimum repetition periods for Domestic Heater Applications

Description of the TDA1023

The TDA1023 is a 16-pin dual in-line integrated circuit designed to provide time-proportional power control of electrical heating elements. The TDA1023 is ideally suited for the control of:

- Panel heaters
- Cooker elements
- Electric irons
- Water heaters
- Industrial applications, e.g. temperature controlled oil baths, air conditioners.

The TDA1023 Incorporates the following functions:

- A stabilised power supply. The TDA1023 may be connected directly to the AC mains using either a dropping resistor or capacitor. It provides a stabilised reference voltage for the temperature-sensing network.

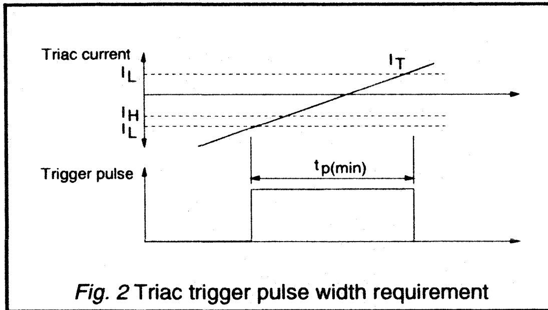


Fig. 2 Triac trigger pulse width requirement

- A zero-crossing detector to synchronise the output trigger pulses to the zero-crossings of the mains supply. The detector produces a pulse, the duration of which is determined by an external resistor, centred on the zero-crossing of the mains voltage.

- A comparator with adjustable hysteresis, preventing spurious triggering of the output. This compares a thermistor voltage, a function of the room temperature, with the voltage from the temperature selection dial.

- A voltage translation circuit for the potentiometer input. Normally, the relatively small temperature variation in a room (5˚C to 30˚C) corresponds to a narrow angle of rotation of a potentiometer shaft. Use of this circuit doubles the angle of rotation of the potentiometer shaft for the same temperature range.

- A sensor fail-safe circuit to prevent triggering if the thermistor input becomes open or short-circuited.

- A timing generator with an adjustable proportional band. This allows a full 100% control of the load current over a temperature range of only 1˚C or 5˚C. The repetition period of the timing generator may be set by an external capacitor to conform to the CENELEC specifications for mains load switching.

- An output amplifier with a current-limited output. The amplifier has an output current capability of at least 200mA and is stabilised to 10V while the current limit is not exceeded.

- Input buffers, to isolate the voltage translation circuit and comparator from external influences.

- A control gate circuit to activate the output if there is a mains zero-crossing, the comparator is ON and the fail-safe comparator is OFF.

Although designed specifically for time proportional control, the TDA1023 is also suitable for applications requiring on/off control if the timing generator is not used.

Required Duration of Triac Trigger Pulse

The main advantage of triggering at the instant when the applied voltage passes through zero is that this mode of operation renders the use of RF suppression components unnecessary. For time-proportional control, continuous conduction of the triac may be required for many cycles of the mains supply. To maintain conduction while the load current is approaching the zero-crossing, the trigger pulse must last from the time when the load current falls to the value of the triac holding current (I_H), until the time when the load current reaches the triac latching current (I_L).

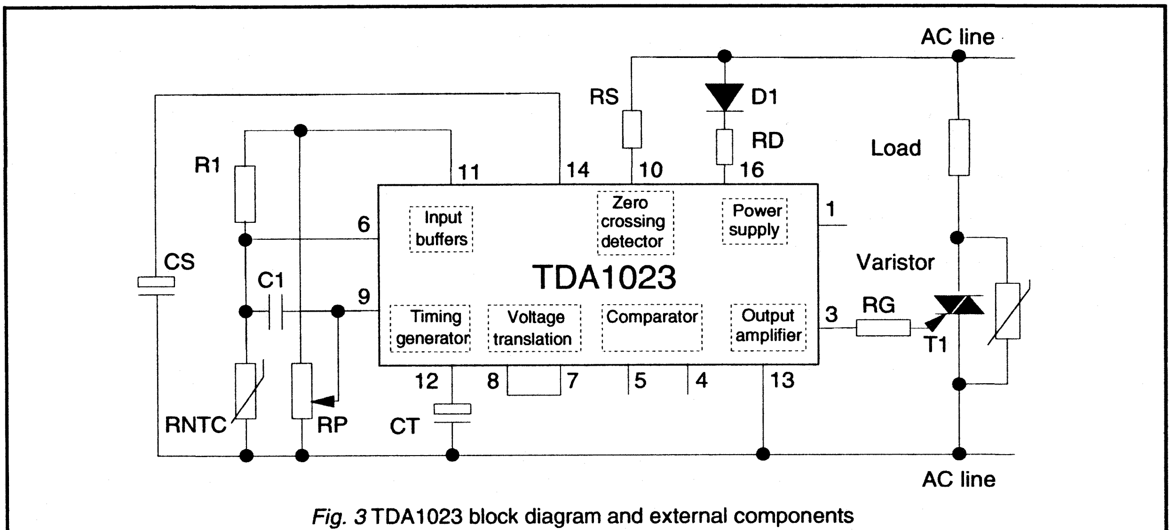


Fig. 3 TDA1023 block diagram and external components

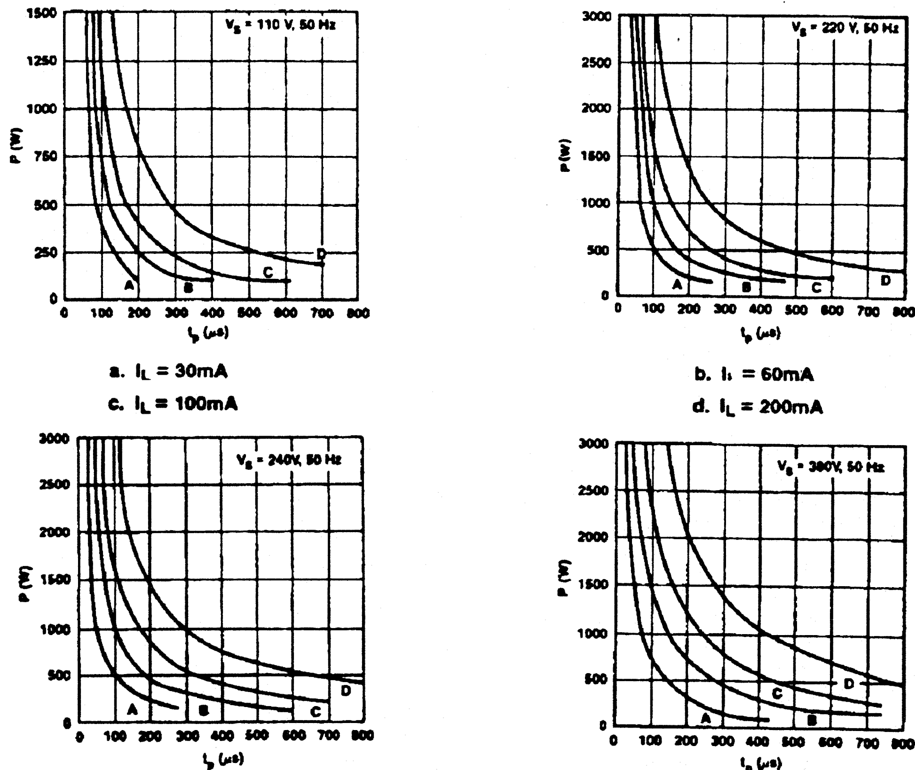


Fig. 4 Minimum pulse width as a function of supply voltage and latching current

In general, the latching current of a triac is higher than the holding current, so the minimum trigger pulse duration may be taken as twice the time for the load current in the triac (I_T) to rise from zero to the triacs latching current, see Fig. 2. The current passed by the triac is a function of its on-state voltage, the load resistance, and the applied voltage. The trigger pulse width is therefore a function of:

- triac latching current (I_L)
- applied AC voltage ($v = V\sin\omega t$)
- load resistance (R)
- on-state voltage of the triac (V_T) at I_L.

The load resistance is related to the nominal load power, P and nominal supply voltage, V_s by $R=V_s^2/P$. Assuming that the load resistance has a tolerance of 5% and the AC voltage variation is 10%, the minimum required width of the trigger pulse in the worst case can be calculated. The graphs of Fig. 4 show $t_{p(MIN)}$ as a function of P for four common mains voltages with values of 30mA, 60mA, 100mA, and 200mA for the triac latching current I_L and a maximum on-state voltage of V_T=1.2V at I_L.

Selection of external components

The external components required by the TDA1023 determine the operation of the device. The following paragraphs describe the selection of these components to ensure reliable operation under worst-case conditions.

Synchronisation Resistor, R_S

A current comparator is used as a zero-crossing detector to provide trigger pulse synchronisation. It compares the current through the synchronisation resistor (R_S) with a reference current. As the supply voltage passes through

zero the current in the synchronisation resistor becomes less than the reference current and a trigger pulse is given until the current in R_S increases above the reference level.

Thus, the duration of the trigger pulse depends upon the rate of change of current in R_S at the supply voltage zero-crossing point. This rate of change is affected by:

- -the AC supply voltage
- the supply frequency
- the value of the synchronisation resistor.

Fig. 5 shows the value of R_S as a function of trigger pulse width, with the AC supply voltage as a parameter.

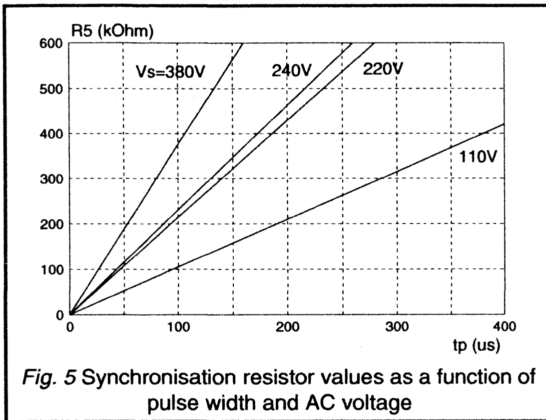


Fig. 5 Synchronisation resistor values as a function of pulse width and AC voltage

Gate Resistor R_G

The guaranteed minimum amplitude of the output trigger pulse of the TDA1023 is specified as 10V at an output current less than 200mA. The output stage is protected against damage due to short-circuits by current-limiting action when the current rises above 200mA.

Although the output is current-limited, it is still advantageous to include a gate series resistor in the circuit. Inclusion of a gate resistor to limit the gate current to the minimum value required reduces the overall current consumption and the power dissipation in the mains dropping resistor. Furthermore, the point at which current limiting occurs is subject to considerable variation between samples of the TDA1023: a gate resistor will reduce the effect of this in production circuits.

The rectangular output V/I characteristic of the TDA1023 is shown in Fig. 6. Load lines for various values of gate resistor have been plotted on this diagram so that the maximum value of gate resistor can be selected by plotting horizontal and vertical lines to represent the required minimum gate current and voltage. The following example illustrates the use of Fig. 6.

The triac to be triggered is a Philips BT139. At 0˚C the trigger pulse requirements for a standard BT139 are:

I_{GT} = 98 mA
V_{GT} = 1.6 V

These figures are for triggering with a positive gate pulse when MT_2 is negative with respect to MT_1. The lines representing V_{GT}= 1.6V and I_{GT}=98 mA cross the load line for a gate resistor value of 82 Ω. The maximum value of gate resistor is therefore 82 Ω.

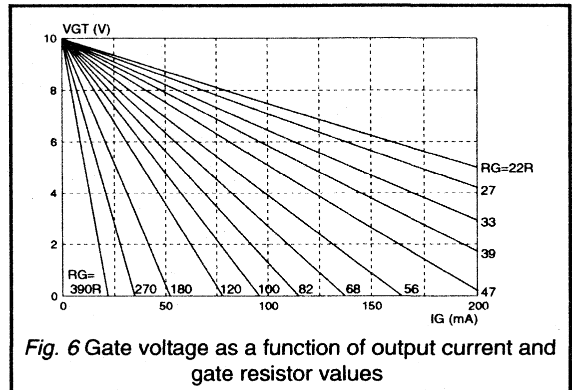


Fig. 6 Gate voltage as a function of output current and gate resistor values

Gate Termination Resistor R_{PD}

The TDA1023 has a resistor approximately 1.5kΩ between Pin 1 and Pin 13. This is intended for use as a pull-down resistor when sensitive triacs are being used.

The Proportional Band Resistor R_5

The proportional band is the input voltage range that provides control of 0% to 100% of the load power. The TDA1023 has a built-in proportional band of V_{pb}=80mV (corresponding to about 1˚C) which can be increased by the addition of resistor R_5 between Pin 5 and ground. The maximum proportional band of 400mV is obtained by shorting Pin 5 to ground.

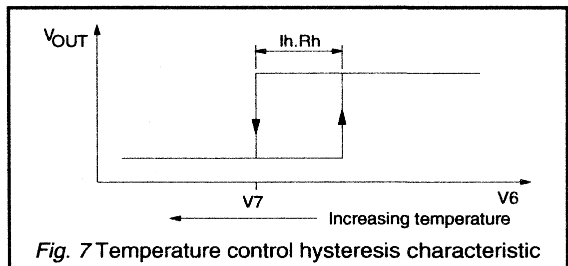


Fig. 7 Temperature control hysteresis characteristic

Hysteresis Resistor R_4

The comparator of the TDA1023 is designed with built-in hysteresis to eliminate instability and oscillation of the output which would cause spurious triggering of the triac. Apart from providing a stable two-state output, the hysteresis gives the comparator increased noise immunity and prevents half-waving.

Proportional Band (mV)	R_5 (kΩ)	R_4 (kΩ)	Hysteresis band (mV)
80	-	-	20
160	3.3	9.1	40
240	1.1	4.3	60
320	0.43	2.7	80
400	0.0	1.8	100

Table 2 Choice of components R_4 and R_5

Figure 7 shows the application of hysteresis to the comparator and the transfer characteristic obtained. The built-in hysteresis of 20mV; this may be increased by adding a resistor (R_4) from Pin 4 to ground which increases the current I_H. Pin 4 shorted to ground gives a maximum of 320mV. Table 2 gives the value of R_4 for a range of hysteresis settings.

When the proportional band (V_{pb}) is increased, it may be necessary to increase the hysteresis voltage (V_h). Table 2 also shows a range of proportional band settings, the values of R_5 required for these, the corresponding minimum hysteresis voltage and the maximum value of hysteresis resistor R_4.

Voltage (V)	AC rating (µF)	DC value (µF)	Catalogue Number
25	47	68	2222 016 90129
40	33	47	2222 016 90131
25	22	33	2222 015 90102
40	15	22	2222 015 90101
25	10	15	2222 015 90099
40	6.8	10	2222 015 90098

Table 3 Preferred capacitors for use with TDA1023

Power (W)	CENLEC t_0 (s)	C_T(DC) (µF)	$t_{0(nom)}$ (s)	$t_{0(min)}$ (s)	$t_{0(max)}$ (s)
2000	24.0	68	41	22	65
1800	16.0	47	28	15	45
1600	10.0	33	20	11	32
1400	7.0	22	13	7	21
1200	4.6	15	9	4.8	14
1000	2.0	10	6	3.2	9.6
800	0.8	10	6	3.2	9.6
600	0.3	10	6	3.2	9.6

Table 4 Timing capacitor values for 220V operation

Smoothing Capacitor, C_S

The smoothing capacitor is required to provide the supply current to the TDA1023 during the negative half cycles of the mains voltage waveform. As the TDA1023 possesses an internal voltage stabilization circuit, a high input ripple voltage can be tolerated. A practical preferred value of C_S is 220µF, 16V.

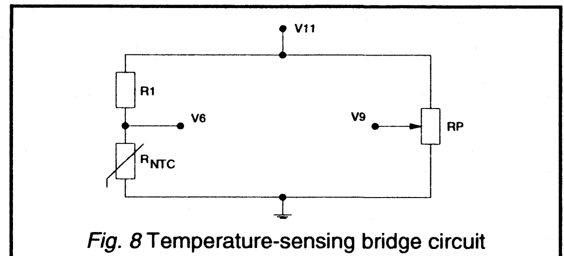


Fig. 8 Temperature-sensing bridge circuit

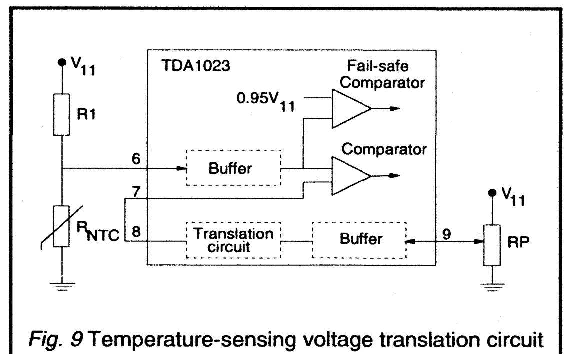


Fig. 9 Temperature-sensing voltage translation circuit

Timing Capacitor, C_T

The minimum repetition period required for a particular application was given in Table 1. This timing is selected using the external capacitor C_T. Typical electrolytic capacitors have wide tolerances: upto -10% to +50%. Moreover, the effective DC capacitance is different from the marked (AC) value, usually greater. Thus, the use of standard capacitors may lead to repetition periods far in excess of those required. A range of electrolytic capacitors has been developed for use with the TDA1023 (Table 3). All further references to C_T assume the use of the preferred capacitors which have the following advantages:

- DC capacitance is known for each marked AC value.
- Tolerance for the DC capacitance is ±20%.
- Very low leakage current (<1µA)
- Long lifetime (>100,000 hours at 40˚C).

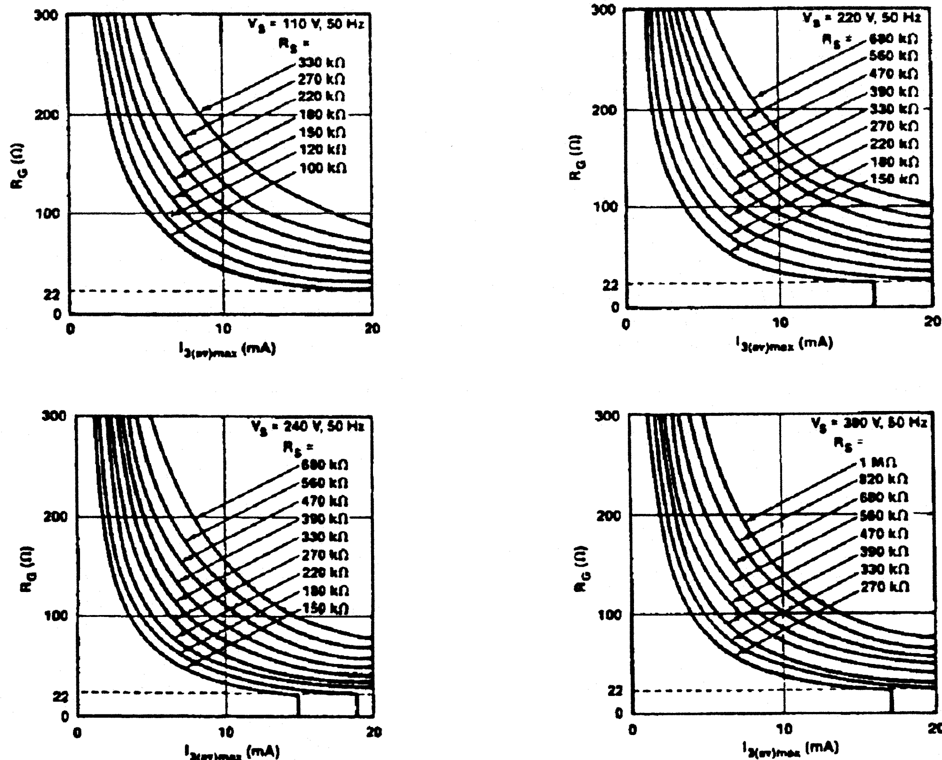


Fig. 10 Average gate current as a function of R_G with R_S and AC voltage as parameters

The timing circuit

The TDA1023 employs a triangular waveform for timing purposes. The advantages of using a triangular waveform are that for a given capacitor value the triangular waveform provides twice the repetition period that the sawtooth gives. This allows the use of smaller capacitors and minimises the effects of the capacitor leakage current thus reducing the spread in repetition periods.

The published data for the TDA1023 specifies the repetition period as 0.6 s ± 0.2 s/µF. Table 4 shows the minimum preferred value of C_T (DC value) to provide the required minimum repetition time for a range of appliance powers operating at 220V AC. The resulting nominal, minimum, and maximum repetition times are also given.

Input voltage translation circuit

Figure 8 shows a temperature sensing network which requires a minimum of components and eliminates performance spreads due to potentiometer tolerances. For applications where the input voltage variation is very much less than the available voltage then the required temperature will be controlled by a small angle of rotation of the potentiometer shaft. The TDA1023 voltage translation circuit allows the use of 80% of the potentiometer rotation giving accurate control of the temperature. If the voltage translation circuit is not used then pins 9 and 11 must be shorted together to disable the circuit. A block diagram of the translation circuit is shown in Fig. 9.

Fail-safe circuits

The TDA1023 is fail-safe for both short-circuit and open-circuit conditions. Either of these conditions will prevent production of trigger pulses for the triac.

Short-circuit sensing is automatically obtained from the normal temperature sensing circuit. When the thermistor input voltage is zero, the triac will never be triggered because the potentiometer slider voltage will be higher. To sense the open-circuit thermistor condition, an extra

comparator is used. This fail-safe comparator will inhibit output pulses if the thermistor input voltage rises above a reference value (see Fig. 9).

Determination of required supply current

Before any calculations concerning the required supply current can be made, the maximum average output current of the TDA1023 must be determined. The minimum supply current required is the sum of the following currents:

- the maximum average output current
- the current drawn by the temperature-sense circuit
- the current required by the integrated circuit.

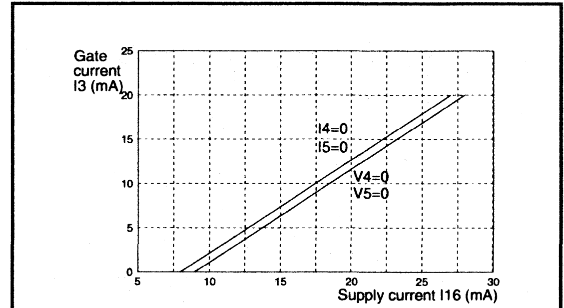


Fig. 11 Maximum required input current as function of gate current for limits of hysteresis band settings

Fig. 12 Input current as a function of R_D and power dissipation (with and without series diode)

For worst-case conditions, a 5% tolerance for R_S and R_G and a 10% variation of the mains is assumed. Figure 10 shows graphs of $I_{G(AV)max}$ as a function of R_G and R_S for four 50Hz supply voltages. Below R_G=22Ω there is no further increase in I_G as the output current is limited. The current drawn by the temperature-sensing circuit must not be greater than 1mA. The current consumption of the TDA1023 depends upon the hysteresis and proportional band settings. Figure 11 shows the minimum supply current as a function of the average output current for limit settings.

The mains dropping resistor, R_D

The value of the mains dropping resistor must be chosen such that the average supply current to the input of the TDA1023 is at least equal to the required minimum. The value of the resistor R_D is defined by the maximum current that can flow into Pin 16, the maximum peak mains voltage, and the minimum voltage at Pin 16. Table 5 shows practical values for $R_{D(min)}$ for four common mains supply voltages

Supply voltage V_s (V)	$R_{D(min)}$ (kΩ)
110	2.0
220	3.9
240	4.3
380	7.5

Table 5 Mains dropping resistor values

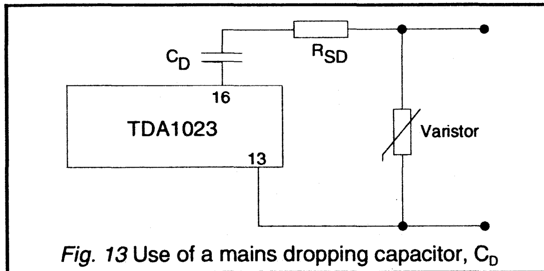


Fig. 13 Use of a mains dropping capacitor, C_D

The power dissipated by the dropping resistor has been computed for four mains voltages as a function of R_D and the results plotted on the graphs of Fig. 12. The power dissipated in R_D may be considerably reduced by the addition of a series diode as in Fig. 14. In this case there is no conduction through R_D during the negative half-cycle of the supply voltage, giving a reduction of more than 50% of the power dissipated in R_D.

Use of a mains dropping capacitor

It is possible to replace the mains dropping resistor and series diode with a capacitor, Fig. 13, and thereby reduce the power dissipation in the voltage reduction components still further. However, for mains voltages below 200V, the power dissipated by the dropping resistor is comparatively small and the use of a capacitor is not considered to be necessary. For mains voltages above 240V, the additional cost of the required high-voltage capacitor is not justified. For these reasons, it is recommended that capacitive voltage reduction is only used with mains supplies of 200V(RMS) or 240V(RMS).

When selecting a capacitor for mains voltage reduction, the following points must be considered:

- ***AC voltage rating***
- ***Suppression of mains-borne transients*** - A voltage-dependent resistor must be connected across the mains input to limit mains borne transients. For R_{SD}=390Ω this yields a maximum transient voltage of about 740V. For 220V operation, a VDR (catalogue number 2322 594 13512) will limit the supply voltage to the required level during current transients of up to about 200A. For 240V operation, a VDR (catalogue number 2322 594 13912) will limit the supply voltage to the required level during current transients of up to about 80A.

Component	Version A 400W - 1200W	Version B 1200W - 2000W
T_1	BT138-500	BT139-500
VDR [1]	350V, 1mA	350V, 1mA
D_1	BYX10G	BYX10G
R_1 [2]	18.7kΩ	18.7kΩ
R_{NTC} [3]	R25=22kΩ,B=4200k	R25=22kΩ, B=4200k
R_P	22kΩ	22kΩ
R_D	4.3kΩ	6.2kΩ
R_G	82Ω	82Ω
R_S	430kΩ	180kΩ
C_1	47nF	47nF
C_S	220µF, 16V	220µF, 16V
C_T	15µF (DC)	68µF (DC)
C_D [4]	680nF	470nF
R_{SD} [4]	390Ω	390Ω

Notes: 1. Cat. No. 2322 594 13512
2. 1% tolerance
3. Cat. No. 2322 642 12223
4. Only required if used in place of D_1 and R_D

Table 6 220V, 50Hz temperature controller components

- ***Limit of Inrush current*** - The capacitor C_D must not be chosen so large that the input current to the TDA1023 violates the absolute maximum specified in the published data. A practical value for C_D is 680nF. Resistor R_{SD} must also limit the peak value of the inrush current to less than 2A under worst case operating conditions. With a 240V (+10%) supply, the value of 390Ω (-5%) will limit the worst case peak value of the inrush current to:

$$\frac{240 \times 1.1}{0.95 \times 390}\sqrt{2} = 1.01\,\mathrm{A}$$

Triac protection

If the mains dropping circuit consists of capacitor C_D and resistor R_{SD}, a VDR must be included in the circuit as described above. This VDR will also protect the triac against current surges in the mains supply. If the mains dropping circuit consists of resistor R_D and diode D1, the VDR may be connected directly across the triac, giving improved protection due to the series resistance of the heater. Current surges in the supply will not harm the TDA1023 as the dropping resistor will limit the current to a safe level.

Application examples

The TDA1023 is intended primarily for room temperature control using electric panel heaters. The controllable heater power range is from 400W to 2000W, although the upper limit may be increased by suitable choice of triacs and/or heatsinks. The TDA1023 may also be used as a time proportional switch for cooker elements and similar devices, giving 100% control of the power dissipation.

1. Domestic panel heater controller

Figure 3 showed the design for a time proportional heater control using the TDA1023. Economies may be gained by the use of smaller or lower power components and so two versions are described in Table 6. Version A, for heaters from 400W to 1200W, uses a BT138 triac and a 15µF timing capacitor, version B, for heaters from 1200W to 2000W, uses a BT139 triac and a 68µF timing capacitor. Table 6 gives the necessary component values under worst case conditions for each of these versions for use with mains supplies of 220V, 50Hz.

The capacitor C1 has been included in the circuit of Fig. 3 to minimise sensor line interference pick-up. This is only necessary when the sensor is remote from the control circuit. The built-in hysteresis and proportional band provides optimum performance for panel heaters so pins 4 and 5 are not connected.

2. Temperature control of 2kW load.

For a load power of 2kW the BT139 triac must be used. The circuit is also that shown in Fig. 3. Table 7 gives a summary of the required component values.

Value of R_S

The required trigger pulse width can be found from Fig. 4 as a function of the load power, latch current and supply voltage (2000W, 60mA, and 220V, 50Hz, respectively): $t_{p(min)}$=64µs. A value of R_S=135kΩ provides a trigger pulse of the required duration. The next preferred value above this is 150kΩ, providing a $t_{p(min)}$ of approximately 70µs.

Value of R_G

The maximum value of R_G that may be used is determined by the minimum conditions to reliably trigger all samples of the triac. In Fig. 6 it can be seen that the operation point of 1.6V and 98 mA lies on the load line for 82Ω and this is the value chosen.

Component	Value	Remarks
T_1	BT139-500	
VDR	350V, 1mA	No. 2322 594 13912
D_1	BYX10G	
R_1	18.7kΩ	1% tolerance
R_{NTC}	R25=22kΩ, B=4200k	No. 2322 642 12223
R_P	22kΩ	
R_D	6.8kΩ	
R_G	82Ω	
R_S	150kΩ	
C_1	47nF	
C_S	220µF, 16V	
C_T	47µF (DC)	No. 2222 016 90129

Table 7 2000W, 220V, 50Hz temperature controller

Component	Value
T_1	BT139-500
VDR	ZnO, 350V, 1mA
D_1	BYX10G
R_1	4.7kΩ
R_2	4.7kΩ
R_P	47kΩ
R_D	5.6kΩ
R_G	82Ω
R_S	220kΩ
C_S	220µF, 16V
C_T	47µF, 25V

Table 8 Time proportional power controller

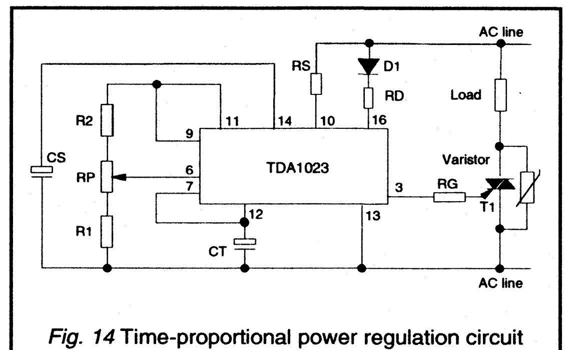


Fig. 14 Time-proportional power regulation circuit

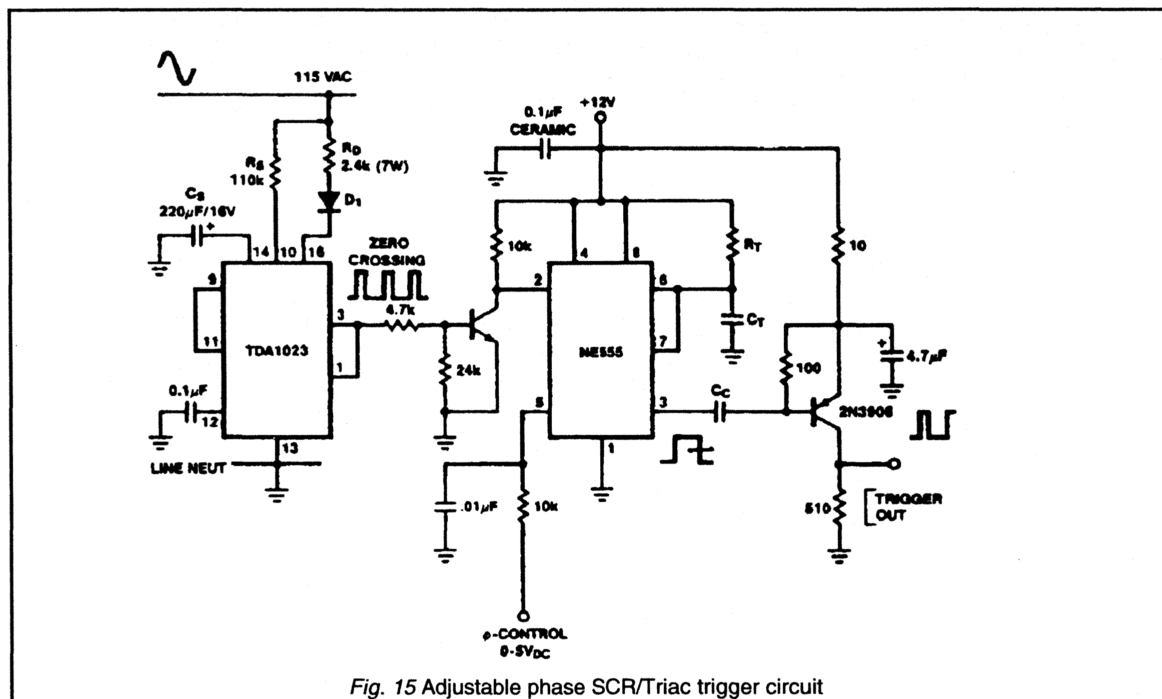


Fig. 15 Adjustable phase SCR/Triac trigger circuit

Value of C_T

For a load of 2kW, the repetition period must be at least 24s (from Table 1). From Table 4 the minimum preferred value of C_T to provide this period is 68µF. However, due to the different performance under AC and DC conditions, then from Table 3, the actual capacitor used should be 47µF, 25V.

Value of R_1 and R_P

For control over the range 5˚C to 35˚C and a thermistor characteristics with R_{25}=22kΩ, a suitable value of R_1 is 18.7kΩ ±1%. A suitable value for R_P is 22kΩ.

Value of R_D

First, the maximum average output current must be found. From Fig. 10 the maximum gate current I_G is given as a function of the values of resistors R_S and R_G. For this circuit $I_{G(AV)max}$=5 mA. Once the maximum average output current is known, the minimum required supply current can be found from Fig. 11. With minimum hysteresis and proportional band, the average value of the supply current is 12.5 mA. Using this value of input current the required value of R_D can be found from Fig. 12 giving R_D = 5.6 kΩ. The power dissipation in the resistor when diode D_1 is present in the circuit is than 5 W.

3. Time proportional power control

The TDA1023 may be used to provide proportional control of devices such as electric cooker elements. The temperature-sensing bridge is replaced by a potentiometer, the power in the load being proportional to the potentiometer setting. Proportional power control is thus obtained while the potentiometer voltage lies between the upper and lower limits of the triangular waveform comparator input.

As the timing capacitor is charged and discharged by current sources, the voltage across it will never reach zero, so that load power will be zero before the potentiometer reaches its minimum setting. Similarly, maximum load power is reached before the maximum setting of the potentiometer. This effect can be reduced by the addition of resistors R_1 and R_2. To ensure that 0% and 100% load power can be selected by the potentiometer setting, the values of R_1 and R_2 should each be limited to 10% of the value of R_P.

All the circuit components are calculated in the same way as for the temperature controller, including the timing capacitor C_T. An example circuit, with components suitable for the control of loads from 1kW to 2kW from 220V, 50Hz supplies, is shown in Fig. 14 and Table 8.

4. Phase control circuit using the TDA1023

Figure 15 shows an adjustable phase control trigger circuit suitable for thyristor or triac controller applications. The circuit uses the TDA1023 control chip and an NE555 timer device to give output phase control proportional to the input voltage command.

CHAPTER 7

Thermal Management

7.1.1 Thermal Considerations for Power Semiconductors
7.1.2 Heat dissipation

7.1.1 Thermal Considerations for Power Semiconductors

The perfect power switch is not yet available. All power semiconductors dissipate power internally both during the on-state and during the transition between the on and off states. The amount of power dissipated internally generally speaking increases in line with the power being switched by the semiconductor. The capability of a switch to operate in a particular circuit will therefore depend upon the amount of power dissipated internally and the rise in the operating temperature of the silicon junction that this power dissipation causes. It is therefore important that circuit designers are familiar with the thermal characteristics of power semiconductors and are able to calculate power dissipation limits and junction operating temperatures.

This chapter is divided into two parts. Part One describes the essential thermal properties of semiconductors and explains the concept of a limit in terms of continuous mode and pulse mode operation. Part Two gives worked examples showing junction temperature calculations for a variety of applied power pulse waveforms.

PART ONE

The power dissipation limit

The maximum allowable power dissipation forms a limit to the safe operating area of power transistors. Power dissipation causes a rise in junction temperature which will, in turn, start chemical and metallurgical changes. The rate at which these changes proceed is exponentially related to temperature, and thus prolonged operation of a power transistor above its junction temperature rating is liable to result in reduced life. Operation of a device at, or below, its power dissipation rating (together with careful consideration of thermal resistances associated with the device) ensures that the junction temperature rating is not exceeded.

All power semiconductors have a power dissipation limitation. For rectifier products such as diodes, thyristors and triacs, the power dissipation rating can be easily translated in terms of current ratings; in the on-state the voltage drop is well defined. Transistors are however somewhat more complicated. A transistor, be it a power MOSFET or a bipolar, can operate in its on-state at any voltage up to its maximum rating depending on the circuit conditions. It is therefore necessary to specify a safe operating area for transistors which specifies the power dissipation limit in-terms of a series of boundaries in the current and voltage plane. These operating areas are usually presented for mounting base temperatures of 25 °C, at higher temperatures operating conditions must be checked to ensure that junction temperatures are not exceeding the desired operating level.

Continuous power dissipation

The total power dissipation in a semiconductor may be calculated from the product of the on-state voltage and the forward conduction current. The heat dissipated in the junction of the device flows through the thermal resistance between the junction and the mounting base, $R_{thj\text{-}mb}$. The thermal equivalent circuit of Fig. 1 illustrates this heat flow; P_{tot} can be regarded as a thermal current, and the temperature difference between the junction and mounting base $\Delta T_{j\text{-}mb}$ as a thermal voltage. By analogy with Ohm's law, it follows that:

$$P_{tot} = \frac{T_j - T_{mb}}{R_{thj-mb}} \qquad 1$$

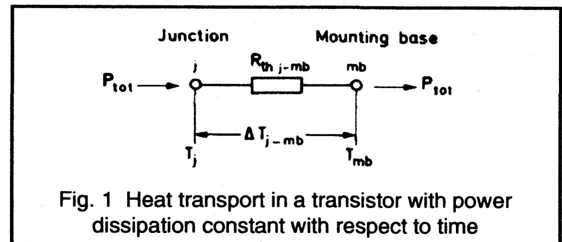


Fig. 1 Heat transport in a transistor with power dissipation constant with respect to time

Fig. 2 shows the dependence of the maximum power dissipation on the temperature of the mounting base. P_{totmax} is limited either by a maximum temperature difference:

$$\Delta T_{j-mb\,\max} = T_{jmax} - T_{mb\,K} \qquad 2$$

or by the maximum junction temperature T_{jmax} ($T_{mb\,K}$ is usually 25°C and is the value of T_{mb} above which the maximum power dissipation must be reduced to maintain the operating point within the safe operating area).

In the first case, $T_{mb} \leq T_{mb\,K}$:

$$P_{tot\,\max K} = \frac{\Delta T_{j-mb\,\max}}{R_{thj-mb}}; \qquad 3$$

that is, the power dissipation has a fixed limit value ($P_{tot\,\max K}$ is the maximum d.c. power dissipation *below* $T_{mb\,K}$). If the transistor is subjected to a mounting-base temperature $T_{mb\,1}$, its junction temperature will be less than T_{jmax} by an amount (T_{mbK} - $T_{mb\,1}$), as shown by the broken line in Fig. 2.

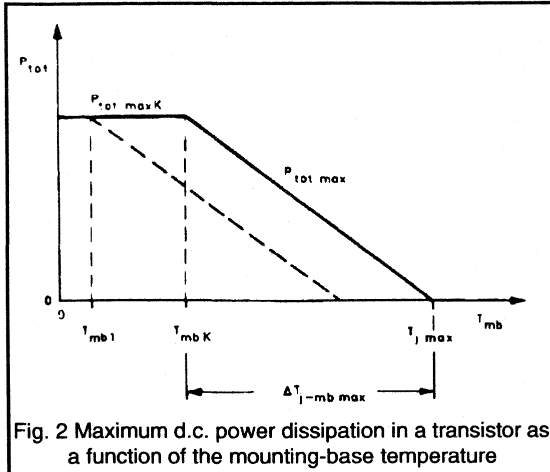


Fig. 2 Maximum d.c. power dissipation in a transistor as a function of the mounting-base temperature

In the second case, $T_{mb} > T_{mb\,K}$:

$$P_{tot\,max} = \frac{T_{jmax} - T_{mb}}{R_{thj-mb}}; \qquad 4$$

that is, the power dissipation must be reduced as the mounting base temperature increases along the sloping straight line in Fig. 2. Equation 4 shows that the lower the thermal resistance R_{thj-mb}, the steeper is the slope of the line. In this case, T_{mb} is the maximum mounting-base temperature that can occur in operation.

Example

The following data is provided for a particular transistor.

$P_{tot\,maxK} = 75$ W

$T_{jmax} = 175$ °C

$R_{thj-mb} \leq 2$ K/W

The maximum permissible power dissipation for continuous operation at a maximum mounting-base temperature of $T_{mb} = 80$ °C is required.

Note that the maximum value of T_{mb} is chosen to be significantly higher than the maximum ambient temperature to prevent an excessively large heatsink being required.

From Eq. 4 we obtain:

$$P_{tot\,max} = \frac{175 - 80}{2} W, \quad = 47.5\,W$$

Provided that the transistor is operated within SOAR limits, this value is permissible since it is below $P_{tot\,max\,K}$. The same result can be obtained graphically from the $P_{tot\,max}$ diagram (Fig. 3) for the relevant transistor.

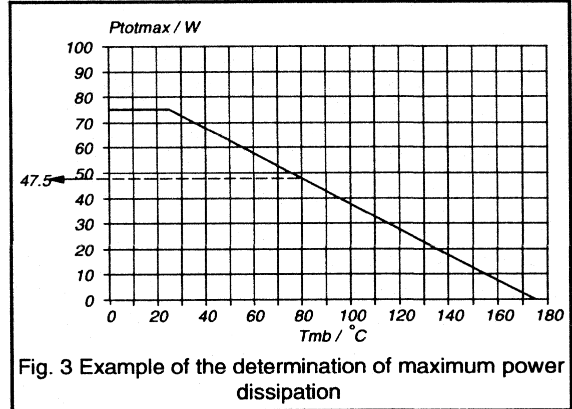


Fig. 3 Example of the determination of maximum power dissipation

Pulse power operation

When a power transistor is subjected to a pulsed load, higher peak power dissipation is permitted. The materials in a power transistor have a definite thermal capacity, and thus the critical junction temperature will not be reached instantaneously, even when excessive power is being dissipated in the device. The power dissipation limit may be extended for intermittent operation. The size of the extension will depend on the duration of the operation period (that is, pulse duration) and the frequency with which operation occurs (that is, duty factor).

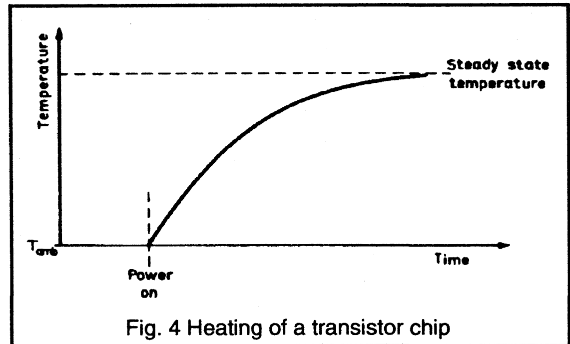


Fig. 4 Heating of a transistor chip

If power is applied to a transistor, the device will immediately commence to warm up (Fig. 4). If the power dissipation continues, a balance will be struck between heat generation and removal resulting in the stabilisation of T_j and ΔT_{j-mb}. Some heat energy will be stored by the thermal capacity of the device, and the stable conditions will be determined by the thermal resistances associated with the transistor and its thermal environment. When the power dissipation ceases, the device will cool (the heating and cooling laws will be identical, see Fig. 5). However, if the power dissipation ceases before the temperature of the transistor stabilises, the peak values of T_j and ΔT_{j-mb} will be less than

the values reached for the same level of continuous power dissipation (Fig. 6). If the second pulse is identical to the first, the peak temperature attained by the device at the end of the second pulse will be greater than that at the end of the first pulse. Further pulses will build up the temperature, until some new stable situation is attained (Fig. 7). The temperature of the device in this stable condition will fluctuate above and below the mean. If the upward excursions extend into the region of excessive T_j then the life expectancy of the device may be reduced. This can happen with high-power low-duty-factor pulses, even though the *average* power is below the d.c. rating of the device.

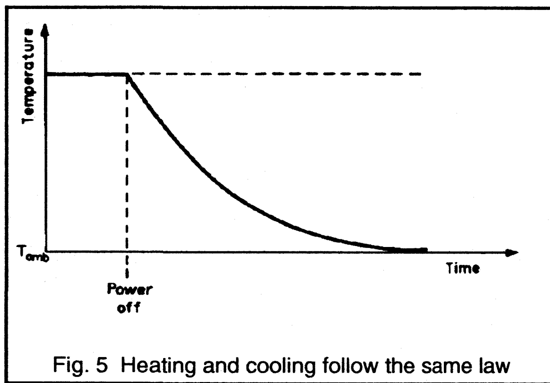


Fig. 5 Heating and cooling follow the same law

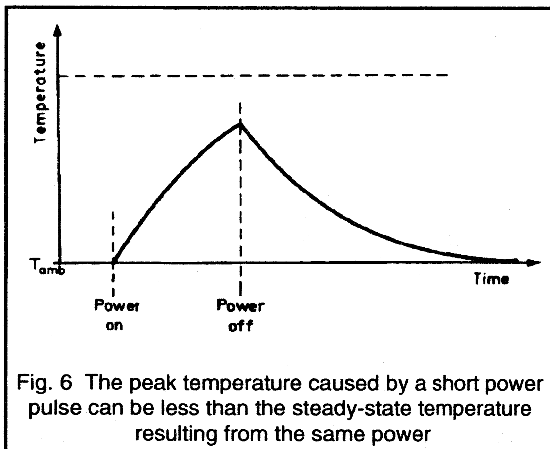


Fig. 6 The peak temperature caused by a short power pulse can be less than the steady-state temperature resulting from the same power

Fig. 8 shows a typical safe operating area for d.c. operation of a power MOSFET. The corresponding rectangular-pulse operating areas with a fixed duty factor, δ = 0, and the pulse time t_p as a parameter, are also shown. These boundaries represent the largest possible extension of the operating area for particular pulse times. When the pulse time becomes very short, the power dissipation does not have

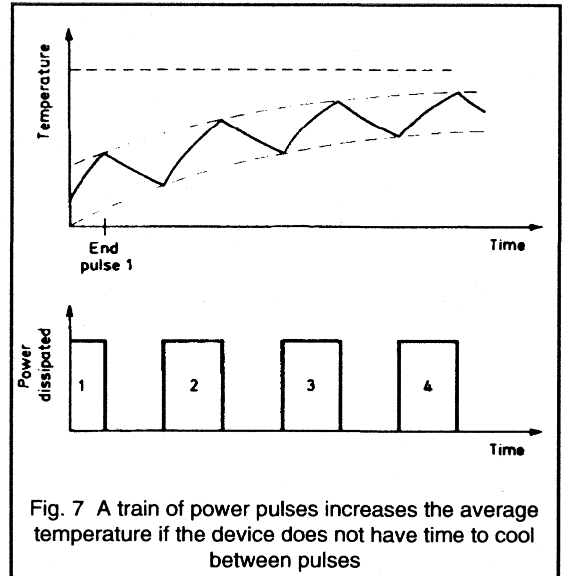


Fig. 7 A train of power pulses increases the average temperature if the device does not have time to cool between pulses

a limiting action and the pulse current and maximum voltage form the only limits. This rectangle represents the largest possible pulse operating area.

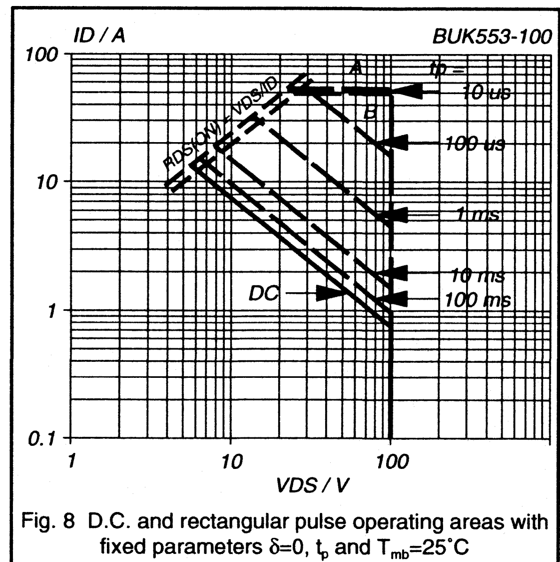


Fig. 8 D.C. and rectangular pulse operating areas with fixed parameters δ=0, t_p and T_{mb}=25˚C

In general, the shorter the pulse and the lower the frequency, the lower the temperature that the junction reaches. By analogy with Eq. 3, it follows that:

$$P_{tot\,M} = \frac{T_j - T_{mb}}{Z_{thj-mb}}, \qquad 5$$

where $Z_{thj\text{-}mb}$ is the transient thermal impedance between the junction and mounting base of the device. It depends on the pulse duration t_p, and the duty factor δ, where:

$$\delta = \frac{t_p}{T}, \quad (6)$$

and T is the pulse period. Fig. 9 shows a typical family of curves for thermal impedance against pulse duration, with duty factor as a parameter.

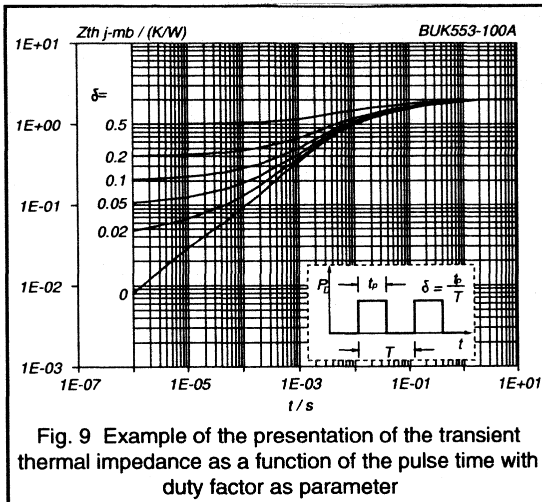


Fig. 9 Example of the presentation of the transient thermal impedance as a function of the pulse time with duty factor as parameter

Again, the maximum pulse power dissipation is limited either by the maximum temperature difference $\Delta T_{j\text{-}mb\,max}$ (Eq. 2), or by the maximum junction temperature T_{jmax}, and so by analogy with Eqs. 3 and 4.

$$P_{tot\,max\,K} = \frac{\Delta T_{j-mb\,max}}{Z_{thj-mb}}, \quad (7)$$

when $T_{mb} \leq T_{mb\,K}$, and:

$$P_{tot\,M\,max} = \frac{T_{jmax} - T_{mb}}{Z_{thj-mb}}, \quad (8)$$

when $T_{mb} > T_{mb\,K}$. That is, below a mounting-base temperature of $T_{mb\,K}$, the maximum power dissipation has a fixed limit value; and above $T_{mb\,K}$, the power dissipation must be reduced linearly with increasing mounting-base temperature.

Short pulse duration (Fig. 10a)

As the pulse duration becomes very short, the fluctuations of junction temperature become negligible, owing to the internal thermal capacity of the transistor. Consequently, the only factor to be considered is the heating of the junction by the average power dissipation; that is:

$$P_{tot(av)} = \delta P_{tot\,M} \quad (9)$$

The transient thermal impedance becomes:

$$\lim_{t_p \to 0} Z_{thj-mb} = \delta R_{thj-mb} \quad (10)$$

The $Z_{thj\text{-}mb}$ curves approach this value asymptotically as t_p decreases. Fig. 9 shows that, for duty factors in the range 0.1 to 0.5, the limit values given by Eq. 10 have virtually been reached at $t_p = 10^{-6}$ s.

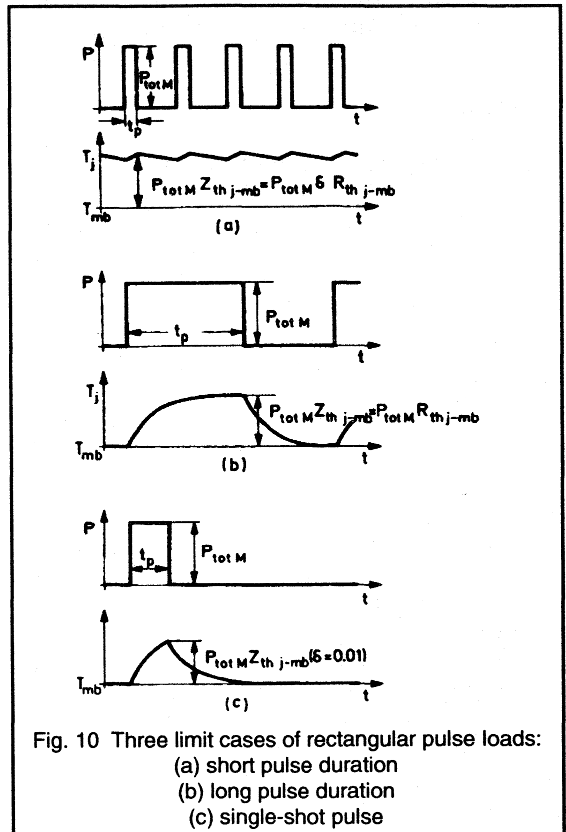


Fig. 10 Three limit cases of rectangular pulse loads:
(a) short pulse duration
(b) long pulse duration
(c) single-shot pulse

Long pulse duration (Fig. 10b)

As the pulse duration increases, the junction temperature approaches a stationary value towards the end of a pulse. The transient thermal impedance tends to the thermal resistance for continuous power dissipation; that is:

$$\lim_{t_p \to \infty} Z_{thj-mb} = R_{thj-mb} \quad (11)$$

Fig. 9 shows that Z_{thj-mb} approaches this value as t_p becomes large. In general, transient thermal effects die out in most power transistors within 0.1 to 1.0 seconds. This time depends on the material and construction of the case, the size of the chip, the way it is mounted, and other factors. Power pulses with a duration in excess of this time have approximately the same effect as a continuous load.

Single-shot pulses (Fig. 10c)

As the duty factor becomes very small, the junction tends to cool down completely between pulses so that each pulse can be treated individually. When considering single pulses, the Z_{thj-mb} values for $\delta = 0$ (Fig. 9) give sufficiently accurate results.

PART TWO

Calculating junction temperatures

Most applications which include power semiconductors usually involve some form of pulse mode operation. This section gives several worked examples showing how junction temperatures be simply calculated. Examples are given for a variety of waveforms:

(1) Periodic Waveforms

(2) Single Shot Waveforms

(3) Composite Waveforms

(4) A Pulse Burst

(5) Non Rectangular Pulses

From the point of view of reliability is is most important to know what the peak junction temperature will be when the power waveform is applied and also what the average junction temperature is going to be.

Peak junction temperature will usually occur at the end of an applied pulse and its calculation will involve transient thermal impedance. The average junction temperature (where applicable) is calculated by working out the average power dissipation using the d.c. thermal resistance.

When considering the junction temperature in a device, the following formula is used:

$$T_j = T_{mb} + \Delta T_{j-mb} \qquad 14$$

where ΔT_{j-mb} is found from a rearrangement of equation 7. In all the following examples the mounting base temperature (T_{mb}) is assumed to be 75˚C.

Periodic rectangular pulse

Figure 11 shows an example of a periodic rectangular pulse. This type of pulse is commonly found in switching applications. 100W is dissipated every 400µs for a period of 20µs, representing a duty cycle (δ) of 0.05. The peak junction temperature is calculated as follows:

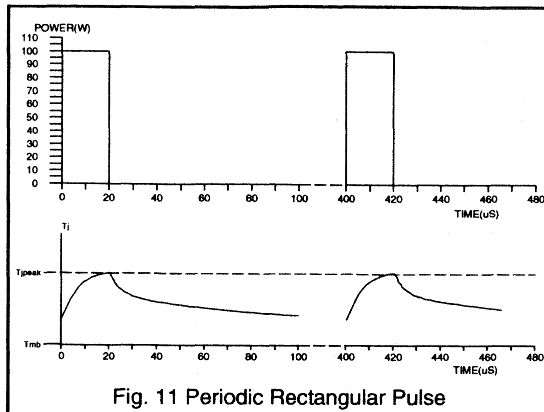


Fig. 11 Periodic Rectangular Pulse

Peak T_j:

$$t = 2 \times 10^{-5}\text{s}$$

$$P = 100\text{W}$$

$$\delta = \frac{20}{400} = 0.05$$

$$Z_{thj-mb} = 0.12\text{K/W}$$

$$\Delta T_{j-mb} = P \times Z_{thj-mb} = 100 \times 0.12 = 12°\text{C}$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 12 = 87°\text{C}$$

Average T_j:

$$P_{av} = P \times \delta = 100 \times 0.05 = 5\text{W}$$

$$\Delta T_{j-mb(av)} = P_{av} \times Z_{thj-mb(\delta=1)} = 5 \times 2 = 10°\text{C}$$

$$T_{j(av)} = T_{mb} + \Delta T_{j-mb(av)} = 75 + 10 = 85°\text{C}$$

The value for $Z_{th\,j-mb}$ is taken from the δ=0.05 curve shown in figure 12 (This diagram repeats figure 9 but has been simplified for clarity). The above calculation shows that the peak junction temperature will be 85˚C.

Single shot rectangular pulse

Figure 13 shows an example of a single shot rectangular pulse. The pulse used is the same as in the previous example, which should highlight the differences between periodic and single shot thermal calculations. For a single shot pulse, the time period between pulses is infinity, ie the duty cycle δ=0. In this example 100W is dissipated for a period of 20µs. To work out the peak junction temperature the following steps are used:

$$t = 2 \times 10^{-5}\text{s}$$

$$P = 100\text{W}$$

$$\delta = 0$$

$$Z_{thj-mb} = 0.04\text{K/W}$$

$$\Delta T_{j-mb} = P \times Z_{thj-mb} = 100 \times 0.04 = 4°\text{C}$$

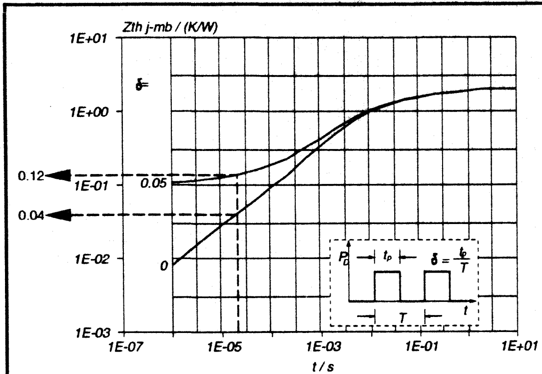


Fig. 12 Thermal impedance curves for δ=0.05 and δ=0

The value for $Z_{th\ j\text{-}mb}$ is taken from the δ=0 curve shown in figure 12. The above calculation shows that the peak junction temperature will be 4˚C above the mounting base temperature.

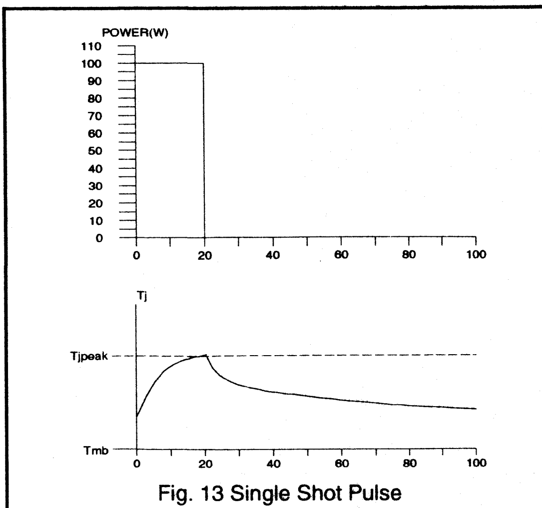


Fig. 13 Single Shot Pulse

For a single shot pulse, the average power dissipated and average junction temperature are not relevant.

Composite rectangular pulse

In practice, a power device frequently has to handle composite waveforms, rather than the simple rectangular pulses shown so far. This type of signal can be simulated by superimposing several rect
angular pulses which have a common period, but both positive and negative amplitudes, in addition to suitable values of t_p and δ.

By way of an example, consider the composite waveform shown in figure 14. To show the way in which the method used for periodic rectangular pulses is extended to cover composite waveforms, the waveform shown has been chosen to be an extension of the periodic rectangular pulse example. The period is 400µs, and the waveform consists of three rectangular pulses, namely 25W for 10µs, 5W for 150µs and 100W for 20µs. The peak junction temperature may be calculated at any point in the cycle. To be able to add the various effects of the pulses at this time, all the pulses, both positive and negative, must end at time t_x in the first calculation and t_y in the second calculation. Positive pulses increase the junction temperature, while negative pulses decrease it.

Calculation for time t_x

$$\Delta T_{j-mb@x} = P_1.Z_{thj-mb(t1)} + P_2.Z_{thj-mb(t3)} + P_3.Z_{thj-mb(t4)} - P_1.Z_{thj-mb(t2)} - P_2.Z_{thj-mb(t4)} \qquad 15$$

In equation 15, the values for P_1, P_2 and P_3 are known: P_1=40W, P_2=20W and P_3=100W. The Z_{th} values are taken from figure 9. For each term in the equation, the equivalent duty cycle must be worked out. For instance the first superimposed pulse in figure 14 lasts for a time t1 = 180µs, representing a duty cycle of 180/400 = 0.45 = δ. These values can then be used in conjunction with figure 9 to find a value for Z_{th}, which in this case is 0.9K/W. Table 1a gives the values calculated for this example.

		t1 180µs	t2 170µs	t3 150µs	t4 20µs
Repetitive T=400µs	δ Z_{th}	0.450 0.900	0.425 0.850	0.375 0.800	0.050 0.130
Single Shot T=∞	δ Z_{th}	0.000 0.130	0.000 0.125	0.000 0.120	0.000 0.040

Table 1a. Composite pulse parameters for time t_x

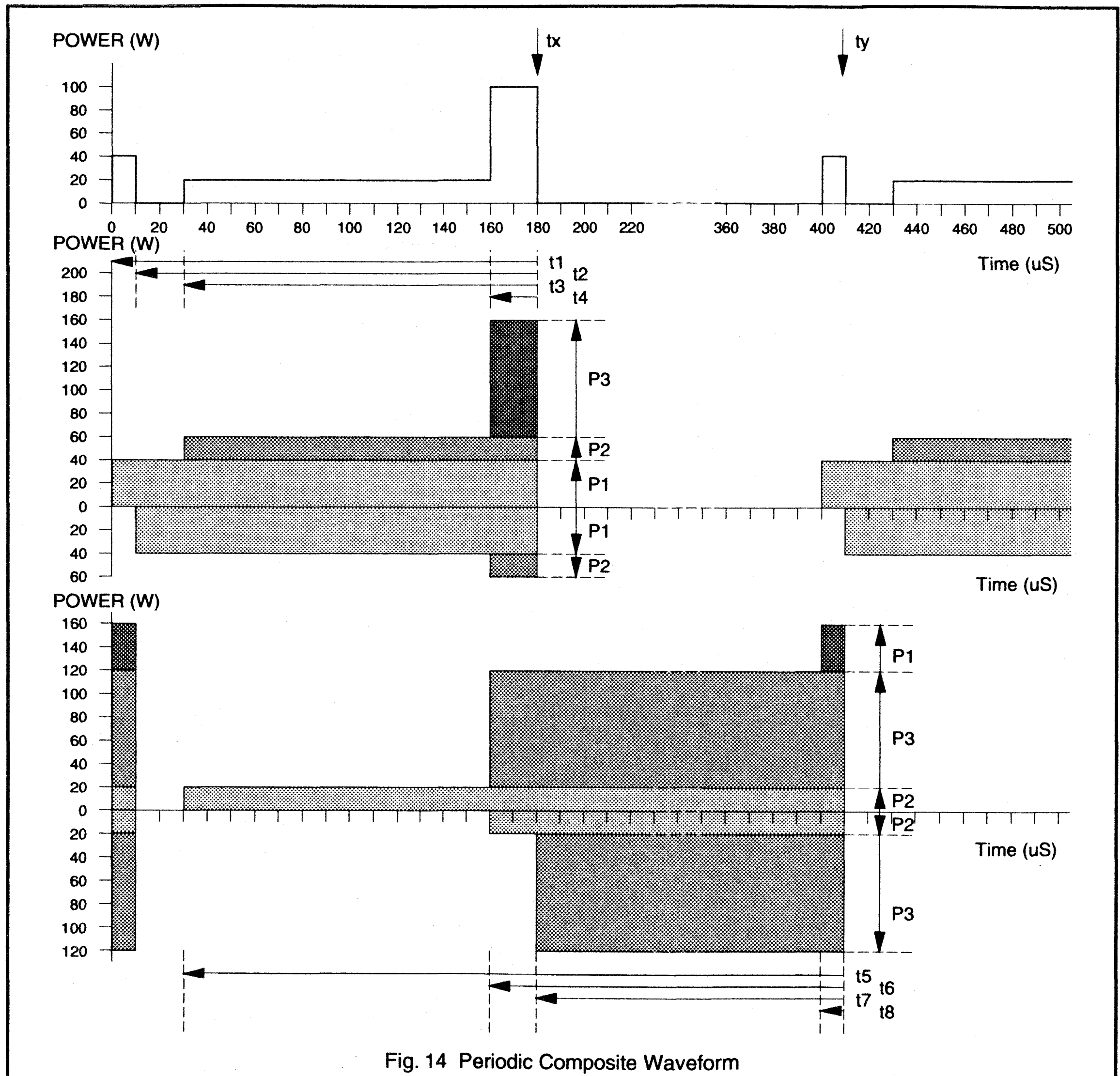


Fig. 14 Periodic Composite Waveform

Substituting these values into equation 15 for $T_{j\text{-mb}@x}$ gives

Repetitive:

$$\Delta T_{j-mb@x} = 40\times0.9+20\times0.85$$
$$+100\times0.13-40\times0.85$$
$$-20\times0.13$$
$$=29.4°C$$

$$T_j = T_{mb}+\Delta T_{j-mb} = 75+29.4 = 104.4°C$$

Single Shot:

$$\Delta T_{j-mb@x} = 40\times0.13+20\times0.125$$
$$+100\times0.04-40\times0.125$$
$$-20\times0.04$$
$$=5.9°C$$

$$T_j = T_{mb}+\Delta T_{j-mb} = 75+5.9 = 80.9°C$$

Hence the peak values of T_j are 104.4˚C for the repetitive

case, and 80.9˚C for the single shot case.

Calculation for time t_y

$$\Delta T_{j-mb@y} = P_2.Z_{thj-mb(t5)} + P_3.Z_{thj-mb(t6)} + P_1.Z_{thj-mb(t8)} - P_2.Z_{thj-mb(t6)} - P_3.Z_{thj-mb(t7)} \quad 16$$

where $Z_{thj-mb(t)}$ is the transient thermal impedance for a pulse time t.

		t5 380µs	t6 250µs	t7 230µs	t8 10µs
Repetitive	δ	0.950	0.625	0.575	0.025
T=400µs	Z_{th}	1.950	1.300	1.250	0.080
Single Shot	δ	0.000	0.000	0.000	0.000
T=∞	Z_{th}	0.200	0.160	0.150	0.030

Table 1b. Composite pulse parameters for time t_y

Substituting these values into equation 16 for $T_{j-mb@y}$ gives

Repetitive: $\Delta T_{j-mb@y} = 20 \times 1.95 + 100 \times 1.3 + 40 \times 0.08 - 20 \times 1.3 - 100 \times 1.25 = 21.2°C$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 21.2 = 96.2°C$$

Single Shot: $\Delta T_{j-mb@y} = 20 \times 0.2 + 100 \times 0.16 + 40 \times 0.03 - 20 \times 0.16 - 100 \times 0.15 = 3°C$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 3 = 78°C$$

Hence the peak values of T_j are 96.2˚C for the repetitive case, and 78˚C for the single shot case.

The average power dissipation and the average junction temperature can be calculated as follows

$$P_{av} = \frac{25 \times 10 + 5 \times 130 + 20 \times 100}{400} = 7.25W$$

$$\Delta T_{j-mb(av)} = P_{av} \times Z_{thj-mb(\delta=1)} = 7.25 \times 2 = 14.5°C$$

$$T_{j(av)} = T_{mb} + \Delta T_{j-mb(av)} = 75 + 14.5 = 89.5°C$$

Clearly, the junction temperature at time t_x should be higher than that at time t_y, and this is proven in the above calculations.

Burst pulses

Power devices are frequently subjected to a burst of pulses. This type of signal can be treated as a composite waveform and as in the previous example simulated by superimposing several rectangular pulses which have a common period, but both positive and negative amplitudes, in addition to suitable values of t_p and δ.

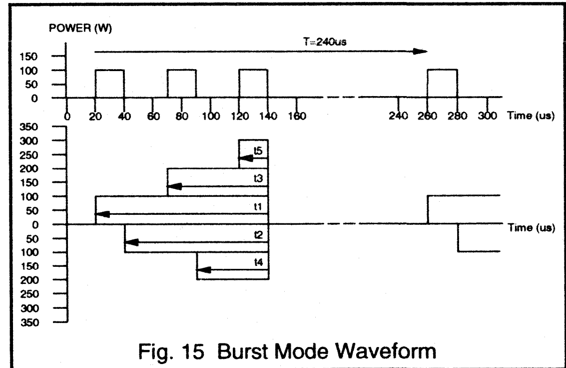


Fig. 15 Burst Mode Waveform

Consider the waveform shown in figure 15. The period is 240µs, and the burst consists of three rectangular pulses of 100W power and 20µs duration, separated by 30µs. The peak junction temperature will occur at the end of each burst at time t = t_x = 140µs. To be able to add the various effects of the pulses at this time, all the pulses, both positive and negative, must end at time t_x. Positive pulses increase the junction temperature, while negative pulses decrease it.

$$\Delta T_{j-mb@x} = P.Z_{thj-mb(t1)} + P.Z_{thj-mb(t3)} + P.Z_{thj-mb(t5)} - P.Z_{thj-mb(t2)} - P.Z_{thj-mb(t4)} \quad 17$$

where $Z_{thj-mb(t)}$ is the transient thermal impedance for a pulse time t.

The Z_{th} values are taken from figure 9. For each term in the equation, the equivalent duty cycle must be worked out. These values can then be used in conjunction with figure 9 to find a value for Z_{th}. Table 2 gives the values calculated for this example.

		t1 120µs	t2 100µs	t3 70µs	t4 50µs	t5 20µs
Repetitive	δ	0.500	0.420	0.290	0.210	0.083
T=240µs	Z_{th}	1.100	0.800	0.600	0.430	0.210
Single Shot	δ	0.000	0.000	0.000	0.000	0.000
T=∞	Z_{th}	0.100	0.090	0.075	0.060	0.040

Table 2. Burst Mode pulse parameters

Substituting these values into equation 17 gives

Repetitive:

$$\Delta T_{j-mb@x} = 100\times1.10 + 100\times0.60 + 100\times0.21 - 100\times0.80 - 100\times0.43 = 68°C$$

$$T_j = 75 + 68 = 143°C$$

Single Shot:

$$\Delta T_{j-mb@x} = 100\times0.10 + 100\times0.075 + 100\times0.04 - 100\times0.09 - 100\times0.06 = 6.5°C$$

$$T_j = 75 + 6.5 = 81.5°C$$

Hence the peak value of T_j is 143˚C for the repetitive case and 81.5˚C for the single shot case. To calculate the average junction temperature $T_{j(av)}$:

$$P_{av} = \frac{3\times100\times20}{240} = 25W$$

$$\Delta T_{j-mb(av)} = P_{av}\times Z_{thj-mb(\delta=1)} = 25\times2 = 50°C$$

$$T_{j(av)} = 75 + 50 = 125°C$$

The above example for the repetitive waveform highlights a case where the average junction temperature (125˚C) is well within limits but the composite pulse calculation shows the peak junction temperature to be significantly higher. For reasons of improved long term reliability it is usual to operate devices with a peak junction temperature below 125˚C.

Non-rectangular pulses

So far, the worked examples have only covered rectangular waveforms, however, triangular, trapeziodal and sinusoidal waveforms are also common. In order to apply the above thermal calculations to non rectangular waveforms, the waveform is approximated by a series of rectangles. Each rectangle represents part of the waveform. The equivalent rectangle must be equal in area to the section of the waveform it represents (ie the same energy) and also be of the same peak power. With reference to figure 16, a triangular waveform has been approximated to one rectangle in the first example, and two rectangles in the second. Obviously, increasing the number of sections the waveform is split into will improve the accuracy of the thermal calculations.

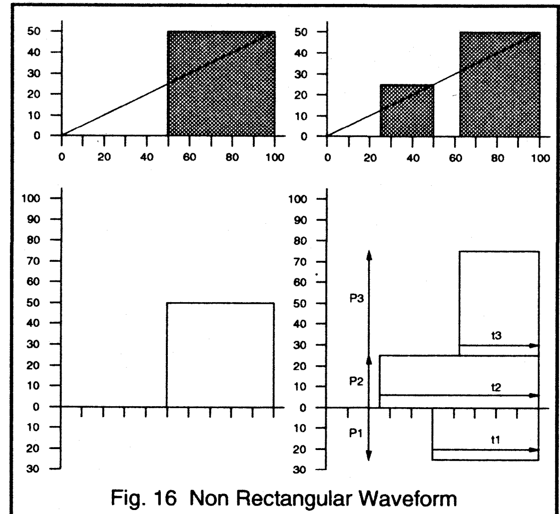


Fig. 16 Non Rectangular Waveform

In the first example, there is only one rectanglular pulse , of duration 50µs, dissipating 50W. So again using equation 14 and a rearrangement of equation 7

$$\Delta T_{j-mb} = P_{tot\,M}\times Z_{thj-mb}$$

Single Shot

$$\Delta T_{j-mb} = 50\times0.065 = 3.25°C$$

$$T_{jpeak} = 75 + 3.25 = 78.5°C$$

10% Duty cycle

$$\Delta T_{j-mb} = 50\times0.230 = 11.5°C$$

$$T_{jpeak} = 75 + 11.5 = 86.5°C$$

50% Duty cycle

$$\Delta T_{j-mb} = 50\times1.000 = 50°C$$

$$T_{jpeak} = 75 + 50 = 125°C$$

When the waveform is split into two rectangular pulses:

$$\Delta T_{j-mb} = P_3.Z_{thj-mb(t3)} + P_1.Z_{thj-mb(t1)} - P_2.Z_{thj-mb(t2)} \qquad 18$$

For this example P_1 = 25W, P_2 = 25W, P_3 = 50W. Table 3 below shows the rest of the parameters:

		t1	t2	t3
		75µs	50µs	37.5µs
Single Shot	D	0.000	0.000	0.000
T=∞	Z_{th}	0.085	0.065	0.055
10% Duty Cycle	D	0.075	0.050	0.037
T=1000µs	Z_{th}	0.210	0.140	0.120
50% Duty Cycle	D	0.375	0.250	0.188
T=200µs	Z_{th}	0.700	0.500	0.420

Table 3. Non Rectangular Pulse Calculations

Sustituting these values into equation 18 gives:

Single shot $\Delta T_{j-mb} = 50 \times 0.055 + 25 \times 0.085 - 25 \times 0.065$

$= 3.25°C$

$T_{jpeak} = 75 + 3.25 = 78.5°C$

10% Duty cycle $\Delta T_{j-mb} = 50 \times 0.12 + 25 \times 0.21 - 25 \times 0.14$

$= 7.75°C$

$T_{jpeak} = 75 + 7.75 = 82.5°C$

50% Duty cycle $\Delta T_{j-mb} = 50 \times 0.42 + 25 \times 0.7 - 25 \times 0.5$

$= 26°C$

$T_{jpeak} = 75 + 26 = 101°C$

To calculate the average junction temperature:

10% Duty Cycle $P_{av} = \frac{50 \times 50}{1000}$

$= 2.5W$

$\Delta T_{j-mb(av)} = P_{av} \times Z_{thj-mb(\delta=1)} = 2.5 \times 2 = 5°C$

$T_{j(av)} = 75 + 5 = 80°C$

50% Duty Cycle $P_{av} = \frac{50 \times 50}{200}$

$= 12.5W$

$\Delta T_{j-mb(av)} = P_{av} \times Z_{thj-mb(\delta=1)} = 12.5 \times 2 = 25°C$

$T_{j(av)} = 75 + 25 = 100°C$

Conclusion

A method has been presented to allow the calculation of average and peak junction tempreatures for a variety of pulse types. Several worked examples have shown calculations for various common waveforms. The method for non rectangular pulses can be applied to any wave shape, allowing temperature calculations for waveforms such as exponential and sinusiodal power pulses. For pulses such as these, care must be taken to ensure that the calculation gives the peak junction temperature, as it may not occur at the end of the pulse. In this instance several calculations must be performed with different endpoints to find the maximum junction temperature.

7.1.2 Heat Dissipation

All semiconductor failure mechanisms are temperature dependent and so the lower the junction temperature, the higher the reliability of the circuit. Thus our data specifies a maximum junction temperature which should not be exceeded under the worst probable conditions. However, derating the operating temperature from T_{jmax} is always desirable to improve the reliability still further. The junction temperature depends on both the power dissipated in the device and the thermal resistances (or impedances) associated with the device. Thus careful consideration of these thermal resistances (or impedances) allows the user to calculate the maximum power dissipation that will keep the junction temperature below a chosen value.

The formulae and diagrams given in this section can only be considered as a guide for determining the nature of a heatsink. This is because the thermal resistance of a heatsink depends on numerous parameters which cannot be predetermined. They include the position of the transistor on the heatsink, the extent to which air can flow unhindered, the ratio of the lengths of the sides of the heatsink, the screening effect of nearby components, and heating from these components. It is always advisable to check important temperatures in the finished equipment under the worst probable operating conditions. The more complex the heat dissipation conditions, the more important it becomes to carry out such checks.

Heat flow path

The heat generated in a semiconductor chip flows by various paths to the surroundings. Small signal devices do not usually require heatsinking; the heat flows from the junction to the mounting base which is in close contact with the case. Heat is then lost by the case to the surroundings by convection and radiation (Fig.1a). Power transistors, however, are usually mounted on heatsinks because of the higher power dissipation they handle. Heat flows from the transistor case to the heatsink by way of contact pressure, and the heatsink loses heat to the surroundings by convection and radiation, or by conduction to cooling water (Fig.1b). Generally air cooling is used so that the ambient referred to in Fig.1 is usually the surrounding air. Note that if this is the air inside an equipment case, the additional thermal resistance between the inside and outside of the equipment case should be taken into account.

Contact thermal resistance $R_{th\ mb-h}$

The thermal resistance between the transistor mounting base and the heatsink depends on the quality and size of the contact areas, the type of any intermediate plates used, and the contact pressure. Care should be taken when drilling holes in heatsinks to avoid burring and distorting the metal, and both mating surfaces should be clean. Paint finishes of normal thickness, up to 50 um (as a protection against electrolytic voltage corrosion), barely affect the thermal resistance. Transistor case and heatsink surfaces can never be perfectly flat, and so contact will take place on several points only, with a small air-gap over the rest of the area. The use of a soft substance to fill this gap lowers the contact thermal resistance. Normally, the gap is filled with a heatsinking compound which remains fairly viscous at normal transistor operating temperatures and has a high thermal conductivity. The use of such a compound also prevents moisture from penetrating between the contact surfaces. Proprietary heatsinking compounds are available which consist of a silicone grease loaded with some electrically insulating good thermally conducting powder such as alumina. The contact thermal resistance $R_{th\ mb-h}$ is usually small with respect to ($R_{th\ j-mb}$ + $R_{th\ h-amb}$) when cooling is by natural convection. However, the heatsink thermal resistance $R_{th\ h-amb}$ can be very small when either forced ventilation or water cooling are used, and thus a close thermal contact between the transistor case and heatsink becomes particularly important.

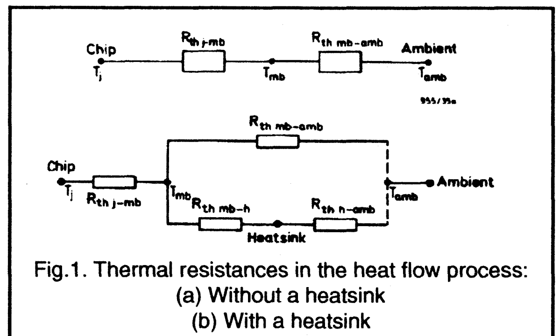


Fig.1. Thermal resistances in the heat flow process:
(a) Without a heatsink
(b) With a heatsink

Thermal resistance calculations

Figure 1a shows that, when a heatsink is not used, the total thermal resistance between junction and ambient is given by:

$$R_{thj-amb} = R_{thj-mb} + R_{thmb-amb} \qquad 1$$

However, power transistors are generally mounted on a heatsink since $R_{th\ j-amb}$ is not usually small enough to maintain temperatures within the chip below desired levels.

Figure 1b shows that, when a heatsink is used, the total thermal resistance is given by:

$$R_{thj-amb} = R_{thj-mb} + R_{thmb-h} + R_{thh-amb} \qquad 2$$

Note that the direct heat loss from the transistor case to the surroundings through $R_{th\ mb-amb}$ is negligibly small.

The first stage in determining the size and nature of the required heatsink is to calculate the maximum heatsink thermal resistance $R_{th\ h-amb}$ that will maintain the junction temperature below the desired value

Continuous operation

Under dc conditions, the maximum heatsink thermal resistance can be calculated directly from the maximum desired junction temperature.

$$R_{thj-amb} = \frac{T_j - T_{amb}}{P_{tot(av)}} \qquad 3$$

and

$$R_{thj-mb} = \frac{T_j - T_{mb}}{P_{tot(av)}} \qquad 4$$

Combining equations 2 and 3 gives:

$$R_{thh-amb} = \frac{T_j - T_{amb}}{P_{tot(av)}} - R_{thj-mb} - R_{thmb-h} \qquad 5$$

and substituting Eq 4 into Eq 5 gives:

$$R_{thh-amb} = \frac{T_{mb} - T_{amb}}{P_{tot(av)}} - R_{thmb-h} \qquad 6$$

The values of $R_{th\ j-mb}$ and $R_{th\ mb-h}$ are given in the published data. Thus, either Eq. 5 or Eq.6 can be used to find the maximum heatsink thermal resistance.

Intermittent operation

The thermal equivalent circuits of Fig.1 are inappropriate for intermittent operation, and the thermal impedance $Z_{th\ j-mb}$ should be considered.

$$P_{totM} = \frac{T_j - T_{mb}}{Z_{thj-mb}}$$

thus:

$$T_{mb} = T_j - P_{totM} . Z_{thj-mb} \qquad 7$$

The mounting-base temperature has always been assumed to remain constant under intermittent operation. This assumption is known to be valid in practice provided that the pulse time is less than about one second. The mounting-base temperature does not change significantly under these conditions as indicated in Fig.2. This is because heatsinks have a high thermal capacity and thus a high thermal time-constant.

Thus Eq.6 is valid for intermittent operation, provided that the pulse time is less than one second. The value of Tmb can be calculated from Eq. 7, and the heatsink thermal resistance can be obtained from Eq.6.

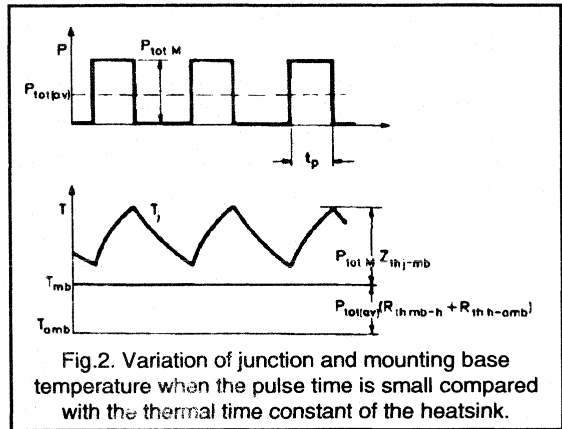


Fig.2. Variation of junction and mounting base temperature when the pulse time is small compared with the thermal time constant of the heatsink.

The thermal time constant of a transistor is defined as that time at which the junction temperature has reached 70% of its final value after being subject to a constant power dissipation at a constant mounting base temperature.

Now, if the pulse duration tp exceeds one second, the transistor is temporarily in thermal equilibrium since such a pulse duration is significantly greater than the thermal time-constant of most transistors. Consequently, for pulse times of more than one second, the temperature difference T_j - T_{mb} reaches a stationary final value (Fig.3) and Eq.7 should be replaced by:

$$T_{mb} = T_j - P_{totM} . R_{thj-mb} \qquad 8$$

In addition, it is no longer valid to assume that the mounting base temperature is constant since the pulse time is also no longer small with respect to the thermal time constant of the heatsink.

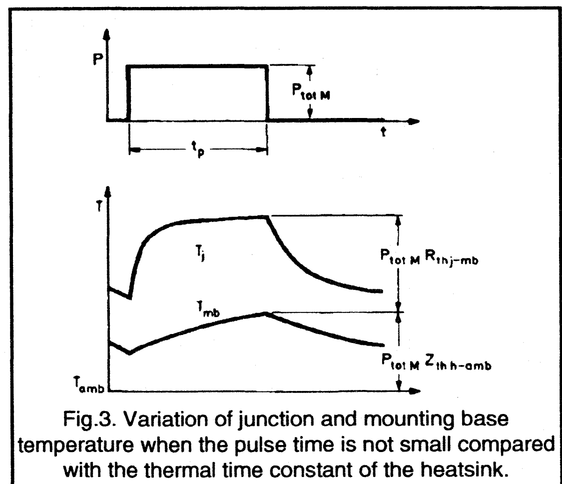


Fig.3. Variation of junction and mounting base temperature when the pulse time is not small compared with the thermal time constant of the heatsink.

Smaller heatsinks for intermittent operation

In many instances, the thermal capacity of a heatsink can be utilised to design a smaller heatsink for intermittent operation than would be necessary for the same level of continuous power dissipation. The average power dissipation in Eq. 6 is replaced by the peak power dissipation to obtain the value of the thermal impedance between the heatsink and the surroundings

$$Z_{thh-amb} = \frac{T_{mb} - T_{amb}}{P_{totM}} - R_{thmb-h} \qquad 9$$

The value of $Z_{th\,h\text{-}amb}$ will be less than the comparable thermal resistance and thus a smaller heatsink can be designed than that obtained using the too large value calculated from Eq.6.

Heatsinks

Three varieties of heatsink are in common use: flat plates (including chassis), diecast finned heatsinks, and extruded finned heatsinks. The material normally used for heatsink construction is aluminium although copper may be used with advantage for flat-sheet heatsinks. Small finned clips are sometimes used to improve the dissipation of low-power transistors.

Heatsink finish

Heatsink thermal resistance is a function of surface finish. A painted surface will have a greater emissivity than a bright unpainted one. The effect is most marked with flat plate heatsinks, where about one third of the heat is dissipated by radiation. The colour of the paint used is relatively unimportant, and the thermal resistance of a flat plate heatsink painted gloss white will be only about 3% higher than that of the same heatsink painted matt black. With finned heatsinks, painting is less effective since heat radiated from most fins will fall on adjacent fins but it is still worthwhile. Both anodising and etching will decrease the thermal resistivity. Metallic type paints, such as aluminium paint, have the lowest emissivities, although they are approximately ten times better than a bright aluminium metal finish.

Flat-plate heatsinks

The simplest type of heatsink is a flat metal plate to which the transistor is attached. Such heatsinks are used both in the form of separate plates and as the equipment chassis itself. The thermal resistance obtained depends on the thickness area, and the orientation of the plate, as well as on the finish and power dissipated. A plate mounted horizontally will have about twice the thermal resistance of a vertically mounted plate. This is particularly important where the equipment chassis itself is used as the heatsink.

In Fig.4, the thermal resistance of a blackened heatsink is plotted against surface area (one side) with power dissipation as a parameter. The graph is accurate to within 25% for nearly square plates, where the ratio of the lengths of the sides is less than 1.25:1.

Finned heatsinks

Finned heatsinks may be made by stacking flat plates, although it is usually more economical to use ready made diecast or extruded heatsinks. Since most commercially available finned heatsinks are of reasonably optimum design, it is possible to compare them on the basis of the overall volume which they occupy. This comparison is made in Fig.4 for heatsinks with their fins mounted vertically; again, the graph is accurate to 25%.

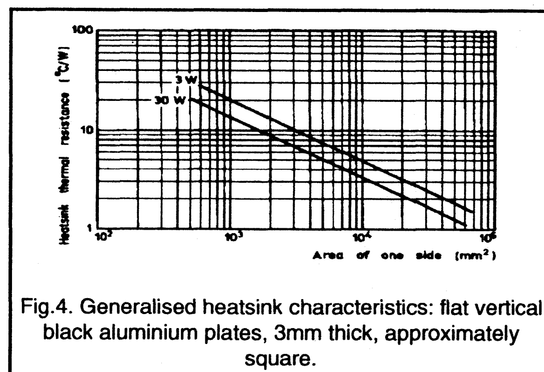


Fig.4. Generalised heatsink characteristics: flat vertical black aluminium plates, 3mm thick, approximately square.

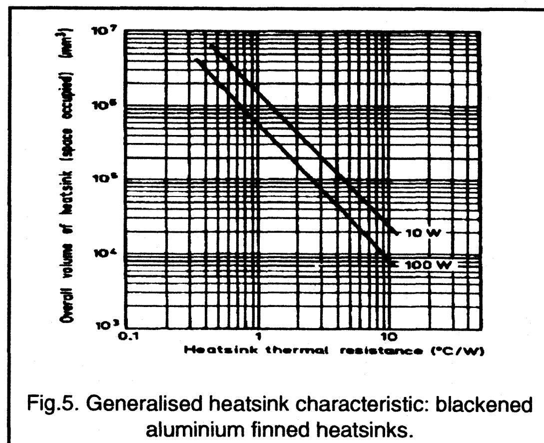


Fig.5. Generalised heatsink characteristic: blackened aluminium finned heatsinks.

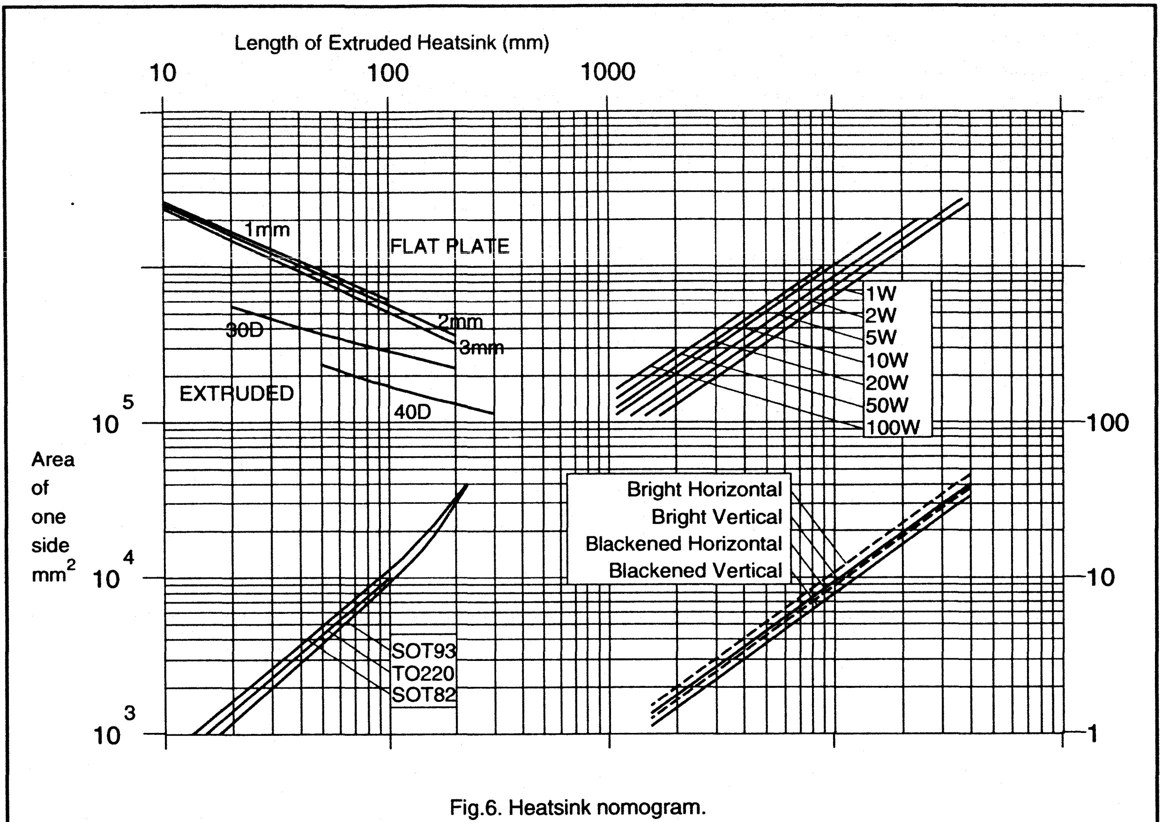


Fig.6. Heatsink nomogram.

Heatsink dimensions

The maximum thermal resistance through which sufficient power can be dissipated without damaging the transistor can be calculated as discussed previously. This section explains how to arrive at a type and size of heatsink that gives a sufficiently low thermal resistance.

Natural air cooling

The required size of aluminium heatsinks - whether flat or extruded (finned) can be derived from the nomogram in Fig.6. Like all heatsinks diagrams, the nomogram does not give exact values for $R_{th\ h\text{-}amb}$ as a function of the dimensions since the practical conditions always deviate to some extent from those under which the nomogram was drawn up. The actual values for the heatsink thermal resistance may differ by up to 10% from the nomogram values. Consequently, it is advisable to take temperature measurements in the finished equipment, particularly where the thermal conditions are critical.

The conditions to which the nomogram applies are as follows:

- natural air cooling (unimpeded natural convection with no build up of heat);
- ambient temperature about 25˚C, measured about 50mm below the lower edge of the heatsink (see Fig.7);
- atmospheric pressure about 10 N/m^2;
- single mounting (that is, not affected by nearby heatsinks);
- distance between the bottom of the heatsink and the base of a draught-free space about 100mm (see Fig.7);
- transistor mounted roughly in the centre of the heatsink (this is not so important for finned heatsinks because of the good thermal conduction).

The appropriately-sized heatsink is found as follows.

1. Enter the nomogram from the right hand side of section 1 at the appropriate $R_{th\ h\text{-}amb}$ value (see Fig.8). Move horizontally to the left, until the appropriate curve for orientation and surface finish is reached.

2. Move vertically upwards to intersect the appropriate power dissipation curve in section 2.
3. Move horizontally to the left into section 3 for the desired thickness of a flat-plate heatsink, or the type of extrusion.
4. If an extruded heatsink is required, move vertically upwards to obtain its length (figures 9a and 9b give the outlines of the extrusions).
5. If a flat-plate heatsink is to be used, move vertically downwards to intersect the appropriate curve for envelope type in section 4.
6. Move horizontally to the left to obtain heatsink area.
7. The heatsink dimensions should not exceed the ratio of 1.25:1.

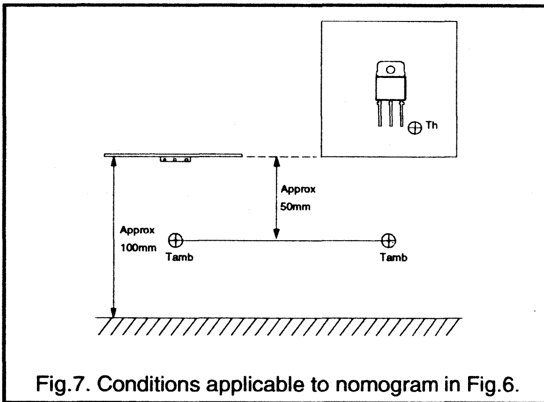


Fig.7. Conditions applicable to nomogram in Fig.6.

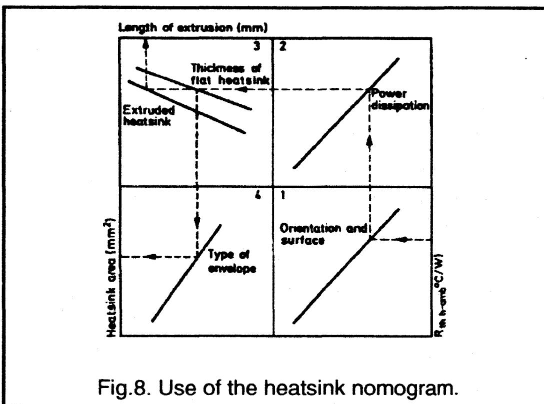


Fig.8. Use of the heatsink nomogram.

The curves in section 2 take account of the non linear nature of the relationship between the temperature drop across the heatsink and the power dissipation loss. Thus, at a constant value of the heatsink thermal resistance, the greater the power dissipation, the smaller is the required size of heatsink. This is illustrated by the following example.

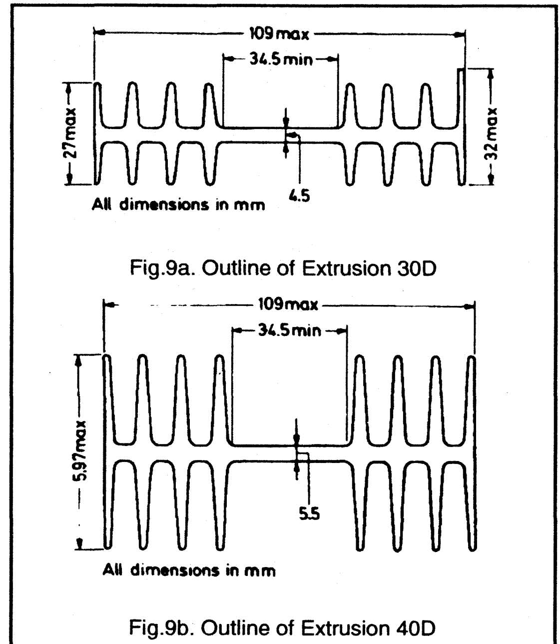


Fig.9a. Outline of Extrusion 30D

Fig.9b. Outline of Extrusion 40D

Example

An extruded heatsink mounted vertically and with a painted surface is required to have a maximum thermal resistance of $R_{th\ h\text{-}amb}$ = 2.6 ˚C/W at the following powers:

$$(a)P_{tot(av)} = 5W \quad (b)P_{tot(av)} = 50W$$

Enter the nomogram at the appropriate value of the thermal resistance in section 1, and via either the 50W or 5W line in section 2, the appropriate lengths of the extruded heatsink 30D are found to be:

(a) length = 110mm and (b) length = 44mm.

Case (b) requires a shorter length since the temperature difference is ten times greater than in case (a).

As the ambient temperature increases beyond 25˚C, so does the temperature of the heatsink and thus the thermal resistance (at constant power) decreases owing to the increasing role of radiation in the heat removal process. Consequently, a heatsink with dimensions derived from Fig.6 at T_{amb} > 25˚C will be more than adequate. If the maximum ambient temperature is less than 25˚C, then the thermal resistance will increase slightly. However, any increase will lie within the limits of accuracy of the nomogram and within the limits set by other uncertainties associated with heatsink calculations.

For heatsinks with relatively small areas, a considerable part of the heat is dissipated from the transistor case. This is why the curves in section 4 tend to flatten out with decreasing heatsink area. The area of extruded heatsinks is always large with respect to the surface of the transistor case, even when the length is small.

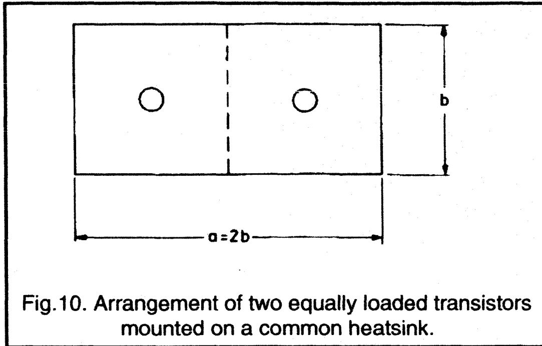


Fig.10. Arrangement of two equally loaded transistors mounted on a common heatsink.

If several transistors are mounted on a common heatsink, each transistor should be associated with a particular section of the heatsink (either an area or length according to type) whose maximum thermal resistance is calculated from equations 5 or 6; that is, without taking the heat produced by nearby transistors into account. From the sum of these areas or lengths, the size of the common heatsink can then be obtained. If a flat heatsink is used, the transistors are best arranged as shown in Fig.10. The maximum mounting base temperatures of transistors in such a grouping should always be checked once the equipment has been constructed.

Forced air cooling

If the thermal resistance needs to be much less than 1˚C/W, or the heatsink not too large, forced air cooling by means of fans can be provided. Apart from the size of the heatsink, the thermal resistance now only depends on the speed of the cooling air. Provided that the cooling air flows parallel to the fins and with sufficient speed (>0.5m/s), the thermal resistance hardly depends on the power dissipation and the orientation of the heatsink. Note that turbulence in the air current can result in practical values deviating from theoretical values.

Figure 11 shows the form in which the thermal resistances for forced air cooling are given in the case of extruded heatsinks. It also shows the reduction in thermal resistance or length of heatsink which may be obtained with forced air cooling.

The effect of forced air cooling in the case of flat heatsinks is seen from Fig.12. Here, too, the dissipated power and the orientation of the heatsink have only a slight effect on the thermal resistance, provided that the air flow is sufficiently fast.

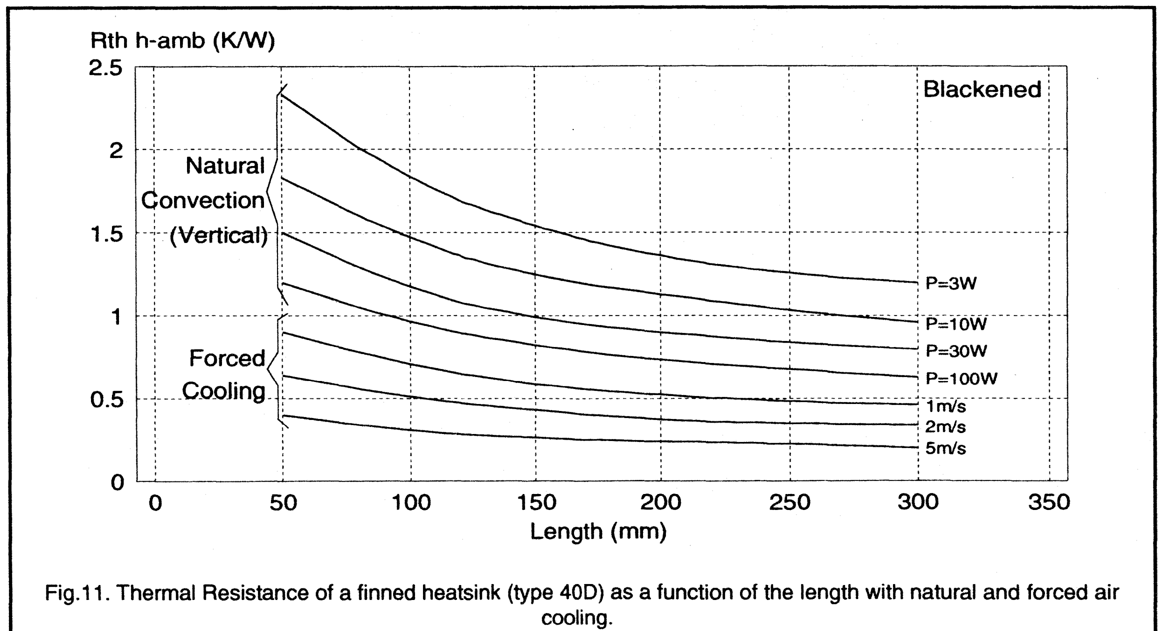


Fig.11. Thermal Resistance of a finned heatsink (type 40D) as a function of the length with natural and forced air cooling.

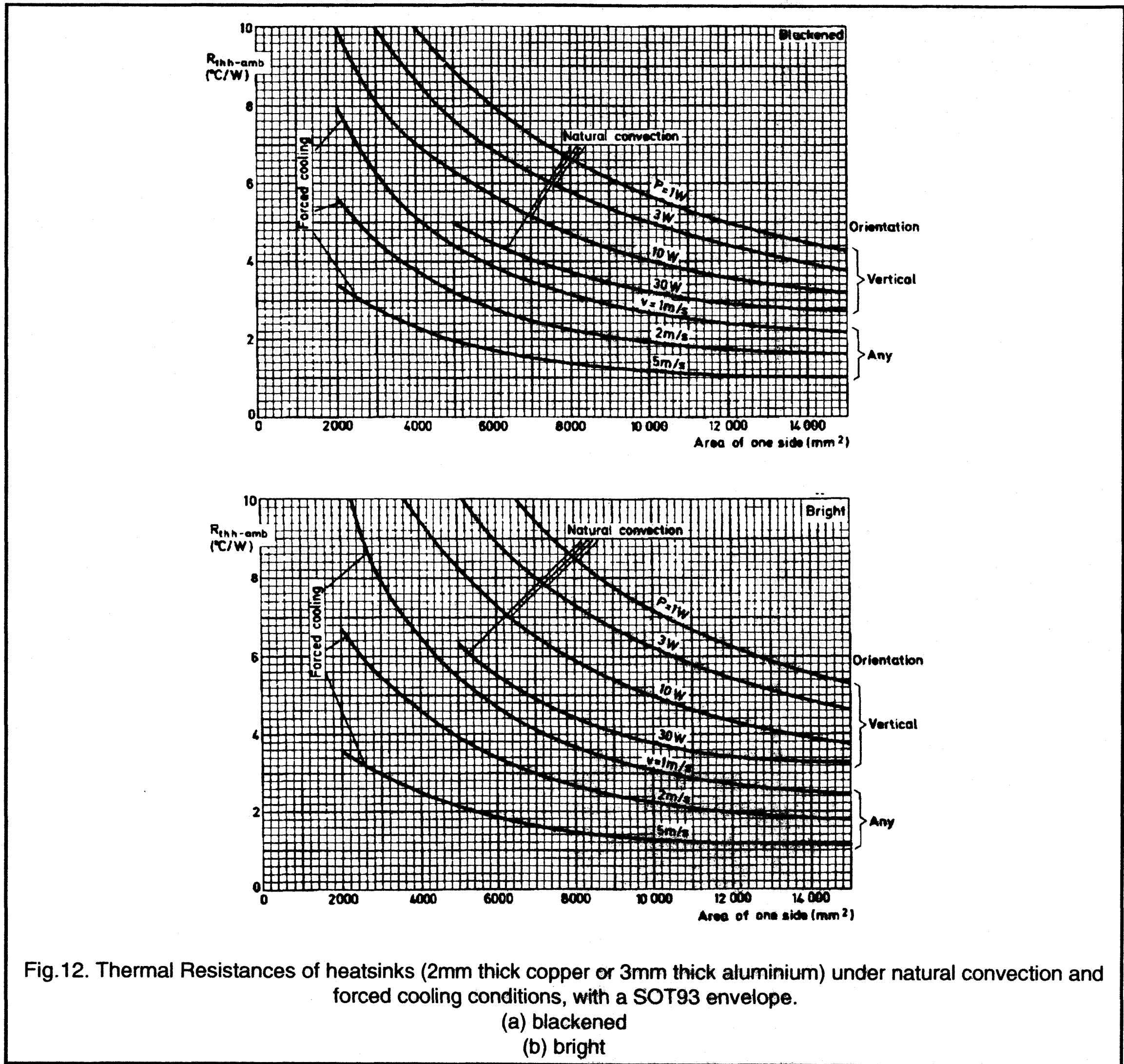


Fig.12. Thermal Resistances of heatsinks (2mm thick copper or 3mm thick aluminium) under natural convection and forced cooling conditions, with a SOT93 envelope.
(a) blackened
(b) bright

Summary

The majority of power transistors require heatsinking, and once the maximum thermal resistance that will maintain the device's junction temperature below its rating has been calculated, a heatsink of appropriate type and size can be chosen. The practical conditions under which a transistor will be operated are likely to differ from the theoretical considerations used to determine the required heatsink, and thus temperatures should always be checked in the finished equipment. Finally, some applications require a small heatsink, or one with a very low thermal resistance, in which case forced air cooling by means of fans should be provided.

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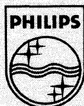

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